3.3 kV SiC MOSFETs Accelerate **Grid-Connected Energy Storage Dr Ranbir Singh Executive Vice President, GeneSiC Product Line** 17th, April 2024



Navitas Electrify Our World™

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The Electricity Grid



• USA Grid

- 11,000 Power Plants & over 158M residential & commercial customers
- Three Distinct Functions
 - Generation (Power Plants)
 - Transmission (HV lines)
 - Distribution (Sub-Stations, Industrial & Commercial Residential)
- Goal of the Grid
 - To efficiently and reliability <u>match</u> the power demand



Source: GAO (2023)

Matching Supply and Demand

Various types of Generation are required throughout the day to support demand:

- Baseline Supports steady state minimum level of production
- Intermediate Operated at expected peak loads
- Peaking Highest peaks of demand



Source: GAO (2023)

Wind/Solar Energy is Difficult to Support Peak Demand **Navitas**

- Solar & Wind Energy weather dependent and does not always match demand (e.g. duck curve)
- Energy storage can reserve renewable energy for peak demand needs



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Main Types of Energy Storage



- Majority of energy storage is in pumped hydroelectric
 - High energy, long discharge time, expensive and large setup
- **Li-on batteries**
 - Fast response time, low-medium energy, medium discharge time, smaller footprint, modular
 - 16GW megawatts of battery capacity in 2023 and 15 GW planned in 2024 ۲

Utility-scale Energy Storage Operation by Technology







Utility-Attached Storage for Renewable Energy Sources Navitas

- Reduces costs Purchase of inexpensive electricity during periods of low demand and supply
- Storage replaces adding generation capacity
- Supports peaking capacity demands with fast response times
- Provides back-up power during outages
- Installations are fast and relatively low cost compared to other generation sources



BESS installation can smooth out variability in the adjacent wind farm, supporting 1GW into the Grid over 4-6 hours



Utility-scale BESS to the California Independent System Operator, with 548 MWh capacity, supporting 26,000 homes

Vision for Electricity Production and T&D Infrastructure Navitas

- Identifying grid-connected storage as critical for more reliable, more cost-effective models
- Energy storage improves T&D performance by compensating for electrical anomalies and disturbances such as:
 - Variations in voltage, (e.g., short-term spikes or dips, longer-term surges, or sags)
 - Variations in the primary frequency at which power is delivered
 - Low power-factor (voltage and current excessively out of phase with each other)
 - Harmonics (the presence of currents or voltages at frequencies other than the primary) interruptions in service



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Integrating a BESS with Medium Voltage (MV) Grid

- BESS is integrated to an MV grid (2.3 kV, 4.16 kV or 13.8 kV) using an isolated topology such as a dual active bridge (DAB) followed by an active front-end converter (AFEC)
- A 3-level, neutral-point clamped topology both reduces filter requirements compared to a twolevel topology, and the voltage stress across the SiC MOSFETs
- Depending on grid voltage, a series connection of the SiC 3.3 kV MOSFET-Diode devices is possible

System topology for interconnecting the BESS system to an MV grid

LV Side BESS Vin DC Mediun Frequency Transformer MOSFETS lepending on the ari

3.3 kv SiC GeneSiC MOSFETs



Integrating a BESS with Medium Voltage (MV) Grid

- The LV side is made through 1,200 V SiC devices
- In the DAB, the MV transformer (LV to MV conversion) can be operated between 10 - 20 kHz
- Single or three-phase system can be used depending on the power requirements

System topology for interconnecting the BESS system to an MV grid





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3.3kV SiC MOSFET with Mono-Integrated MPS Diode

- Further efficiency and reliability advantages can be achieved by monolithically integrating a Merged PiN Schottky (MPS) diode within the MOSFET
- This enables free-wheeling diode operation (low conduction and switching losses) without an externally-connected Schottky diode, while reducing the parasitic inductance associated with an external diode connection.



Cross-sectional device schematic of 3.3 kV SiC MOSFET with monolithically-integrated Schottky rectifier.

3.3kV SiC MOSFET with Mono-Integrated MPS Diode

- This bypasses the built-in P-Well/N-Drift body-diode of the DMOSFET structure whose operation can induce faulting of the basal-plane dislocations inevitably present within the N- drift layer of the DMOSFET
- Advantages Include:
 - More efficient bi-directional performance
 - Temperature independent switching
 - Low switching and conduction losses
 - Reduced cooling requirements
 - Superior long-term reliability
 - Ease of paralleling and lower costs



Cross-sectional device schematic of 3.3 kV SiC MOSFET with monolithically-integrated Schottky rectifier.

Trench-Assisted Planar Gate: No-Compromise Technology



	SiC Planar	SiC Trench	GeneSiC SiC MOSFET
	Source Gate Metal P+ P- Well JFET Region N- Drift layer	P+ P- Well N+ Source P- Well N- Drift layer	Gate Metal Gate Metal N+ source P- Well N- Drift layer Drain
Manufacturability	High-yield & low-cost manufacturing	 Complex manufacturing Low-yield & high-cost 	High-yield & low-cost manufacturing
Performance	 Higher R_{DS(ON)} per Die area Slower switching FoM 	 Lower R_{DS(ON)} per Die area Faster switching FoM Worst R_{DS(ON)} vs. temperature 	 Lowest R_{DS(ON)} per Die area Faster switching FoM Stable R_{DS(ON)} vs. temperature
Reliability	Simpler device structure enables excellent reliability	Reliability concerns due to complex device structure	Simpler device structure enables excellent reliability

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- Unclamped inductive switching (UIS) switching measurements were used to investigate avalanche robustness
- The drain current/voltage waveforms at a peak drain current of 30 A
- Drain voltage rises to a maximum of 4,200 V during the test and a maximum avalanche-withstand time (tAV) of 35 μs and single-pulse avalanche energy (EAS) of 2.6 J
- In comparison, the test performed on a discrete 3.3 kV discrete SiC MOSFET with the same loadinductance extracted an EAS of 4.8 J



3.3kV Mono-Integrated SiC MOSFET UIS Testing

- Short-circuit robustness of the GeneSiC MOSFETs was evaluated by subjecting 3.3 kV discrete SiC MOSFETs with and without monolithicallyintegrated MPS diodes to a 1,200V DC link
- +20 V / -5 V gate-drive scheme was used, and the device was mounted on a 25°C baseplate
- The drain current increases to a maximum of 525 A during the short-circuit pulse and a short-circuit withstand time of 4.5 μs was measured







- The Grid requires BESS to support peaking demand and changes in consumer demand
- Deploying SiC in inverters will accelerate the adoption of energy-storage technologies and make them critical elements of future grids
- Integrating a BESS to an MV grid through an isolated topology shows that using 3.3 kV single SIC MOSFETs enables higher system efficiency, lower operating temperature, and smallest die size, compared to an equivalent silicon IGBT or two 1,700V SiC MOSFETs in series
- GeneSiC 3.3 kV SiC MOSFETs with monolithically-integrated monolithic MPS diodes achieve breakdown voltages well above 3.3 kV and demonstrate smooth switching performance while fully activating the monolithic MPS diode
- This significantly reduces power losses in third quadrant operation and enhances device reliability by alleviating bipolar degradation. UIS testing reveals a robust avalanche capability and short circuit withstand times to 4.5us

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