Application Note AN015

New GaNFast™ Power ICs with GaNSense™ Technology
Loss-Less Current Sensing & Autonomous Protection

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Introduction

The latest family of Navitas GaNFast Power ICs with GaNSense technology includes control, drive, sensing and protection features for high density charger and adapter applications. Integrated gate drive eliminates parasitic gate loop inductance and prevents gate ringing and glitching, integrated lossless current sensing eliminates external current sensing resistors to increase system efficiency and reduce PCB footprint, eliminate R_{CS} hot-spots, and real-time over-current (OCP) and over-temperature protection (OTP) circuits provide fast and reliable protection against short-circuit and overload fault conditions.

This application note includes a detailed description of each new GaNSense function, schematics and PCB layout guidelines, in-circuit examples and waveforms, and thermal management instructions. These guidelines are intended to achieve maximum efficiency and power density and to enable the highest level of system robustness and reliability.

Overview

The industry standard NV611x and NV612x GaNFast ICs have been designed into a variety of high-density power supplies due to integrated gate drive, wide range V_{CC} and PWM inputs, internal ESD protection, and large thermal cooling pad. These key features combined with Navitas 700V GaN IC technology enables high-frequency operation with ease-of-use, design flexibility and compatibility with all popular topologies and controllers. To further enhance the GaNFast product family, GaNSense technology has been implemented to provide state-of-the-art loss-less current sensing of the GaN IC, and to provide an additional layer of OCP and OTP protection. Autonomous standby mode is also included to reduce system no load and light-load power losses. The IC pinout of the PQFN 6x8 and 5x6 package versions includes (see Fig. 1) Drain pins (D), Source pins (S), I/O pins, and a large Source cooling pad (PAD). The I/O pins include IC supply pins, PWM input, dV/dt turn-on control, and current sensing output. Most of the switching currents of the external power conversion circuit flow from the Drain pins, through the GaN power FET, and to the Source pins. Heat generated from the GaN IC ***must be*** taken out through the Source cooling pad (PAD) and to the PCB. Large PCB copper areas and thermal vias are then used to transfer the heat to the opposite side of the PCB and/or to inner layers that have large copper planes where it can then be spread and cooled. The cooling pad is conveniently connected to P_{GND} to gain additional PCB thermal copper area.

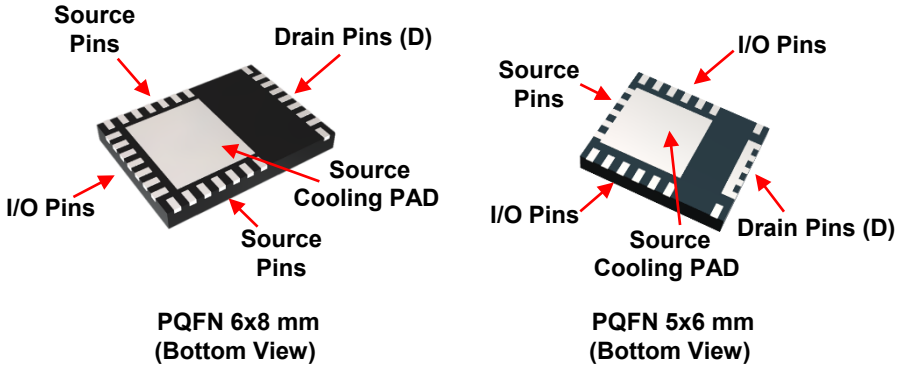


Fig 1. PQFN 6x8 and 5x6 packages and simplified schematic

IC Pins, Connections and Components

The typical connection diagram for this GaN IC is shown in Fig. 2. The IC pins include drain of the GaN IC (D), source of the GaN IC (S), IC supply (V_{CC}), gate drive supply (V_{DD}), gate drive turn-on control SET input (R_{DD}), PWM input (PWM), separate signal GND (S_{GND}), current sensing output (CS), auto-standby mode input ($\overline{STBY}$) and 5V supply (5V). The Source pad and Source pins (S) should all be connected to the system P_{GND}. S_{GND} pin 4 must be connected directly to Source PAD underneath IC. The Source pins (S) should each be connected externally to the Source pad directly underneath the IC. The Drain Pins (D) should all be connected together in the layout (see Section 9). The external components around the IC include V_{CC} filter capacitor (C_{VCC}) connected between V_{CC} pin and S_{GND} pin, V_{DD} filter capacitor (C_{VDD}) connected between V_{DD} pin and S_{GND} pin, turn-on dV/dt set resistor (R_{DD}) connected between V_{DD} pin and R_{DD} pin, current-sense amplitude-set resistor (R_{SET}) connected between CS pin and S_{GND}, and auto-standby mode pin ($\overline{STBY}$) connected to S_{GND}. An external capacitor (C_{5V}, 0.01uF max) is required between pin 5V and S_{GND}. This 5V pin is for internal purposes only and must not be used for biasing external circuitry. The table below (Table I) shows the recommended component values (typical only) for the external components connected to the pins of this GaN IC. These components should be placed as close as possible to the IC.

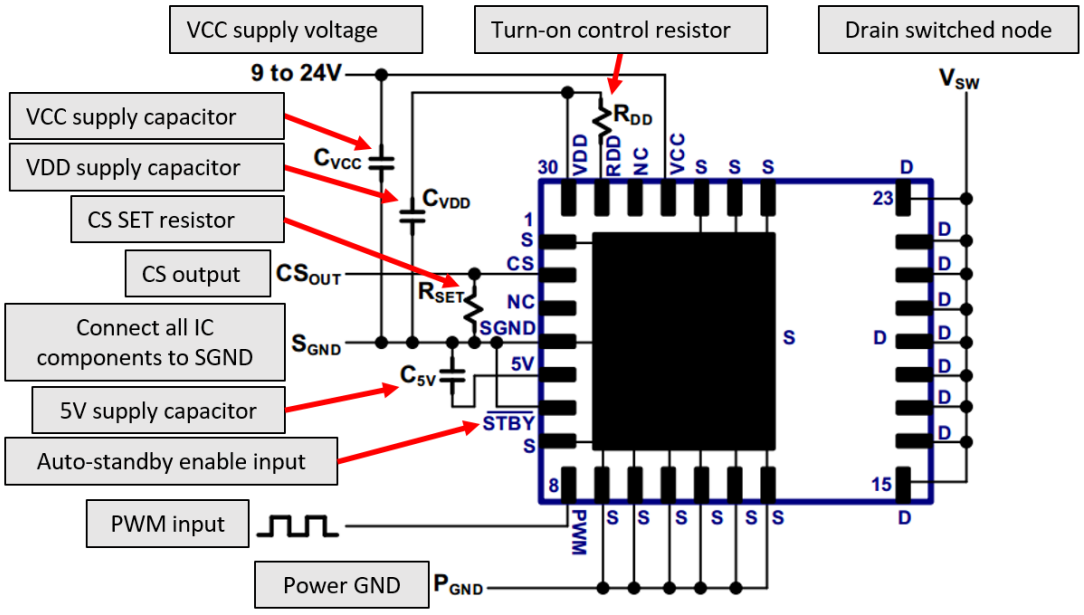


Fig 2. GaN IC connection diagram

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} supply capacitor	0.1	µF
C_{VDD}	V_{DD} supply capacitor	0.010	µF
R_{DD}	Gate drive turn-on current set resistor	50	Ω
R_{SET}	Current sense amplitude set resistor	Depends on system design (See Eq. 1, Page 4)	Ω
C_{5V}	5V supply capacitor	0.01	µF

Table I. Recommended component values (typical only)

Loss-Less Current Sensing

For many applications it is necessary to sense the cycle-by-cycle current flowing through the GaN IC. Existing current sensing solutions include placing a series current sensing resistor in between the Source connection of the power FET and P_{GND}. Using external current sensing resistors increases system conduction power losses, creates a hot-spot on the PCB, and lowers overall system efficiency. To eliminate external resistors and hot-spot, and increase system efficiency, this GaN IC integrates accurate and programmable loss-less current sensing. The I_{DS} current flowing through the GaN IC is sensed internally (Fig. 4) and then amplified, trimmed and converted to a current at the current sensing output pin (CS). An external resistor (R_{SET}) is connected from the CS pin to the S_{GND} pin and is used to set the amplitude of the CS pin voltage signal. This allows for the CS pin signal to be programmed to work with different controllers with different current sensing input thresholds.

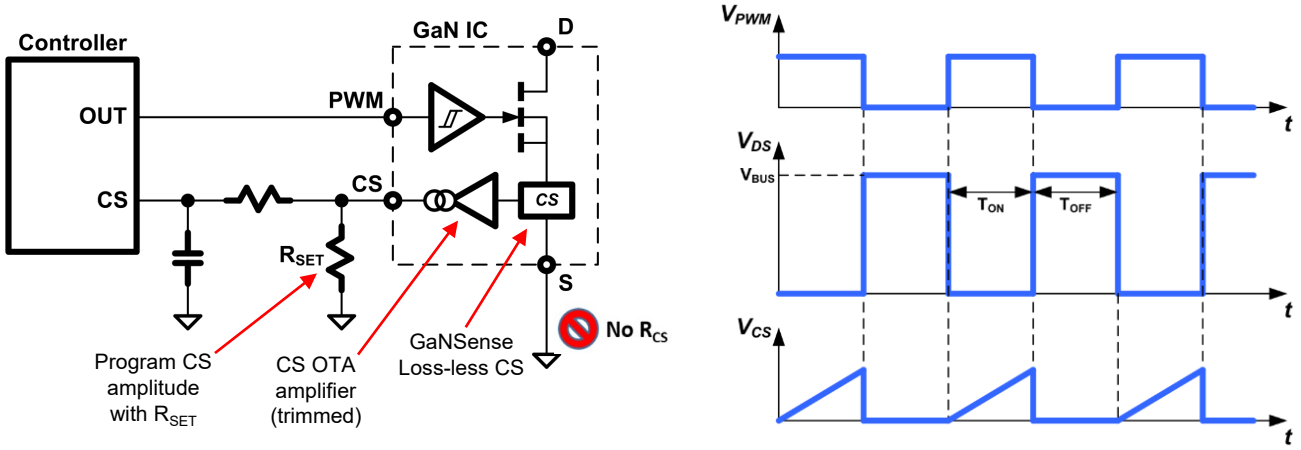


Fig 4. Loss-less current sensing circuit and timing diagram

The overall accuracy of the internal current sensing circuit depends on the trimming results of the CS output current at final test during production. The post trimming production data (Fig. 5) shows a tight distribution (+/- 1.4%, +/- 3σ, 70ku) and highlights the high accuracy of the internal GaNSense and amplifier circuits. The CS pin current versus temperature graph illustrates the normal positive temperature coefficient behavior of the internal circuit and has +/- 4% tolerance from -40 to 125C.

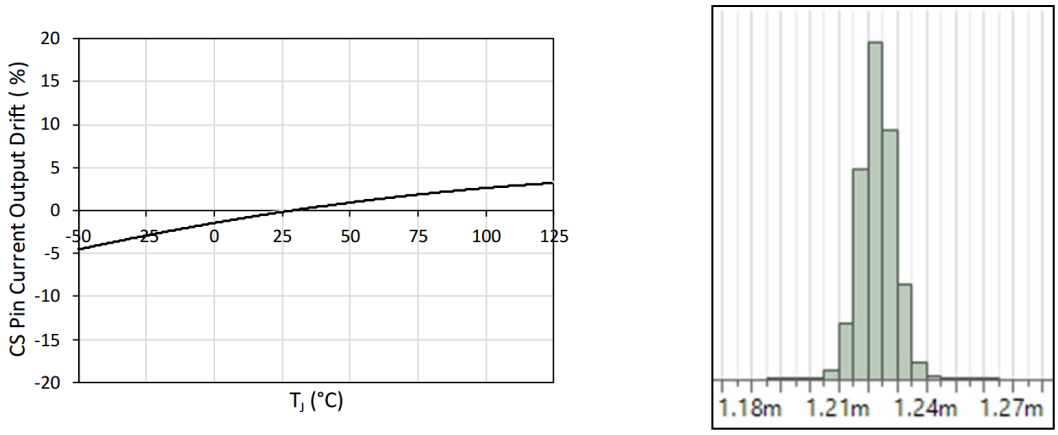


Fig 5. CS pin current vs Tcase and post-trim production data (NV6136A)

Loss-Less Current Sensing (cont.)

When comparing GaNSense technology versus an existing external resistor sensing method (Fig. 6), the total ON resistance, RON(TOT), can be substantially reduced. For a 65W high-frequency QR flyback circuit, for example, RON(TOT) is reduced from 340 mΩ to 170 mΩ. The power loss savings by eliminating the external resistor results in a +0.5% efficiency benefit for the overall system.

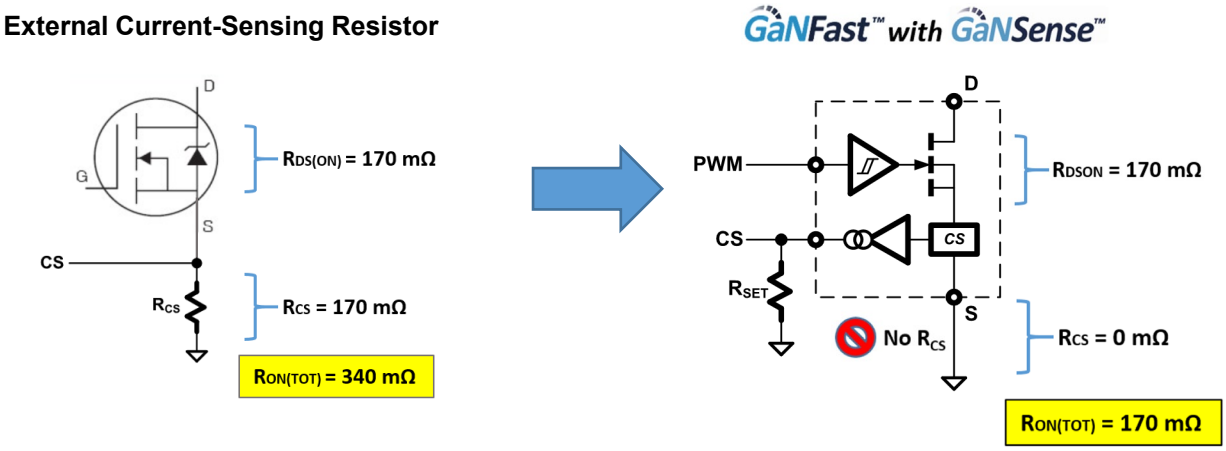


Fig 6. External resistor sensing vs. GaNSense technology

To select the correct R_{SET} resistor value, the following equation (Equation 1) can be used. This equation uses the equivalent desired external current sensing resistor value (R_{CS}), together with the gain of the internal sensing circuitry, to generate the equivalent R_{SET} resistor value. This R_{SET} value will then give the correct voltage level at the CS pin to be compatible with the internal current sensing threshold of the system controller.

$$I_{OUT}\ Ratio = \frac{I_{DS}}{I_{CS}} = \frac{4.4A}{0.00125A} = 3520$$

$$R_{SET} = 3520 * R_{CS}$$

$$3520 * 170m\Omega = 598.4\Omega$$

Equation 1. R_{SET} resistor value equation (NV6136A)

Loss-Less Current Sensing (cont.)

During application testing, the switching waveforms (Fig. 7) show the tracking comparison between the CS pin output voltage and the actual I_{DS} current of the GaN IC. The 65 W HFQR waveforms (Fig. 7a) show the CS pin tracking performance during ZVS/ZCS conditions. The boost circuit waveforms (Fig. 7b) show the CS pin voltage during CCM conditions. Both switching conditions show acceptable real-time tracking performance. To show tracking accuracy, the CS pin voltage scale for all waveforms is based on RCS gain calculation to match current probe scale.

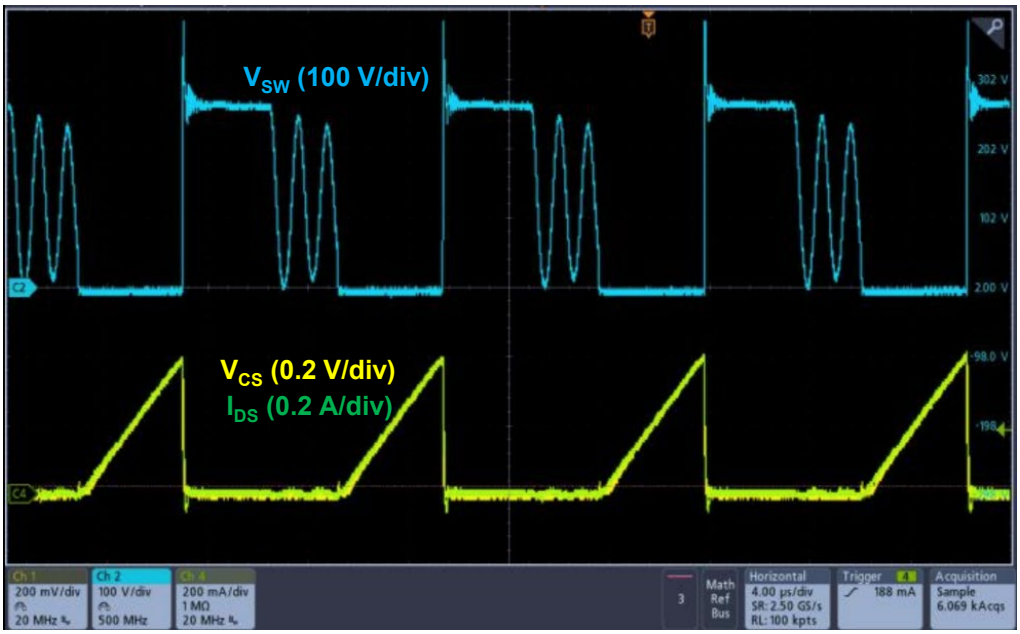


Fig 7a. Loss-less current-sensing waveforms
(65 W HFQR, 115 V_{AC} / 20 V / 3.25 A, 192 kHz)

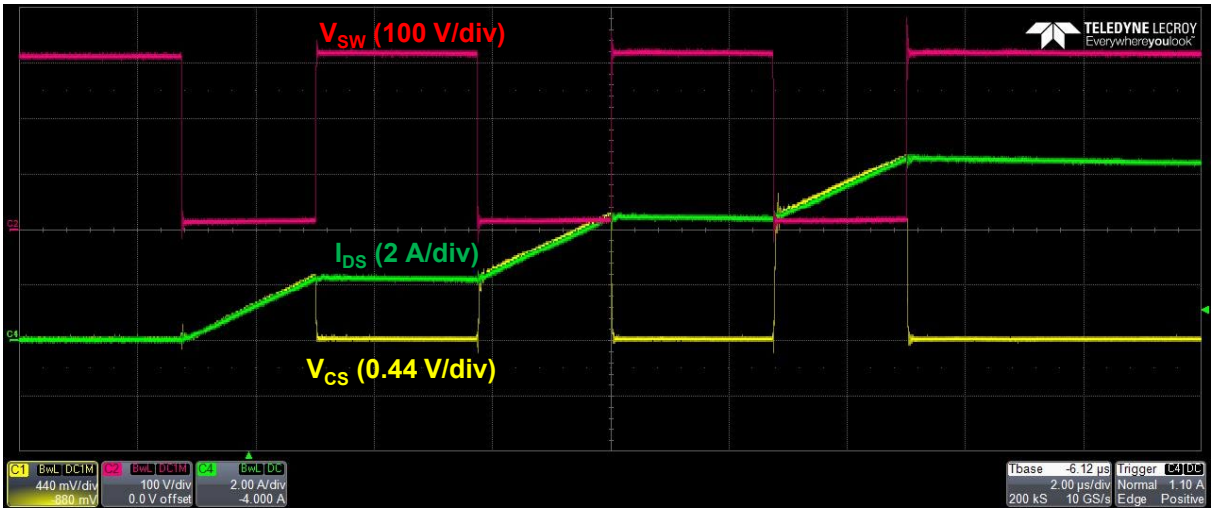


Fig 7b. Loss-less current-sensing waveforms
(Boost CCM, 200 kHz)

Loss-Less Current Sensing (cont.)

The NV6136A and NV6134A with GaNSense technology were compared versus NV6125 with external current-sensing resistor (Fig. 8). The NV6136A (Fig. 8a, 170 mΩ) shows +0.5% higher efficiency during low-line full load conditions due to lower $R_{ON(TOT)}$, and also shows R_{CS} hot-spot removal and GaN IC temperature reduction by 12 ℃. The NV6134A (Fig. 8b, 260 mΩ) shows similar efficiency and similar GaN IC temperatures. The NV6134A offers a higher $R_{DS(ON)}$ / lower cost option if higher efficiency is not required by the application.

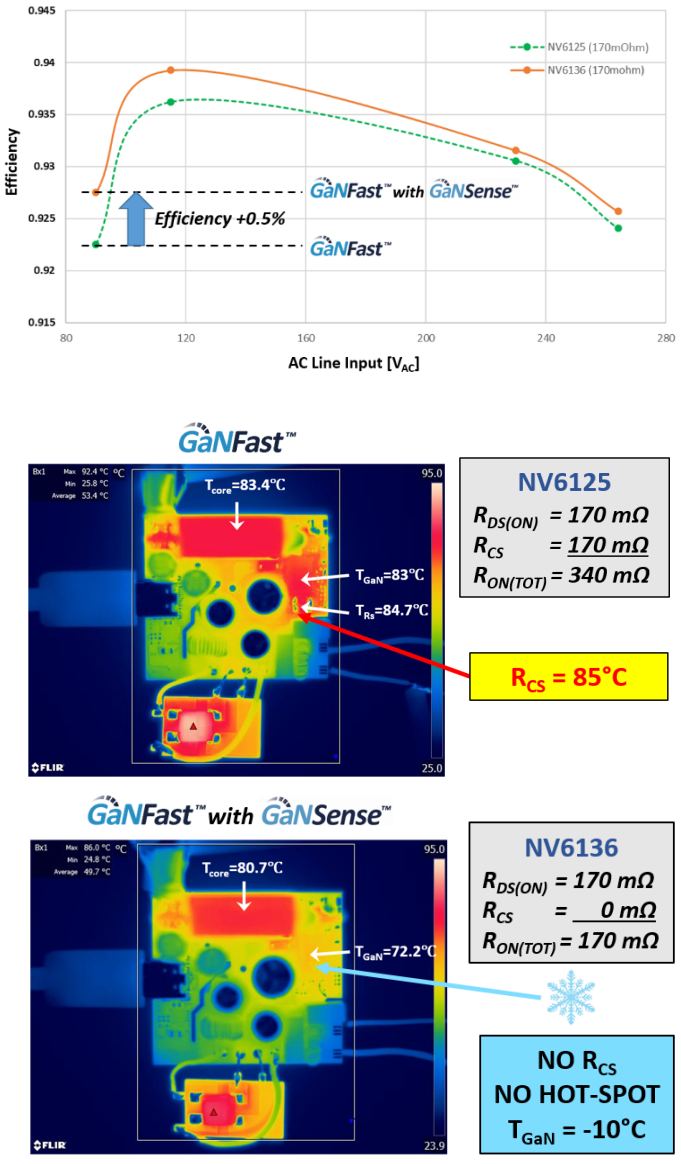


Fig 8a. Loss-less current sensing (NV6136A, 170 mΩ, higher efficiency option)

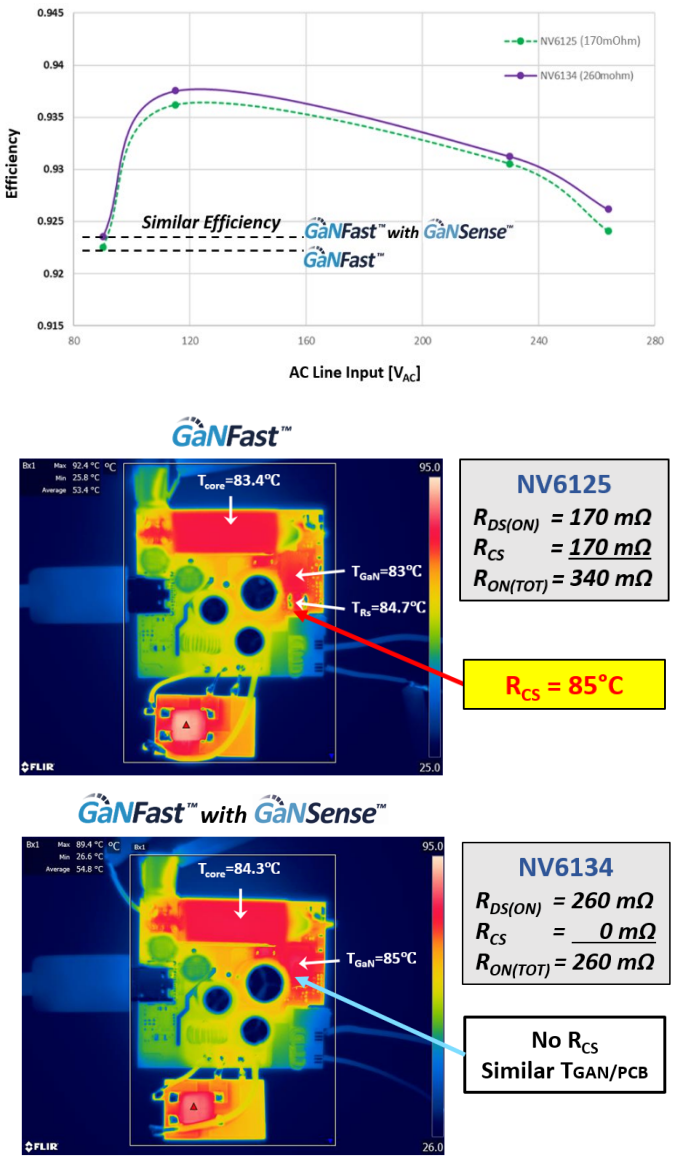


Fig 8b. Loss-less current sensing (NV6134A, 260 mΩ, similar efficiency / higher $R_{DS(ON)}$ option)

Over Current Protection (OCP)

This GaN IC includes cycle-by-cycle over-current detection and protection (OCP) circuitry to protect the GaN IC against high current levels. During the on-time of each switching cycle, should the peak current exceed the internal OCP threshold (1.9 V, typical), then the internal gate drive will turn the GaN IC off quickly and truncate the on-time period to prevent damage from occurring to the IC. The IC will then turn on again at the next PWM rising edge at the start of the next on-time period (Fig. 8). This OCP protection feature will self-protect the IC each switching cycle against fast peak over current events and greatly increase the robustness and reliability of the system. The actual peak current threshold can be calculated using Equation 2 and is a function of the internal current-sensing ratio and the external R_{SET} resistor. The internal OCP threshold (1.9 V, typical) is much higher than the OCP thresholds of many popular QR, AHB and PFC controllers. This ensures good compatibility of this IC with existing controllers without OCP threshold conflicts. Fig. 9 shows actual OCP waveforms limiting the peak current cycle-by-cycle during inductive switching.

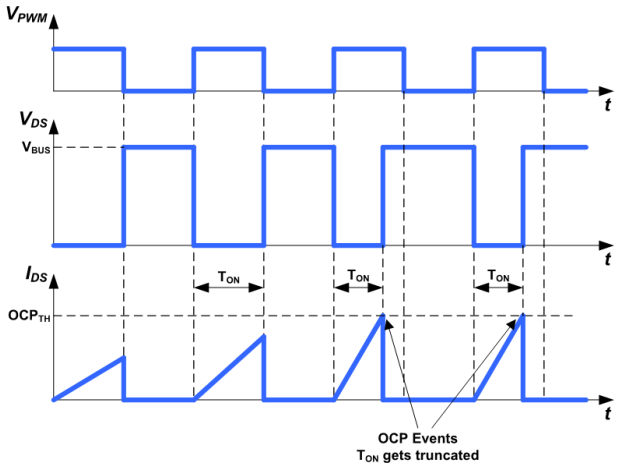


Fig 8. OCP timing diagram

$$I_{OCP} = \frac{[\,1.9\ \text{V} \times 3520\,]}{R_{SET}}$$

Equation 2. OCP current threshold equation (NV6136A)

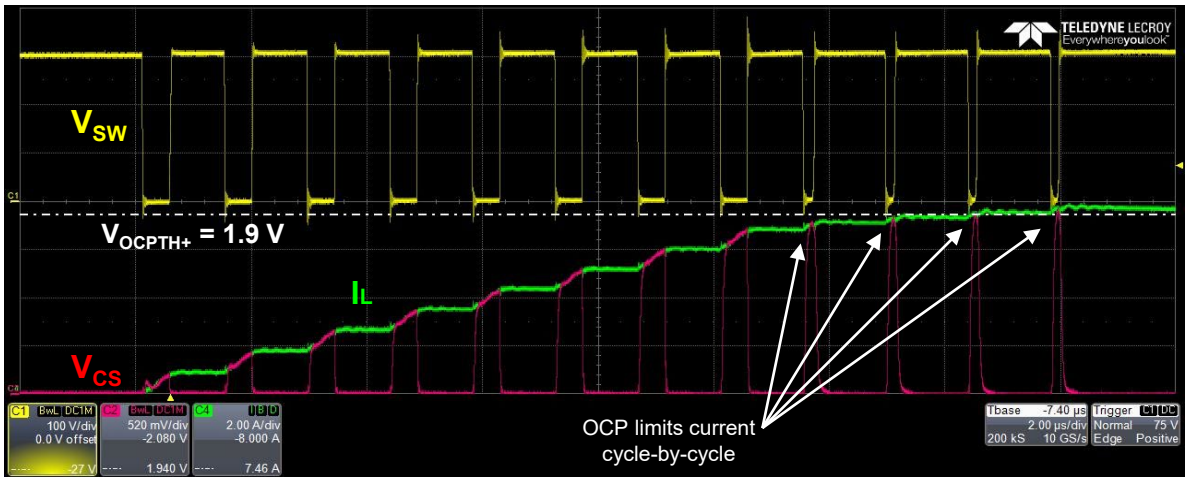


Fig 9. Over-current cycle-by-cycle limitation during boost CCM

Over-Temperature Protection (OTP)

This GaN IC includes over-temperature detection and protection (OTP) circuitry to protect the IC against excessively high junction temperatures (T_J). High junction temperatures can occur due to overload, high ambient temperatures, and/or poor thermal management. Should T_J exceed the internal T_{OTP+} threshold (165 ºC, typical) then the IC will latch off safely. When T_J decreases again and falls below the internal T_{OTP-} threshold (105 ºC, typical), then the OTP latch will be reset. Until then, internal OTP latch is guaranteed to remain in the correct state while V_{CC} is greater than 5 V. During an OTP event, this GaN IC will latch off and the system V_{CC} supply voltage will decrease due to the loss of the aux winding supply. The system V_{CC} will fall below the lower UV- threshold of the controller and the high-voltage start-up circuit will turn-on and V_{CC} will increase again (Fig. 10). V_{CC} will increase above the rising UV+ threshold and the controller turn on and deliver PWM pulses again.

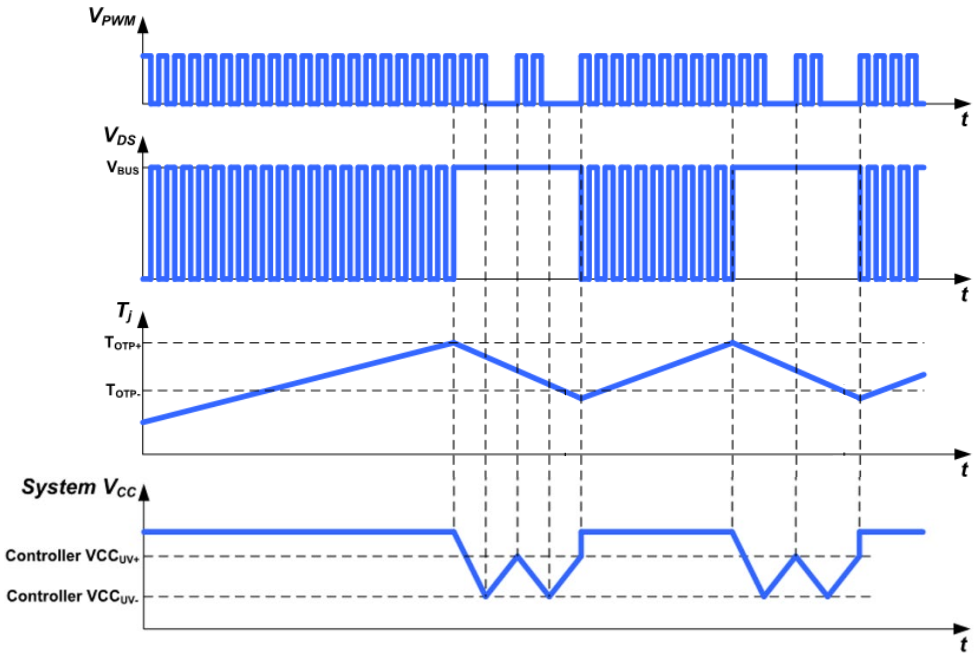


Fig 10. OTP timing diagram

Programmable Turn-on dV/dt Control

During first start-up pulses or during hard-switching conditions, it is desirable to limit the slew rate (dV/dt) of the drain of the GaN IC during turn-on. This is necessary to reduce EMI or reduce circuit switching noise. To program the turn-on dV/dt rate of the GaN IC, a resistor (R_{DD}) is placed between the V_{DD} pin 30 and the R_{DD} pin 29 (see Fig. 2). This resistor (R_{DD}) sets the turn-on current of the internal gate driver and therefore sets the turn-on falling edge dV/dt rate of the drain of the power FET (Fig. 11). The actual V_{DS} waveforms for different R_{DD} values are also shown (Fig. 12).

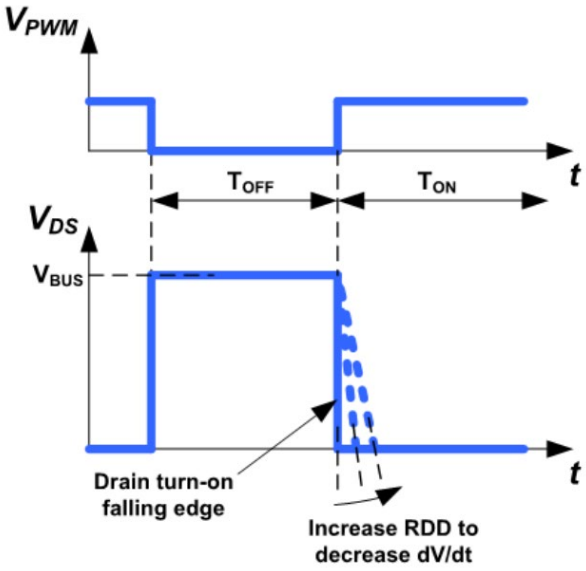


Fig 11. Turn-on dV/dt slew rate control simplified timing diagram

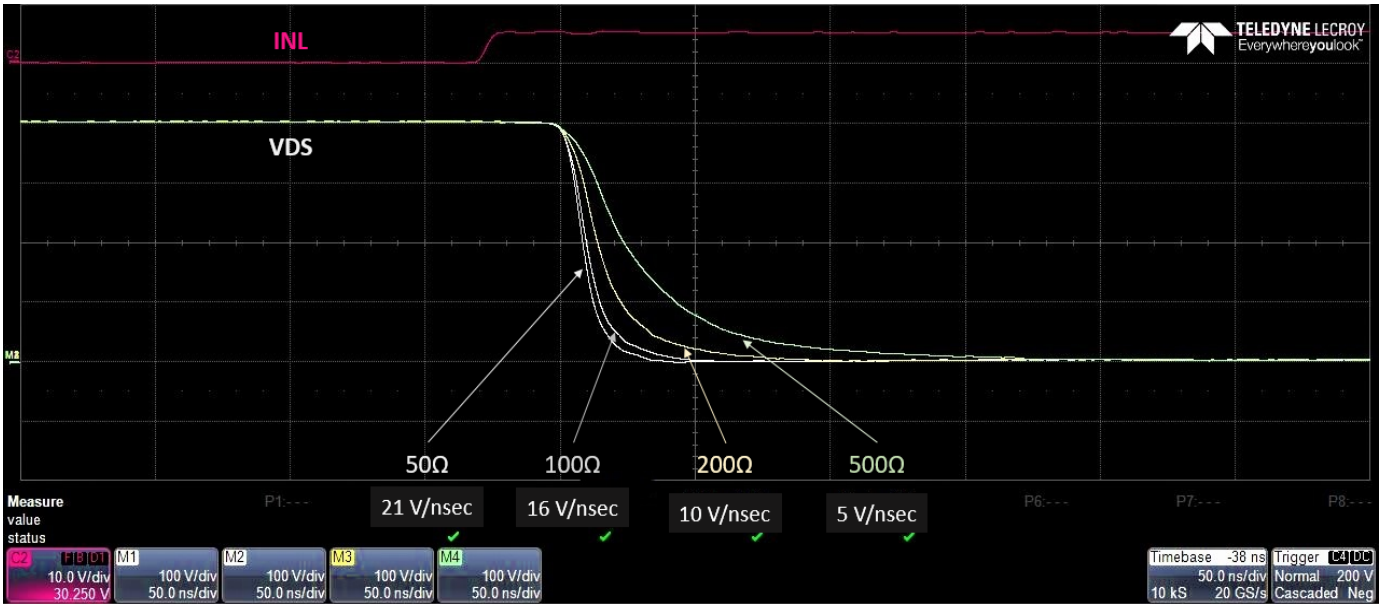


Fig 12. V_{DS} turn-on slew rate (dV/dt) waveforms for different R_{DD} values (NV6136A, 90%-10%)

Autonomous Low-Power Standby Mode

This GaN IC includes an autonomous low-power standby mode for disabling the IC and reducing the V_{CC} current consumption. During normal operating mode, the PWM pin toggles high and low to turn the GaN IC on and off. If the input pulses at the PWM pin stop and stay below the lower V_{PWML} turn-off threshold (1.1V, typical) for the duration of the internal timeout standby delay (t_{TO_STBY}, 90 us, typical), then the IC will automatically enter low power standby mode (Fig. 13). This will disable the gate drive and other internal circuitry and reduce the V_{CC} supply current to a low level (275 uA, typical). When the PWM pulses restart, the IC will wake up at the first rising edge of the PWM input and enter normal operating mode again. To enable autonomous standby mode, the auto-standby mode pin 6 ($\overline{STBY}$) should always be connected to S_{GND} pin 4 (set low). To disable autonomous standby mode, $\overline{STBY}$ pin 6 should be connected to the 5 V pin 5 (set high).

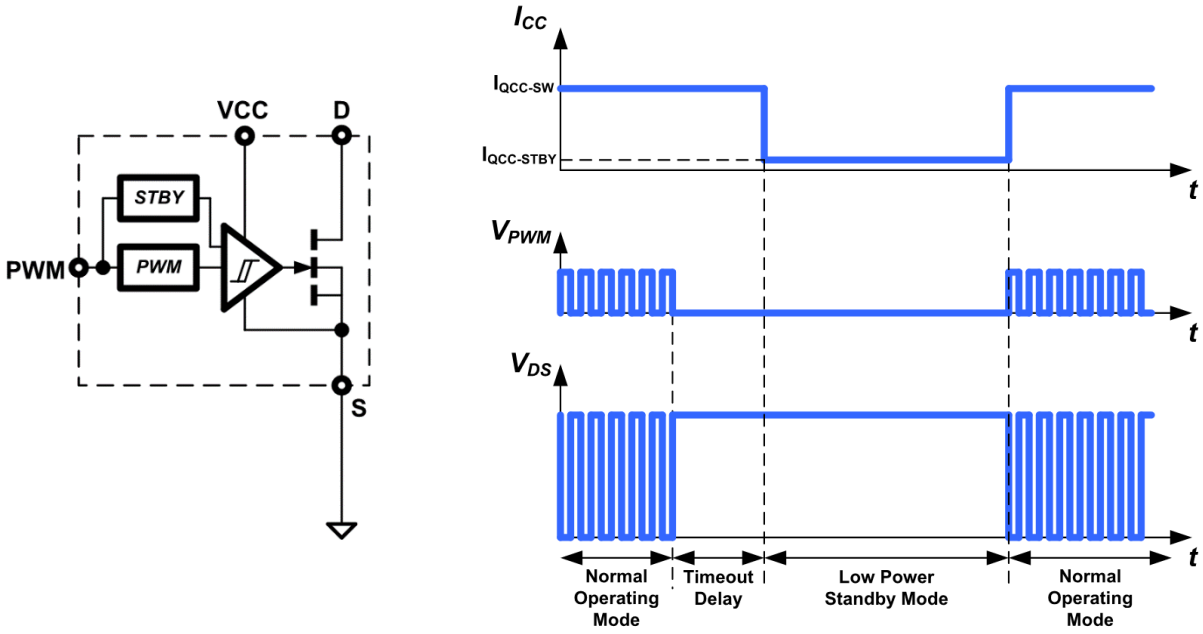
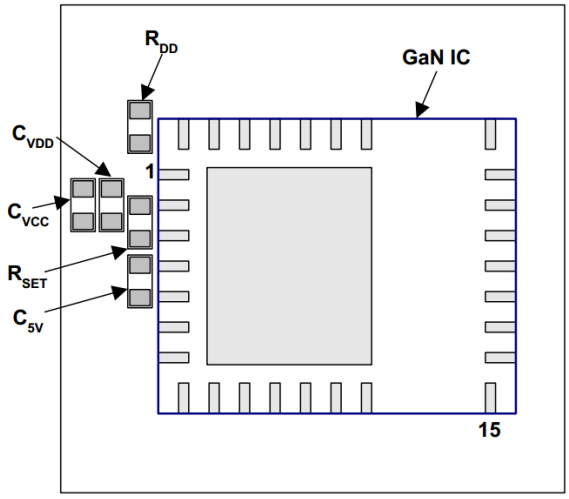


Fig 13. Autonomous low-power standby mode simplified circuit and timing diagram

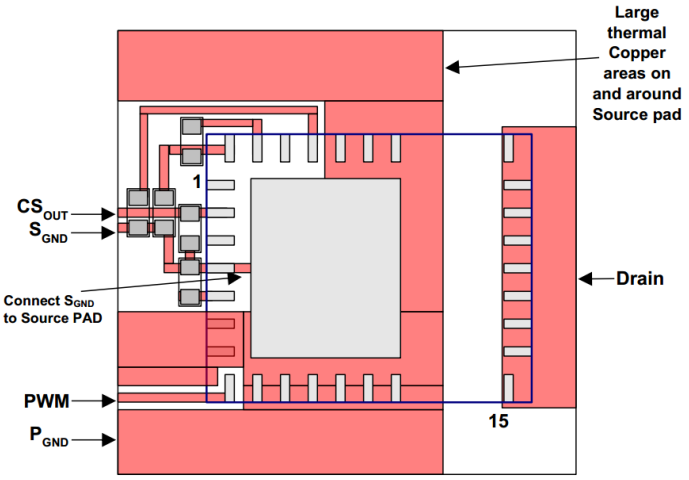
PCB Layout Guidelines (QFN 6x8)

For best electrical and thermal results, these PCB layout guidelines (and 4 steps below, Fig. 14) must be followed:

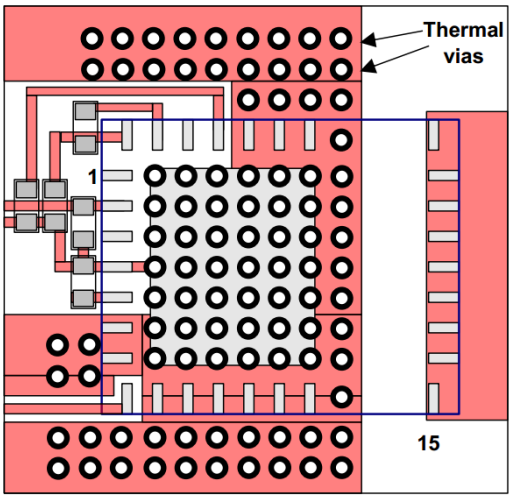
1) **Place IC components as close as possible to the GaN IC**. Place R_{SET} resistor directly next to CS pin to minimize high frequency switching noise.
2) Connect the ground of IC components to S_{GND} pin4 to minimize high frequency switching noise. Connect S_{GND} pin4 directly to Source PAD underneath the IC.
3) Route all connections on single layer without vias. This allows for large thermal copper areas on other layers.
4) Place large copper areas on and around Source pad.
5) Place many thermal vias inside Source pad and inside source copper areas.
6) Place large as possible copper areas on all other layers (bottom, top, mid1, mid2).



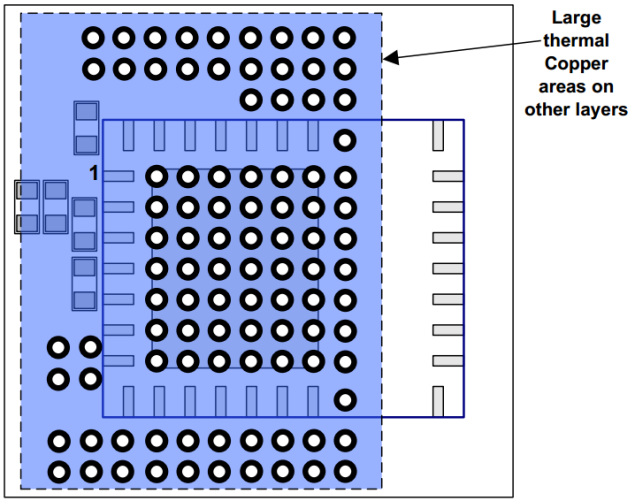
(a) Place GaN IC and SMD components on top layer



(b) Route Drain pins, Source pins, Source PAD, SMD components, and place large copper areas on top layer



(c) Place thermal vias inside cooling pad and sides



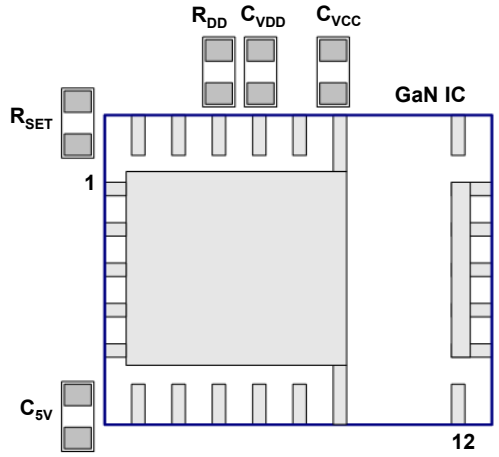
(d) Place large copper areas on bottom and mid layers

Fig 14. PCB layout steps

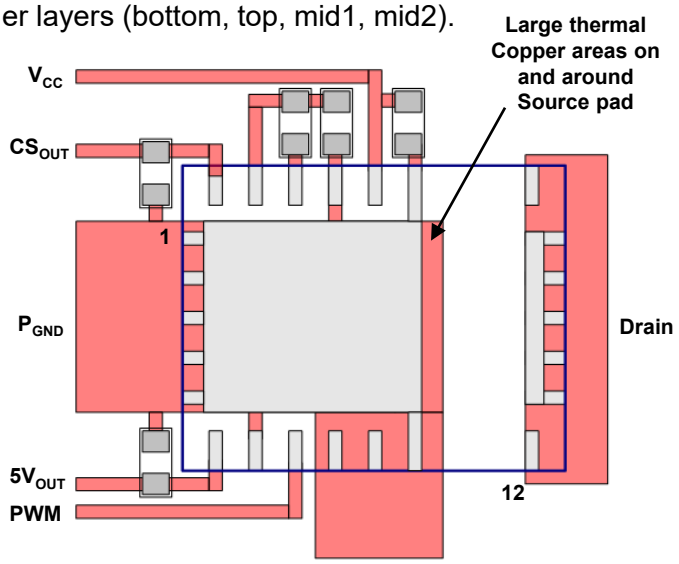
PCB Layout Guidelines (QFN 5x6)

For best electrical and thermal results, these PCB layout guidelines (and 4 steps below, Fig. 15) must be followed:

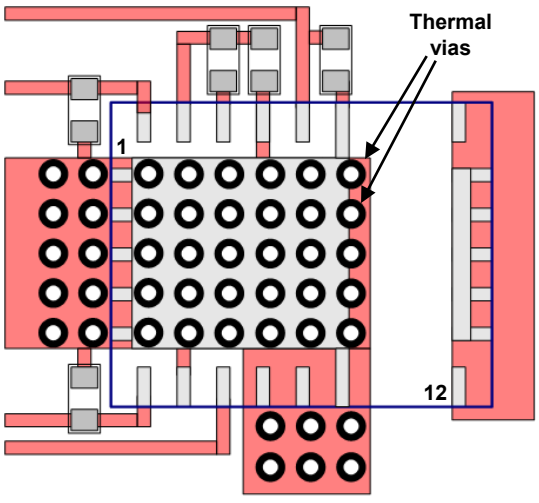
1) **Place IC components as close as possible to the GaN IC**. Place R_{SET} resistor directly next to CS pin to minimize high frequency switching noise.
2) Connect the ground of IC components directly to Source (S) to minimize high frequency switching noise.
3) Route all connections on single layer. This allows for large thermal copper areas on other layers.
4) Place large copper areas on and around Source pad.
5) Place many thermal vias inside Source pad and inside source copper areas.
6) Place large as possible copper areas on all other layers (bottom, top, mid1, mid2).



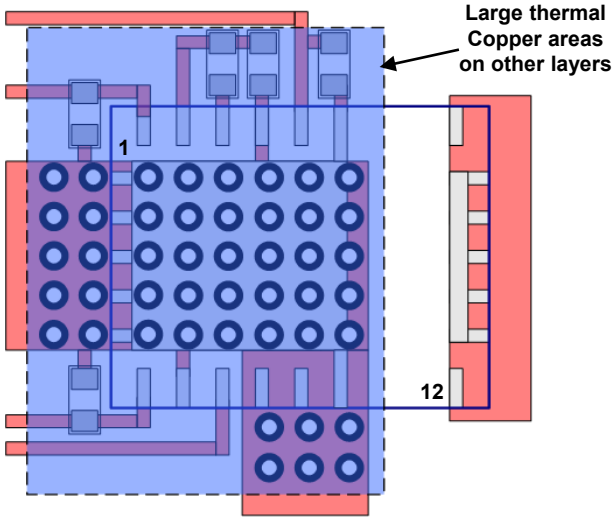
Step 1. Place GaN IC and components on PCB.
Place components as close as possible to IC!



Step 2. Route all connections on single layer.
Make large copper areas on and around Source pad!



Step 3. Place many thermal vias inside source pad and inside source copper areas.
(dia=0.65mm, hole=0.33mm, pitch=0.925mm, via wall=1mil)

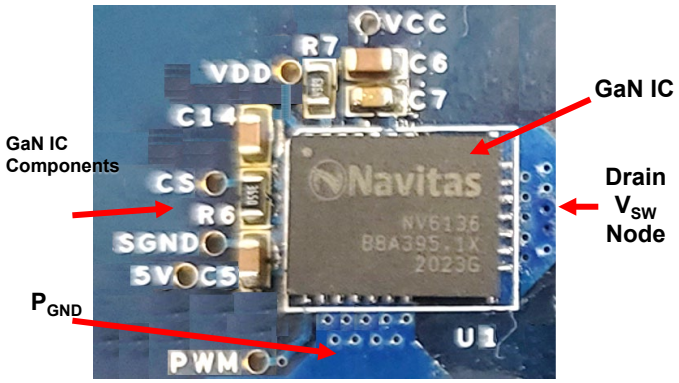


Step 4. Place large copper areas on other layers.
Make all thermal copper areas as large as possible!

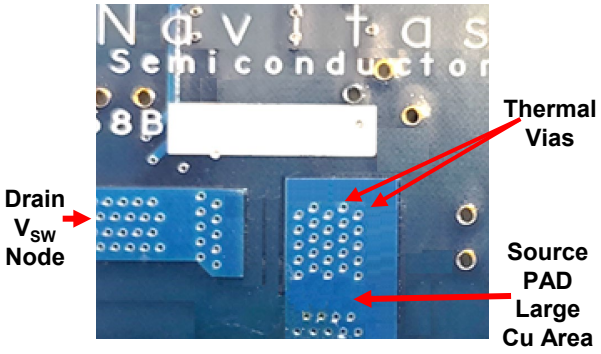
Fig 15. PCB layout steps

PCB Layout Example

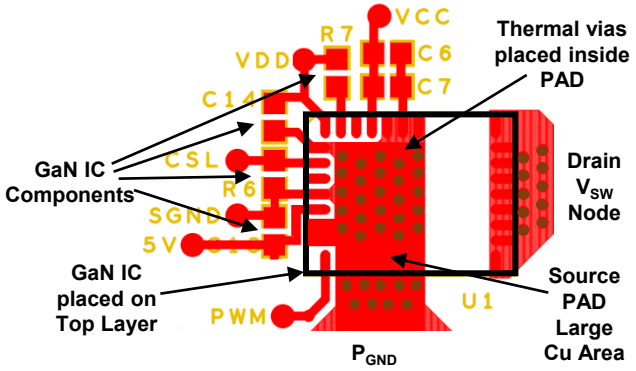
The following example (Fig. 16) shows actual PCB test board example of proper layout practices for QFN 6x8 mm version. All components are placed and routed on the top layer allowing all other layers to be used for large copper area and thermal vias. If 4-layer PCB is used, then additional thermal copper area can be gained.



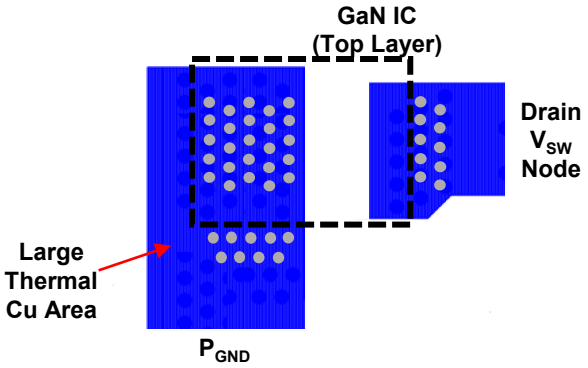
(a) Top-side PCB



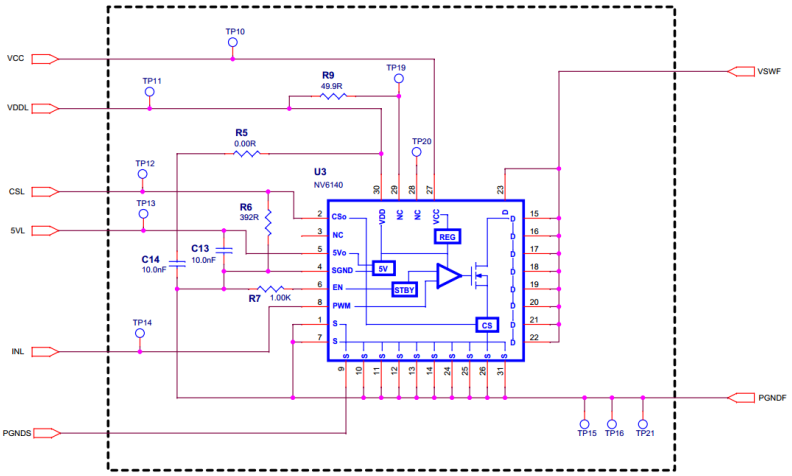
(b) Bottom-side PCB



(c) Top-layer layout



(d) Bottom-layer layout (mirrored)



(e) Circuit schematic

Fig 16. PCB and layout example for GaN IC.

(a) Top-side PCB, (b) Bottom-side PCB, (c) Top layout, (d) Bottom/Mid layout, (e) Circuit schematic

Thermal Management

The following thermal model (Fig. 17) is for a typical application where the heat from the GaN IC flows up from the top of the QFN 6x8 package through the thermal interface material (TIM), as well as laterally through the PCB to the sides (and up through the TIM). The TIM then goes to the insulating material (Mylar) and then to a Cu shield. To represent the actual thermal conditions inside a 65W charger running at full load, the Cu shield is held at 85°C, the T_{AMB} is set at 80 °C, and P_{LOSS} for the GaN IC is set at 0.6 W. Mylar is also placed at the bottom of the PCB and set at 85 °C, to simulate other hot components that may be located on the bottom side of the PCB (i.e. XFMR). From the thermal simulation (Fig. 18), the T_J of the GaN IC reaches approx. 104°C. This result looks reasonable for the GaN IC running during worst case line, load and ambient temperature conditions. Further improvement of the GaN IC temperature is possible by using TIM with higher conductivity and by using thinner Mylar (if safety conditions allow).

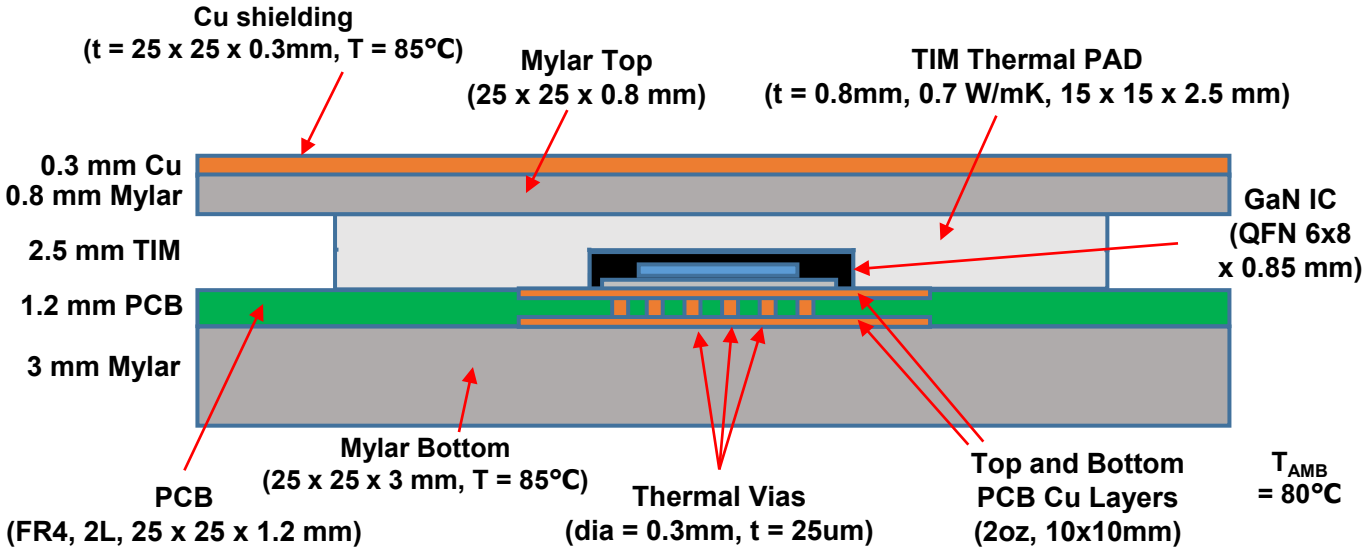


Fig 17. Thermal model for lateral and vertical heat conduction

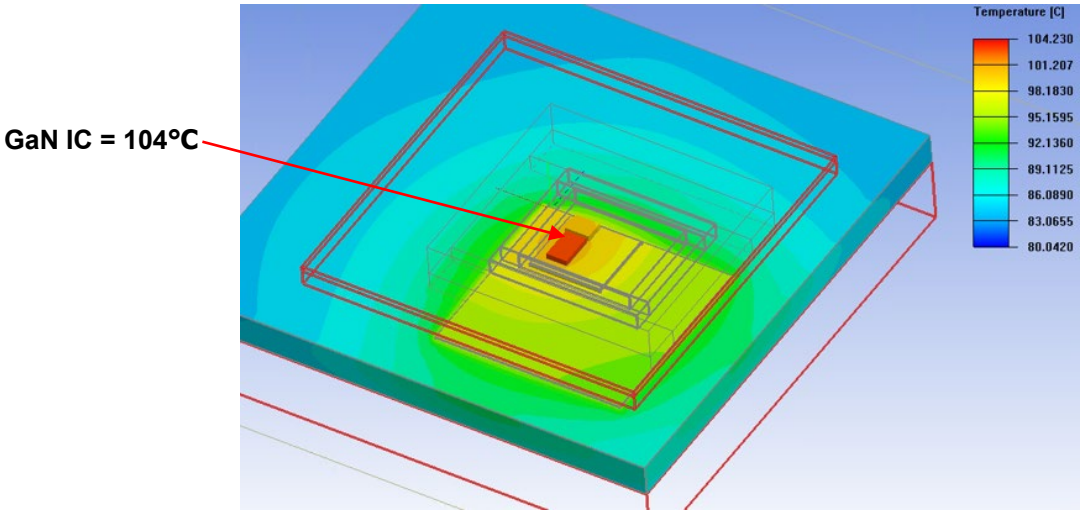
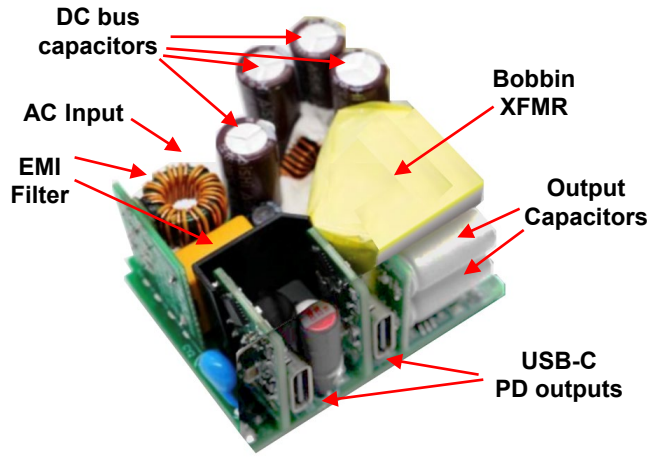


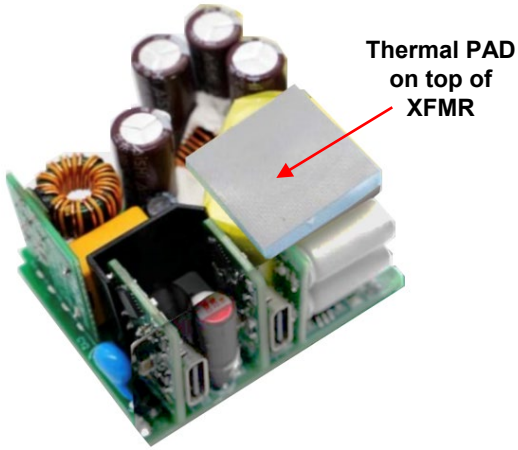
Fig 18. Thermal simulation for lateral and up heat conduction model.
(P_{LOSS_GaN} = 0.6 W, T_{AMB} = 80°C)

High Density 65W-2C Charger (65cc) Example

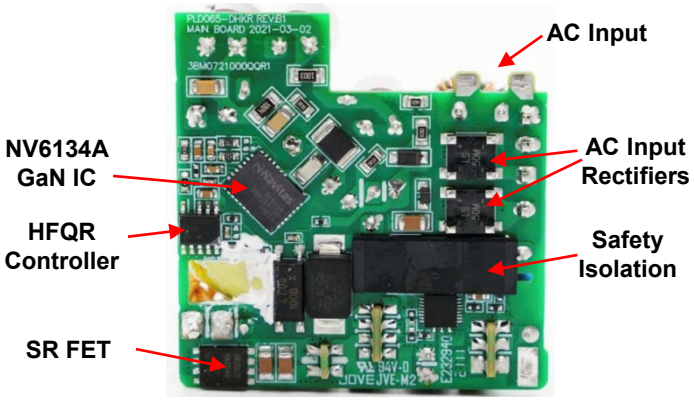
The following example (Fig. 19) demonstrates the construction details of a typical 65 W HFQR USB-C PD charger product. This multi-daughtercard design uses thermal pads placed on top of the power components, followed by safety insulation and an aluminum shield for heat spreading and EMI reduction.



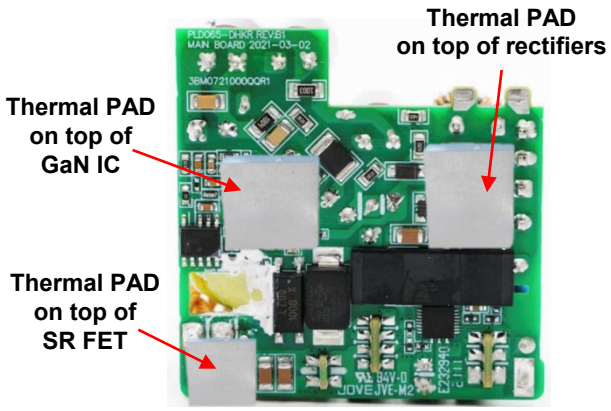
(a) 65 W charger top-side PCBA



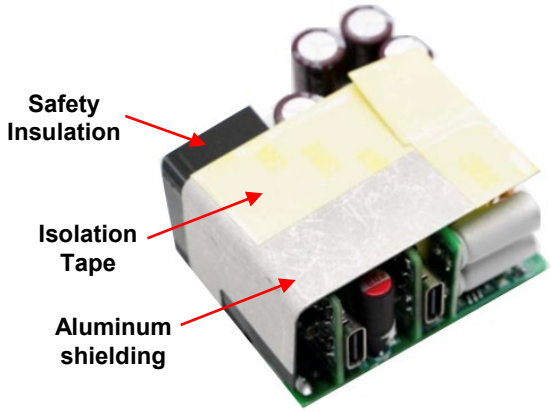
(b) Place thermal PAD on top of XFMR



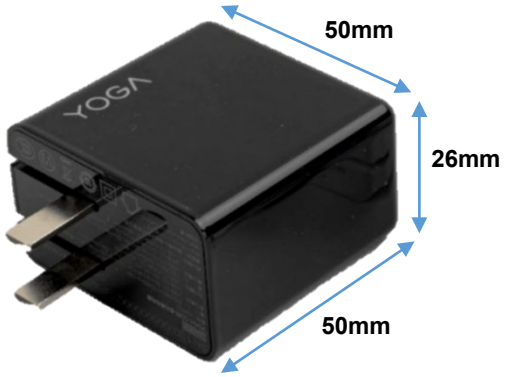
(c) 65 W charger bottom-side PCBA



(d) Place thermal PAD on top of GaN IC & rectifiers



(e) Add safety insulation & Aluminum shield with isolating tape



(f) Add foldable AC plug and plastic case (65 cc)

Fig 19. 65 W 2C USB-C PD charger construction details

References (www.navitassemi.com)

1) GaNFast NV6123, NV6125, NV6127 datasheets, Navitas Semiconductor, 2019
2) Thermal Management of GaNFast Power ICs, AN010, Navitas Semiconductor, 2019
3) GaNFast NV613x/NV615x Power ICs with GaNSense Technology datasheets, Navitas Semiconductor, 2021

Additional Information

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