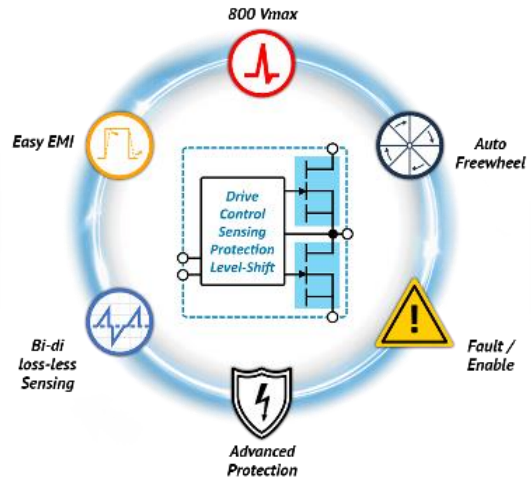
Navitas

Application Note AN025

New GaNSense™ Motor Drive ICs

Tom Ribarich, Sr. Director Strategic Marketing



Introduction

NV6257/87/88 GaNSense Motor Drive ICs includes two GaN power FETs and drivers, plus control, level-shifting, sensing and protection features for 400-600 W motor drive applications. Comprehensive integration delivers specific motor drive functions, high reliability, high efficiency and density, and creates an easy-to-use motor inverter building block.

Benefits of Integration

- **Reliability:** No gate ringing and glitching due to monolithic integration of GaN FET and GaN driver (no parasitic gate-loop inductance). Real-time short-current (SCP) and over-temperature protection (OTP) deliver fast and reliable protection against short-circuit and overload fault conditions, plus wide-range V_{CC}, 2 kV ESD protection, shoot-through protection, and UVLO functions are also included.
- **Efficiency:** Loss-less bi-directional current-sensing eliminates external shunt resistors to increase system efficiency, reduce PCB footprint, and eliminate hot-spots. Thermally-enhanced 6x8 mm and 8x10 mm PQFN packages with dual large cooling-pads enables a small PCB footprint with excellent cooling and no heatsinks. Auto SR mode reduces free-wheeling losses, and auto-standby mode reduces off-state losses.
- **Easy-to-use:** Independent, low-side-referenced PWM inputs feed an integrated level-shifter and bootstrap for isolated, high- and low-side half-bridge switching. Adjustable Ton/off slew-rate control enables easy EMI compliance, 40% fewer external components and PCB area than discrete designs, and standard QFN packages enable shorter design-times and maximize chance of first-time-right.

Applications Overview

GaNSense Motor Drive ICs enable robust hard-switching performance and include rich motor-specific features to increase inverter efficiency, reduce component count, and eliminate heatsinks in motor drive applications. The product family (Figure 1) includes power level coverage of 400 to 600W for 3-ph motor drive applications such as air-conditioners, heat pumps, washing machines, dryers, dishwashers, refrigerators, hair dryers, circulator pumps, and fans.

This application note includes a detailed description of the IC features and functions, schematics and PCB layout guidelines, in-circuit examples and waveforms, and electrical model simulation results.

PQFN 6x8

Part #	Pkg	RDSon (Typ mΩ)	Power	Application
NV6257	PQFN 6x8	170	400W	1-ph/3-ph Motor
NV6287	PQFN 8x10	170	500W	1-ph/3-ph Motor
NV6288	PQFN 8x10	120	600W	1-ph/3-ph Motor

Fig 1. GaNSense Motor Drive IC family and power levels

Package & IC Connections

The IC integrates a complete half-bridge power-train together with level-shifting, bootstrap, two low-side GND-referenced PWM inputs, and low-side loss-less bi-directional current-sensing. The IC pinout (see Fig. 2) includes high-voltage DC-bus input and high-side GaN power FET drain connection (V_{IN}), high-side GaN power FET source pad and low-side GaN power FET drain connection (V_{SW}), high-side I/O pins, low-side GaN power FET source pad (P_{GND}) and low-side I/O pins. High-side I/O pins include the high-side IC supply pins, and low-side I/O pins include PWM inputs, dV/dt turn-on control, and current-sensing output. The complementary switching currents of the external power-conversion circuit flow through the drain-to-source of both GaN power FETs. Heat generated from GaN power FETs is removed through both source cooling pads at the bottom side of QFN package to the PCB. Large PCB copper areas and thermal vias are then used to transfer the heat to the opposite side of the PCB and/or to inner layers that have large copper planes where it can then be spread and cooled. The low-side cooling pad is conveniently connected to P_{GND} to gain additional PCB thermal copper area. The low-side source pad and I/O pins are separated from the high-side source pad and I/O pins by a sufficient high-voltage creepage distance.

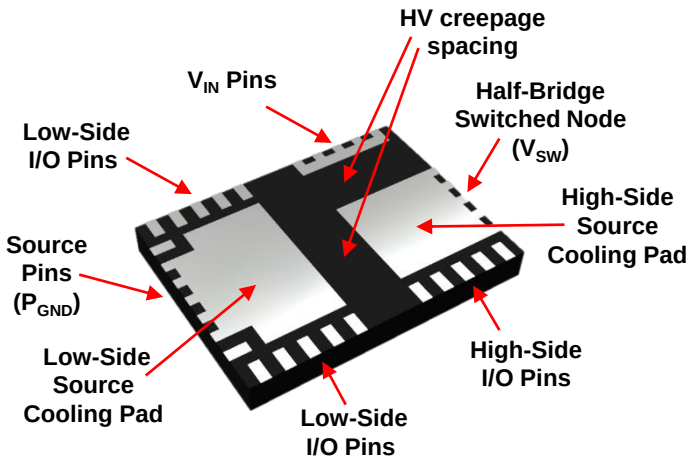


Fig 2. GaNSense Motor Drive IC PQFN 6x8 package highlights (bottom view)

The typical connection diagram for the IC is shown in Figure 3. The IC pins include the drain of the high-side GaN power FET (V_{IN}), the half-bridge mid-point switched node (V_{SW}), the source of the low-side GaN power FET and IC GND (P_{GND}), low-side IC supply (V_{CC}), low-side turn-on/off dV/dt control ($R_{DDL,SSL}$), low-side referenced PWM inputs (IN_L, IN_H), low-side bi-directional current sensing output (CS), FLT/EN I/O, high-side supply (V_B), and high-side turn-on/off dV/dt control ($R_{DDH,SSH}$). The external low-side components around the IC include V_{CC} supply capacitor (C_{VCC}) connected between V_{CC} pin and P_{GND}, low-side turn-on dV/dt set resistor (R_{DDL}) connected between R_{DDL} pin and V_{CC} pin, low-side turn-off dV/dt set resistor (R_{SSL}) connected between R_{SSL} pin and P_{GND}, current sense amplitude set resistors ($R_{SET1,2}$) connected from CS pin to ext. V_{REF} and P_{GND}, and pull-up resistor (R_{FLT}) connected from FLT/EN pin to V_{CC}. The external high-side components around the IC include V_B supply capacitor (C_{VB}) connected between V_B pin and V_{SW}, high-side turn-on dV/dt set resistor (R_{DDH}) connected between R_{DDH} pin and V_B pin, and high-side turn-off dV/dt set resistor (R_{SSL}) connected between R_{SSL} pin and V_{SW}.

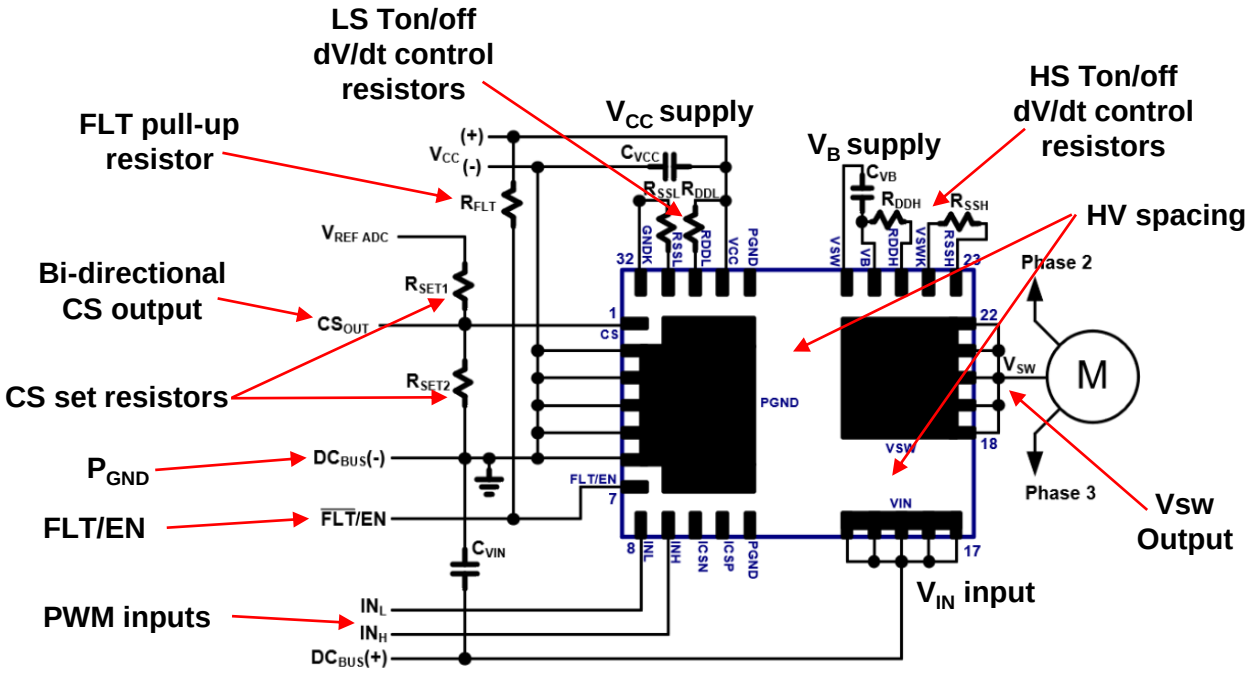


Fig 3. NV6257 connection diagram

The following table (Table 1) shows the recommended component values (typical only) for the external components connected to the pins of the IC. These components should be placed as close as possible to the IC. Please see PCB Layout Guidelines for more information.

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} low side IC supply capacitor	0.1	µF
$R_{DDL,H}$	Low-side/high-side gate drive turn-on current set resistor	200	Ω
$R_{SSL,H}$	Low-side/high-side gate drive turn-off current set resistor	50	Ω
$R_{SET1,2}$	Current sense amplitude set resistors	Page 7, Equation 1	Ω
R_{FLT}	FLT/EN pull-up resistor for enabling of the device	5000	Ω
C_{VB}	V_B high side IC supply capacitor	0.01	µF

Table 1. Recommended component values (typical only)

NV6257 400W 3-ph Motor Inverter Evaluation Board

A multi-layer, 3-ph motor inverter evaluation board has been designed for bench testing purposes and to review the basic functionality and switching performance of the IC (Fig. 4). The EVB can be easily connected to an MCU at the input and a motor load at the output, and includes the IC and all necessary external components. The external IC components have been placed and routed as close the IC as possible. Large copper planes and thermal vias have been placed on all layers at both source pads for good thermal management. See PCB Layout Guidelines (page 14) for more information on proper PCB layout design.

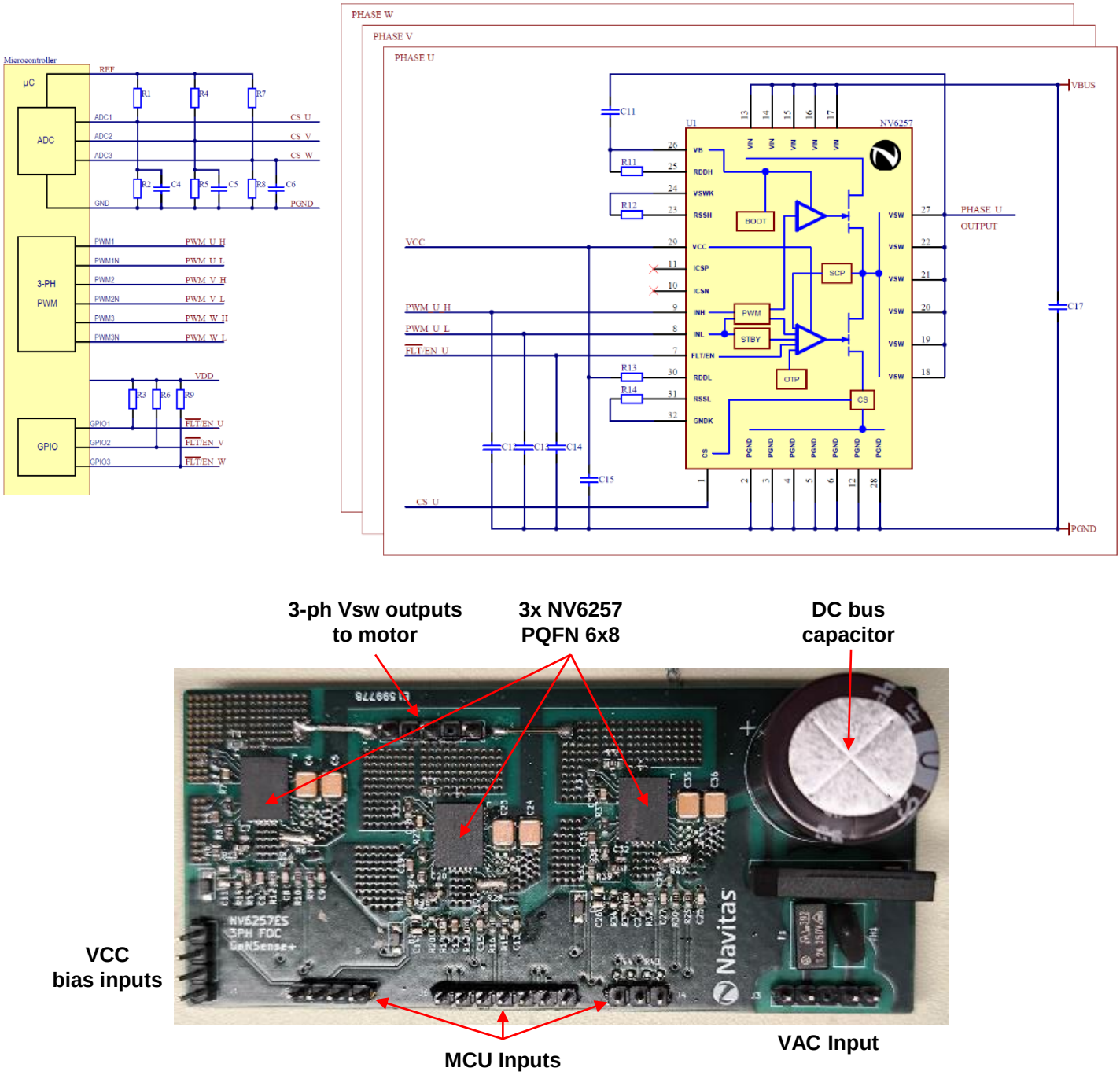


Fig 4. NV6257 400W 3-ph motor inverter schematics & EVB

NV6257 400W 3-ph Motor Inverter Evaluation Board (cont.)

The basic motor inverter switching waveforms (Fig. 5, 3-ph mod FOC, 8 kHz) includes the I_{DS} current (entering the Vsw pin) and the corresponding bi-directional CS pin voltage (single phase). The amplitude of the bi-directional CS pin voltage shows excellent (+) and (-) tracking of the I_{DS} current. The CS pin voltage of all three phases are monitored directly by the ADC block of the MCU, and then used to perform the necessary modulated FOC control without the need for external shunt resistors.

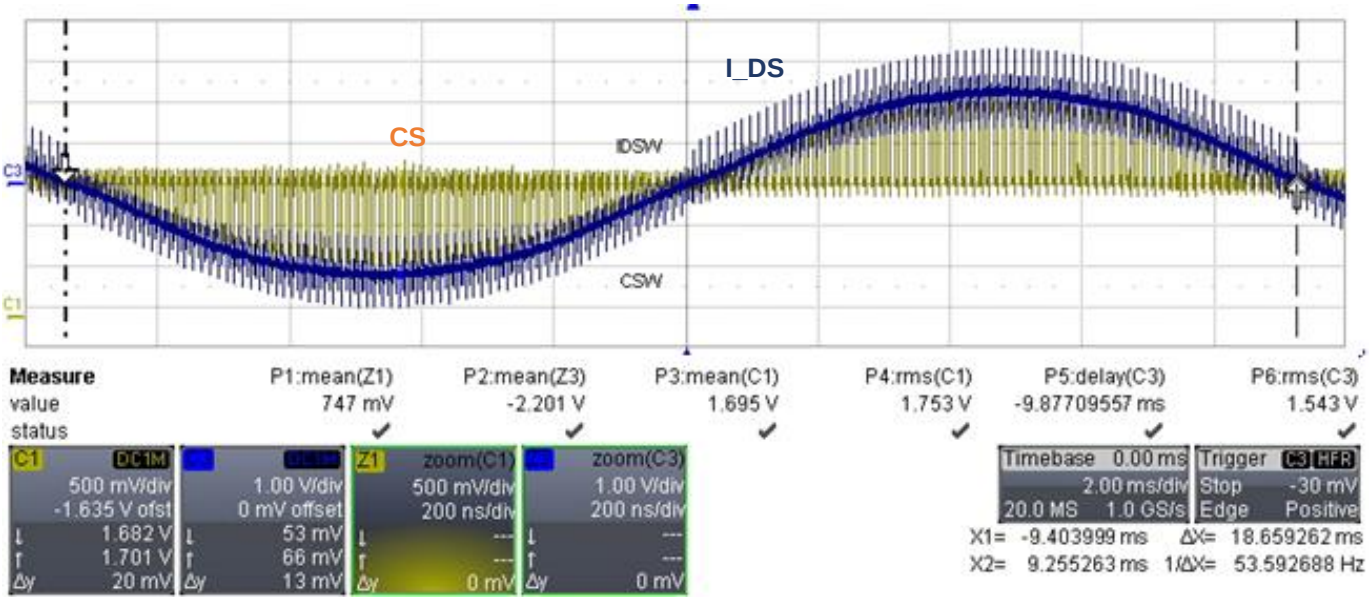


Fig 5. Motor inverter IDS & CS waveforms
(3-ph mod FOC, F_{SW} = 8 kHz, single phase shown)

Bi-directional Loss-Less Current-Sensing

The current flowing through the internal low-side GaN power FET is sensed internally and then converted to a current at the current sensing output pin (CS). An external resistor divider (R1, R2) is connected to the CS pin and is used to set the amplitude of the CS pin voltage signal (Fig. 6). This allows for the CS pin signal to work with different controllers with different current sensing input thresholds. It is recommended to place the resistor divider close to the CS pin for improved robustness against system noise. The resistor divider is driven by an external voltage, allowing it to set the mid-point voltage at an arbitrary level. Positive current through the GaN power FET will result in a current out of the CS pin, increasing the voltage at the mid-point of the resistor divider, and negative current through the GaN power FET will result in a current into the CS pin, reducing this voltage. The CS pin current is a function of the gain factor and the absolute current in the power transistor (see Equation 1). Care should be taken in the choice of resistor values, to ensure that the voltage range corresponding to full positive to full negative current is adequately positioned within the ADC input voltage range, and the maximum voltage at the CS pin (see Equation 2).

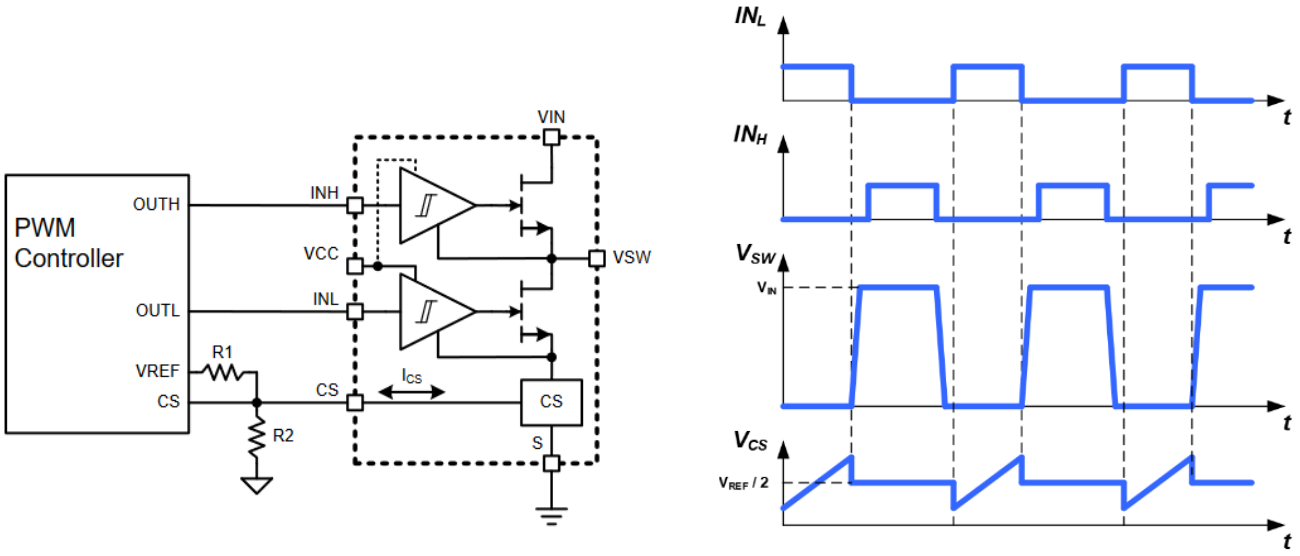


Fig 6. Bi-directional simplified schematic & timing diagram

$$Gain = \frac{ICS}{IDS} = \frac{1.25mA}{4.5A} = 0.2778\frac{mA}{A}$$

Eq. 1. Internal Current Sense Amplifier Gain Ratio

$$V_{CS} = \frac{R_{CS}}{2} * Gain * I_{DS} + \frac{VREF}{2}, with\ RCS = R1 = R2$$

Eq. 2. Current Sense Pin Voltage

Autonomous Synchronous Rectification Mode

In motor inverter applications where reverse current can flow through the power switches, also called "freewheeling", the voltage across the switch in combination with the reverse current can create high power dissipation. In order to reduce the impact, multiple things can be done, including shortening the dead time (depending on the control algorithm), or driving the power switch as a synchronous rectifier (requiring appropriate control firmware). The IC provides autonomous synchronous rectification, where upon detection of significant reverse current, the power switch is turned ON, and upon approaching zero current (SR_{OFF}) the switch is turned OFF, without any burden on the controller. The activation sequence of the SR functionality includes arming, turn-on, turn-off, and re-arming (Figure 7). During the arming phase, the IC will "arm" itself for SR operation if V_{DS} exceeds the SR_{ARM} voltage (9.8V typical). During the turn-on phase, if the chip was previously "armed" AND V_{DS} falls below the SR_{ON} voltage (-1.05V typical) for more than the $SR_{DEGLITCH}$ interval (100ns typical), the driver will activate and turn on the power FET gate. The gate will stay on for at least the SR_{MOT} minimum on time interval (90ns typical) to ensure switching noise does not falsely trip the turn-off detection circuit. During the turn-off phase, once the magnitude of current flowing from Source to Drain falls below the SR_{OFF} threshold (600mA), the chip will turn off the power FET gate. During the final re-arming phase, V_{DS} must rise above the SR_{ARM} voltage (9.8V typical) for the chip to be ready for the next SR cycle.

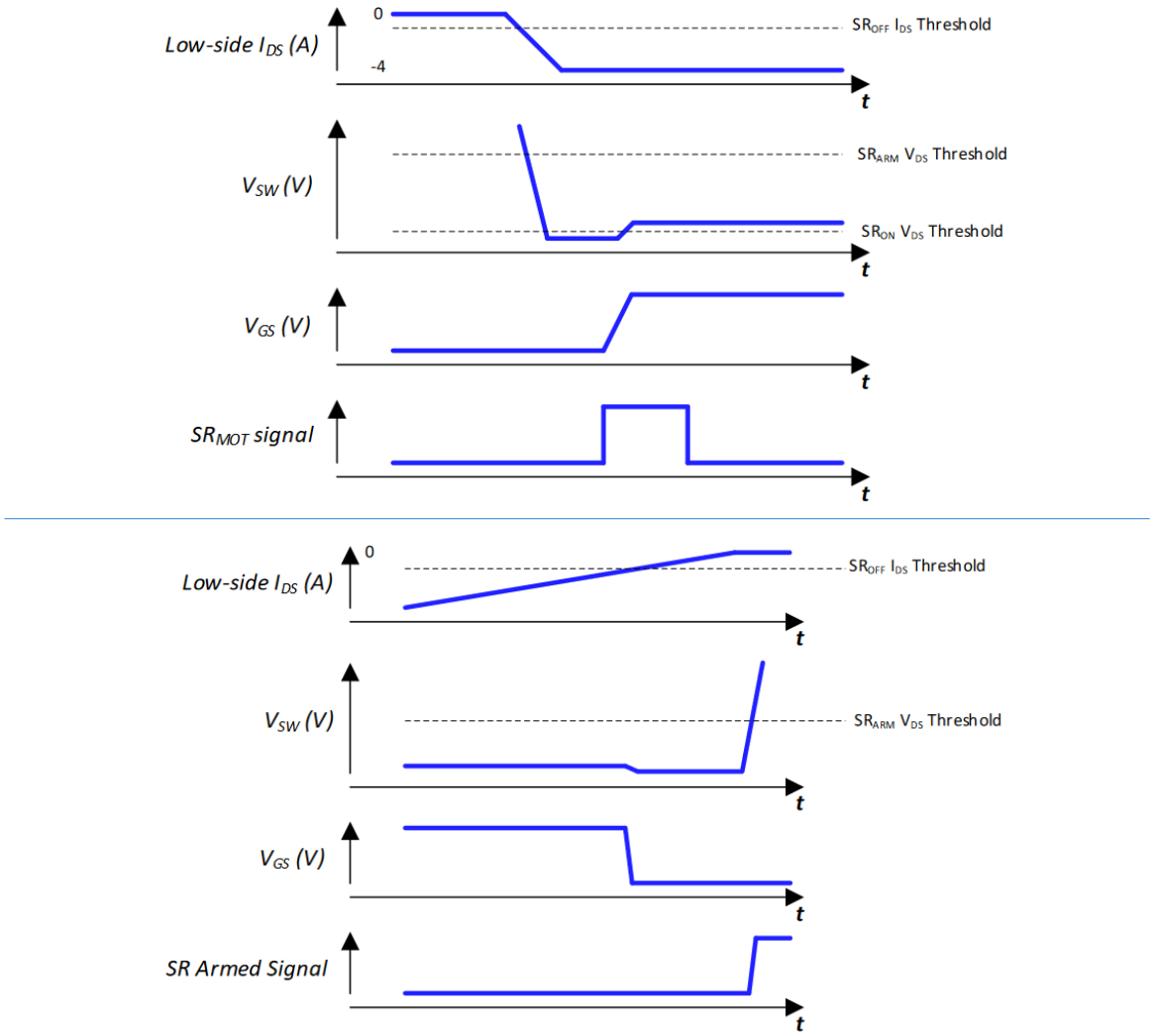


Figure 7. Auto SR mode turn-on (upper) and turn-off (lower) timing diagrams

Over-Temperature Protection (OTP)

The IC includes over-temperature detection and protection (OTP) circuitry to protect the IC against excessively high junction temperatures (T_J). High junction temperatures can occur due to overload, high ambient temperatures, and/or poor thermal management. Should T_J exceed the internal T_{OTP+} threshold (165℃, typical) then the IC will latch off safely (Fig. 8). When T_J decreases again and falls below the internal T_{OTP-} threshold (105℃, typical), then the OTP latch will be reset. Until then, internal OTP latch is guaranteed to remain in the correct state while V_{CC} is greater than 5 V. During an OTP event, the IC will latch off and the system V_{CC} supply voltage can decrease due to the loss of the aux winding supply. The system V_{CC} will fall below the lower UV- threshold of the system controller and the system high-voltage start-up circuit will turn-on and V_{CC} will increase again (Fig. 8). V_{CC} will increase above the rising UV+ threshold and the controller will turn on and deliver PWM pulses again, but the IC will remain off until T_J has decreased below T_{OTP-} and the OTP fault latch is reset. Once the fault latch is reset, the IC will start switching again at the next PWM pulses from the controller.

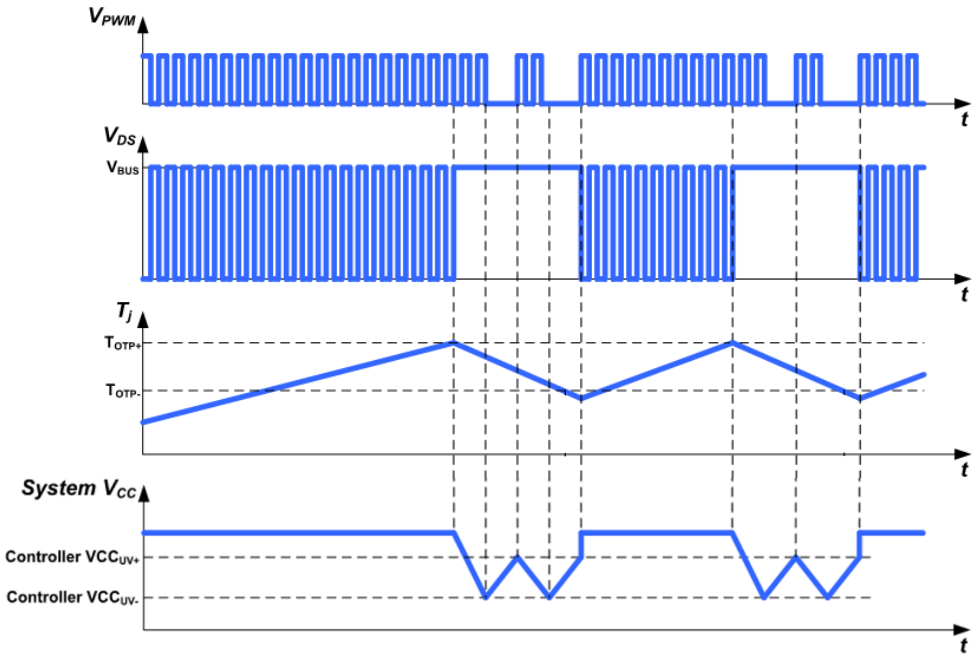


Fig 8. OTP timing diagram

Programmable Turn-on dV/dt Control

During hard-switching conditions, it is desirable to limit the turn-on/off dV/dt slew rates of the drain of the low- or high-side GaN power FET. This is necessary to reduce EMI or reduce circuit switching noise. Resistors $R_{DDL,H}$ set the turn-on current of the internal high- and low-side gate drivers and sets the turn-on dV/dt slew rate of the drain of the high- and low-side GaN power FETs (Fig 9). Resistors $R_{SSL,H}$ set the turn-off current of the internal high- and low-side gate drivers and sets the turn-on dV/dt slew rate of the drain of the high- and low-side GaN power FET (Fig. 9). The actual low-side and high-side turn-on/off dV/dt slew rates versus different $R_{DDL/H}$ and $R_{SSL/H}$ resistor values are also shown (Fig. 10).

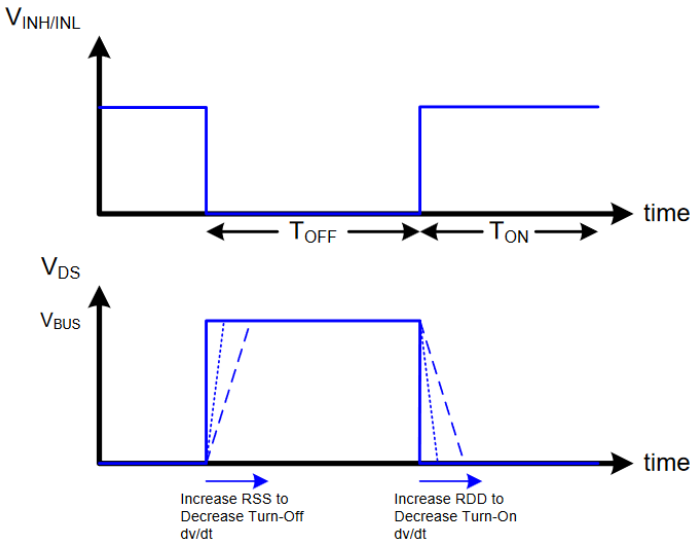


Fig 9. High- & low-side turn-on/off dV/dt slew rate control timing diagram during hard-switching conditions

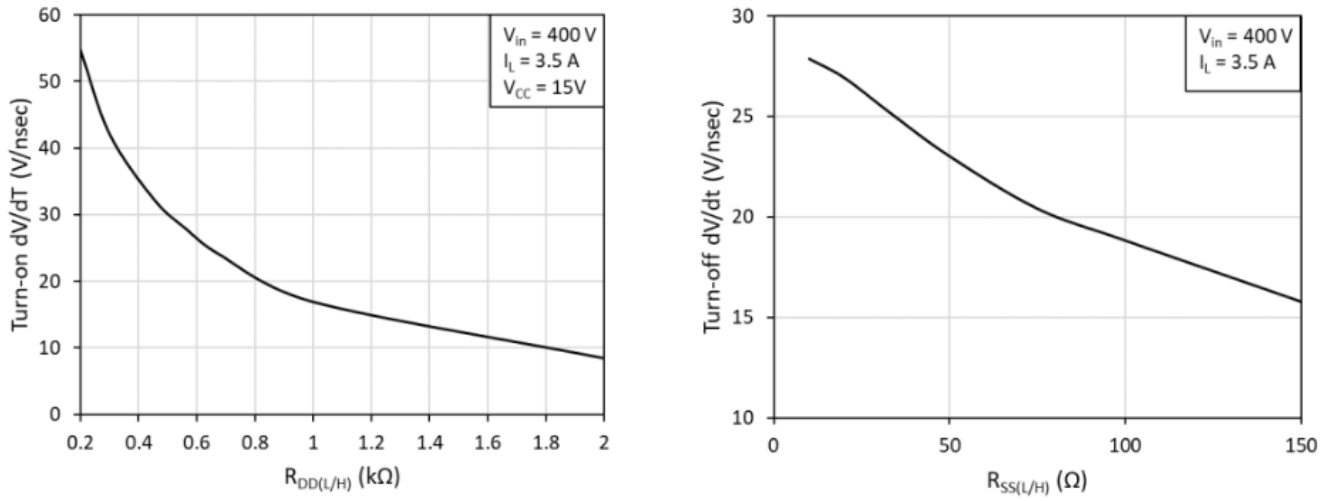


Fig 10. High-side & low-side turn-on dV/dt vs $R_{DDL,H}$ and high-side & low-side turn-off dV/dt vs $R_{SSL,H}$

PCB Layout Guidelines (PQFN 6x8 mm)

For best electrical and thermal results, these PCB layout guidelines (and 3 steps below) must be followed:

1) Place IC components as close as possible to the GaN IC. Place $R_{SET1,2}$ resistors directly next to CS pin to minimize high frequency switching noise.

2) Connect the ground of IC components to Source to minimize high frequency switching noise. Connect controller ground also to Source (P_{GND}).

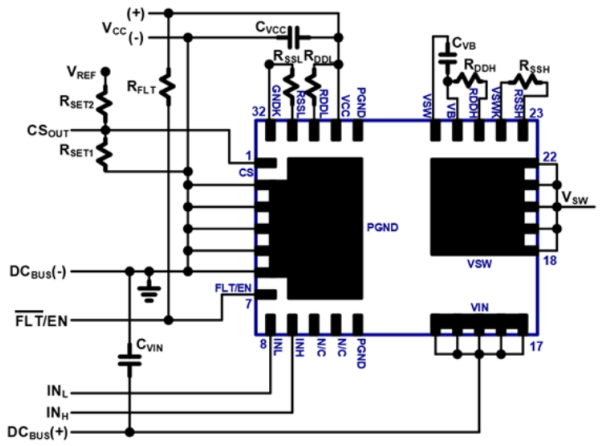
3) Route all connections on single layer. This allows for large thermal copper areas on other layers.

4) Place large copper areas on and around Pad1 and Pad2.

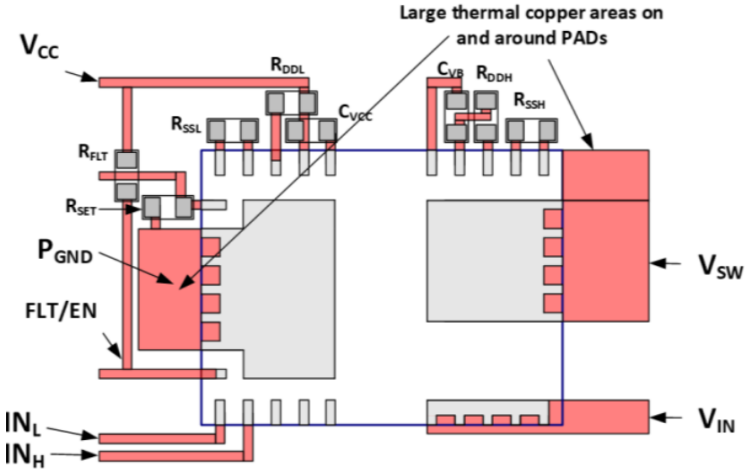
5) Place many thermal vias inside Pad1 and Pad2 and inside Pad1 and Pad2 copper areas.

6) Place large possible copper areas on all other PCB layers (bottom, top, mid1, mid2).

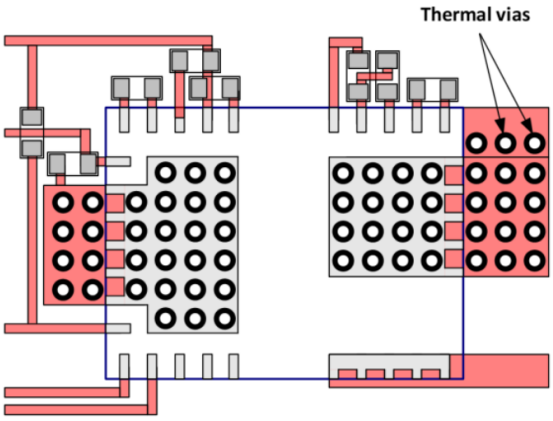
Do not extend copper planes from the low-side across the components or pads of the high-side; do not extend copper planes from the high-side across the components or pads of the low-side! Keep high and low-side layouts separate. Do not overlap!



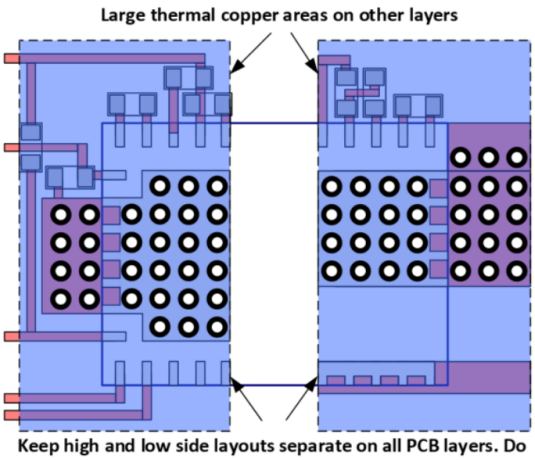
IC connection diagram



Step 1. Route all connections on single layer. Make large copper areas on and around Source pad



Step 2. Place many thermal vias inside source pad and inside source copper areas.
(via outer dia=0.65mm, via hole=0.33mm, via pitch=0.925mm, via wall thickness=1mil)



Step 3. Place large copper areas on other layers. Make all thermal copper areas as large as possible!
Keep high and low side layouts separate on all PCB layers! Do not overlap high- and low-side layouts

Fig 11. PCB layout steps

Electrical Simulation Models

PSPICE-based electrical simulation models have been developed for the NV6257/87/88 product family. The models are compatible with SiMetrix, LTSPICE and PSPICE platforms, and include all internal circuitry and logic, current-sensing, level-shifting, bootstrap, protections, and both high- and low-side GaN power FETs. The model file (.cir) and steady-state waveforms are shown for a resistive hard-switching circuit (Fig. 12). Both PWM inputs (IN_H and IN_L) are shown together with the half-bridge switched node (V_{SW}) and drain pull-up resistor current (I_{R1}).

```
* NV6257-1_COMPLETE
*$
********************************************************************************
*
* NV6257-1 Spice Model
*
********************************************************************************
*
* This simulation model uses typical parameter values and it is based on
* a behavioral model. This model is supplied "as is" and the author
* provides no warranties, either expressed or implied, with respect
* to the operation and accuracy of the model within a customer circuit
* or system.
*
********************************************************************************
*
* NAVITAS SEMICONDUCTOR
* Part Nr:      NV6257-1
* Date:   01/08/2025
* Model Type: SPICE (LTspice / Pspice compatible)
* Model Version: v1.1
*
* Revision notes:
*
* v1.0 - Initial version
*
********************************************************************************
*
* NV6257-1 Top level 12/05/2024
*
********************************************************************************
.SUBCKT NV6257-1 VCC RDDL RSSL GNDK FLT INH INL CS VB RDDH RSSH VSWK VIN VSW
.PARAM VCCTH=7.35 VCCHYS=2.5 VDDLTH=4 VDDLHYS=0.5 VBTH=7.35 VBHYS=2.5 VDDHTH=
+ VLHYS=1.4 CSGAIN=277u TOTP=160 IQCC=1.1m IQCCSTBY=300u VSCP=9.8
V1 N015 SGND {VLTH}
C1 INH SGND 1p
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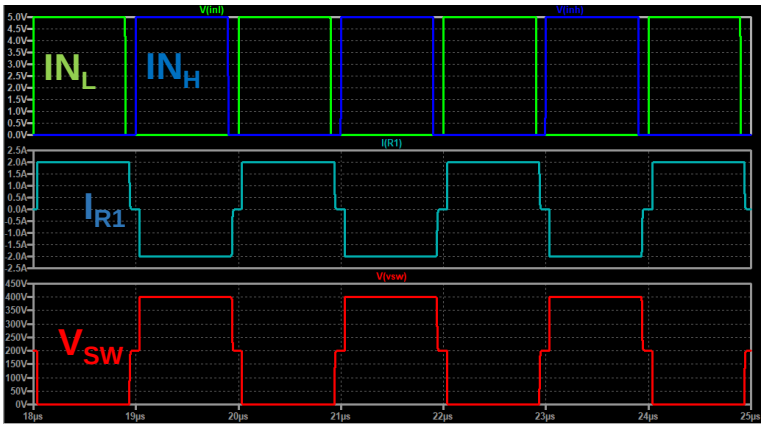

Fig 12. NV6257 SPICE model and simulation waveforms (resistive hard-switching conditions)

3D Mechanical Models

3D mechanical models have been developed for this IC (Fig. 13). The NV6257/87/88 .stp files are available and easily importable into many popular PCB design software platforms (such as Altium Designer). This model is useful for generating 3D renderings of assembled power supply designs to check for any design issues before releasing PCB gerber files for manufacturing.

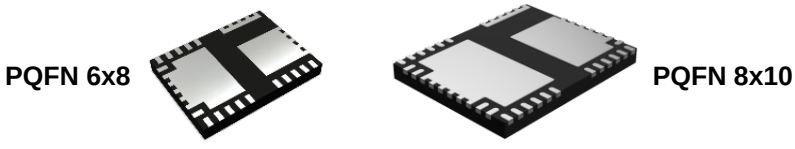

Fig 13. Bottom views of 3D models of NV6257 (left, PQFN6x8) & NV6287/88 (right, PQFN8x10)

References (www.navitassemi.com)

1) GaNSense Motor Drive ICs NV6257/87/88 datasheets, Navitas Semiconductor, 2025
2) New GaNFast Power ICs with GaNSense Technology Loss-Less Current Sensing & Autonomous Protection, AN015, Navitas Semiconductor, 2021
3) GaNFast Half-Bridge ICs with GaNSense Technology, AN020, Navitas Semiconductor, 2023

Revision History

Date	Status	Notes
May-1, 2025	Final	

Additional Information

Contact: info@navitassemi.com