1200 V Schottky Diodes With Temperature Invariant Barrier Heights and Ideality Factors

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I. Introduction

This product note demonstrates the near theoretical ideality factors and barrier heights measured on GeneSiC's 1200V SiC Schottky diodes, which were designed for operation at temperatures > 225 °C, and targeted for down-hole oil-drilling, aerospace and electric vehicle applications. The temperature invariance of the ideality factors and barrier heights measured on the GeneSiC diodes enabled near theoretical Richardson's constants to be extracted. These results are an indication of the robust Schottky surface preparation procedures used for the design and fabrication of the Schottky diodes at GeneSiC, resulting in a homogeneous spatial distribution of barrier heights at the metal-semiconductor interface[i].

II. Extraction of Barrier Heights and Idealities

The forward current flow in Schottky diodes which are unipolar devices is dominated by the thermionic emission process assisting the majority carrier injection. The forward bias current can be expressed as:

$$J = J_o[\exp\left(\frac{qV}{nkT}\right) - 1] \quad (1)$$

where '*q*' is the electronic charge, '*V*' is the applied bias, '*kT*' is the thermal energy, '*n*' is the ideality factor, '*J*' is the forward current density and 'J_o' is the saturation current density[ii]. The saturation current density can be expressed as:

$$J_o = A^*T^2 \exp\left(-\frac{q\emptyset_{BN}}{kT}\right) \quad (2)$$

where '$\emptyset_{BN}$' is the metal-semiconductor Barrier Height and '*A**' is the effective Richardson constant whose theoretical value is 146 A cm^{-2} K^{-2} for 4H-SiC.

The Ideality Factor (IF) is a measure of the quality of the Metal-Semiconductor (Schottky) interface and assumes values $\geqslant 1$. An ideality factor of exactly 1 indicates a theoretical Schottky interface. The thermionic work function of the Schottky metal employed and associated processing determine the Barrier Height (BH) of a Schottky diode. Both BH and IF of Schottky diodes vary with the semiconductor surface morphology[iii]. Any surface contamination introduced during the diode fabrication process deteriorates the surface homogeneity, which affects the BH and the IF of the diodes.

The parameters BH, IF and A* are extracted from the measured forward I-V curves as described below. Equation (1) can also be expressed as:

$$J = J_o \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{-qV}{nkT}\right)\right] \quad (3)$$

From the semilog plot of log $\left(\frac{J}{\left[1-exp\left(\frac{-qV}{nkT}\right)\right]}\right)$ and V, the intercept of the current density axis at V = 0 gives the saturation current density, J_o. The BH (ϕ_{BN}) can be expressed as:

$$\emptyset_{BN} = \left(\frac{kT}{q}\right) In\left(\frac{A^*T^2}{J_o}\right) \quad (4)$$

The zero bias saturation current densities at different temperatures are extracted from the semilog plots, from which the BHs are calculated using (4). The slope of the above semilog plot is given by $\left(\frac{q}{2.3nkT}\right)$, from which IFs at different temperatures are calculated and shown in Figure 1.

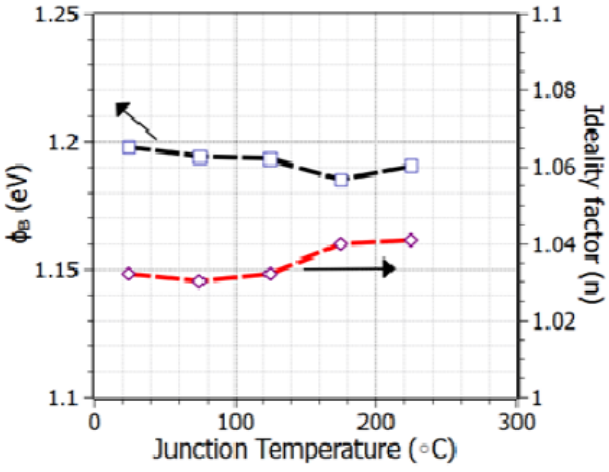

Fig. 1: Temperature dependence of barrier height and ideality factor calculated from measurements on a representative JBS diode.

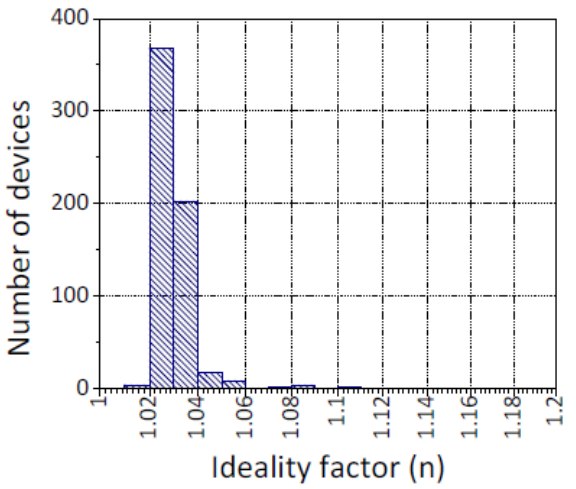

Figure 2: Histogram of ideality factors extracted from I-V measurements on 1200 V rated JBS diodes from a representative wafer.

The extracted BHs and IF are almost temperature invariant, as can be seen in Figure 1. Moreover as shown in Figure 2, the IF values measured on all devices from one wafer are confined in a narrow range between 1.02 and 1.04, which validates the successful implementation of robust processing techniques used for fabrication. These results are made possible by the highly homogenous Schottky metal-SiC interface resulting from optimized device processing techniques employed at GeneSiC.

III. Extraction of Richardson's constant

A conventional Richardson's plot is the plot of $\ln(I/T^2)$ as a function of $1/T$ at a constant forward bias voltage. Using (2), (1) can also be written as:

$$\ln\left(\frac{I}{T^2}\right) = \ln(AA^*) - \frac{q(\emptyset_{BN} - V/n)}{kT} \quad (5)$$

'I' can be replaced with 'I_s' for V=0. So, Richardson's constant can be extracted from the X-axis intercept of the plot of $\ln(I_s/T^2)$ versus 1/T, whose slope is a function of BH. The values of BH and IF required for the Richardson's plot are derived using the procedures explained in section 1. Richardson's plots are prone to show nonlinear behavior when both the IF and BH are temperature dependent. Since, the IF and BH plots are nearly temperature independent for the GeneSiC diodes (Figure 1), the Richardson's plot is perfectly linear as shown in Figure 3. The extracted Richardson's constant is 138.2 A/cm^{2}K^2, which is close to the theoretical value of 146 A/cm^{2}K^2 for 4H-SiC. The extracted near-theoretical Richardson's constant indicates the homogeneous spatial distribution of BHs at the metal-semiconductor interface.

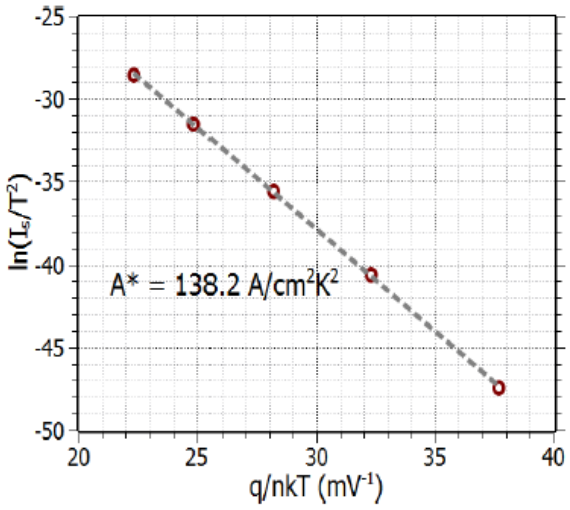

Fig. 3: Richardson's plot of a representative JBS diode constructed using Φ_{BN} and n values from Figure 1, from which a near-ideal A*=138 A/cm^{2}K^2 is extracted.

References

i. F. Roccaforte et al. J. Appl. Phys. 93(11), 2003, pp. 9137-9144.

ii. Dieter K. Schroder, “Semiconductor material and device characterization”, Wiley-Interscience publication, ISBN: 0-471-24139-3

iii. K.V. Vassilevski et al. “Microelectronic Engineering”. 83, 2006, pp. 150–154.

Additional Information

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