APPLICATION NOTE
AN1001

Silicon Carbide (SiC) Power Diode Reliability

CONTENTS

1 – Summary

GeneSiC Semiconductor's Silicon Carbide (SiC) Merged PiN-Schottky (MPS™) power diodes have a proven track record over the last few years and therefore, an outstanding record of inherent reliability performance. The *MPS* and *SLT* series of the SiC Merged PiN-Schottky power diode family have already entered the maturity phase of their lifecycles and have accumulated more than 10 billion device-hours in field applications and the total FIT (Failures in Time) rate for this family is 1.5 failures per billion device hours which substantiate our long-established technology. This paper explains the approach to reliability assessment and presents the expected lifetime under various operational and environmental conditions.

The earliest generations of the SiC power diodes were the basic Schottky Barrier Diodes (SBDs) which were prone to increasing reverse leakage currents over time until they exhibited catastrophic failures. Later, the trend moved towards the development of the Junction Barrier Schottky (JBS) diodes to result in extremely lower reverse leakage currents and higher breakdown voltages. This enhanced design significantly increased both – the reliability and the robustness of the diode. However, during a high surge current condition, the pure Schottky diode essentially transitions into thermal runaway due to the resultant high forward voltage drop and therefore, resulting in eventual damage of the diode. Again, the industry evolved into the modern generation known as Merged PiN-Schottky (MPS™) SiC power diodes which exhibit an increased forward current conduction capability in both, steady state and forward transient conditions with only a slight increase in the forward voltage drop. This prevented the thermal runaway of the diode and demonstrated a much higher degree of the device ruggedness.

In addition to these, the inherent natural properties of Silicon Carbide (SiC) have proved its reliability for high power and high-temperature semiconductor devices. It is highly corrosion resistant, exhibits high mechanical robustness and has a thermal conductivity comparable to that of copper. GeneSiC Semiconductor thrives to ensure a highly reliable process flow to meet the engineering challenges and manufacture promising high-quality semiconductor devices.

2 – Reliability Assessment

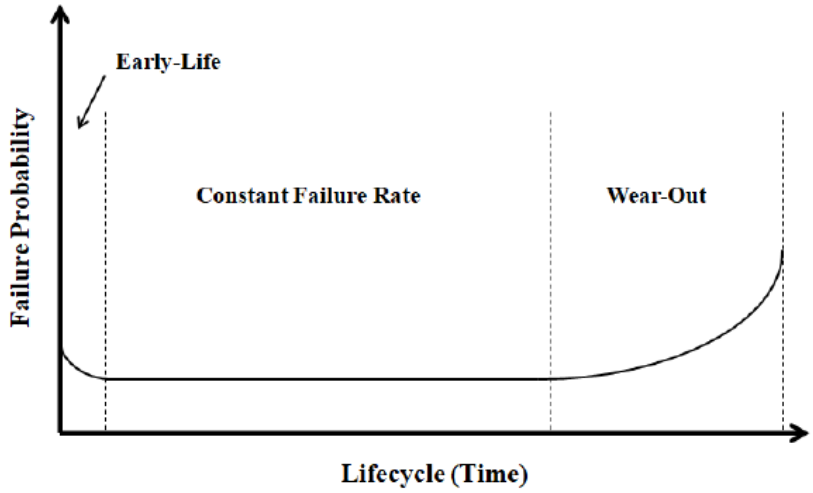
Reliability is defined as the probability that a semiconductor device will continue to provide its intended performance under rated operating conditions over a specified period of time.

GeneSiC Semiconductor's approach to reliability assessment begins at the R&D center itself with a series of robustness and operational stress tests at different ambient conditions. Once the materials and device design establish an excellent test record, a series of qualification tests are performed to the newly developed device to ensure that the product meets our rigorous quality standards. Later, ongoing reliability assessments are made in fielded products. We firmly believe that actual field data presents a very substantial picture of the device reliability. However, this data is only meaningful after a significant number of device hours are achieved in actual field applications. GeneSiC Semiconductor's SiC power diodes have an established record in the field – needless to say, that it is very promising to accept the high reliability and robustness.

Lifecycle

The typical lifecycle of any semiconductor device can be categorized into three phases:

- Early-Life
- Constant Failure Rate
- Wear-Out



The figure below shows the failure probability of a semiconductor device during these three phases. It is commonly known as the bath-tub curve. With a high-quality manufacturing operation and development stage reliability assessment, GeneSiC Semiconductor has significantly reduced the probability of failure during the early-life stage (sometimes commonly known as 'infant mortality'). This failure probability is now only slightly higher than that during the constant failure rate stage. Wear-Out failures occur towards the end of the product lifecycle due to degradation processes inherent to the materials and process technologies used in the manufacture of the semiconductor device.

Reliability Metrics

The following table provides the definitions of industry standard terms used to describe the failure rate of semiconductor devices.

Term	Symbol	Definition
Failure in Time	FIT	This metric specifies the average failures rate in 10^9 device operation hours during the early-life and constant failure rate stages of the device lifecycle.
Mean Time to Failure	MTTF	This metric describes the time at which 50% of the devices are expected to reach the wear-out phase of the life cycle.
Acceleration Factor	A_f	It is a constant derived from experimental data to relate the failure rates from accelerated test conditions to field conditions.

Reliability Calculation

The most dominant approach to establishing a reliability level is to evaluate the probability of failure in different phases of the lifecycle. Infant mortality is typically related to quality control issues and GeneSiC Semiconductor has successfully reduced the failure rate during this phase with a superior manufacturing operation. So, the FIT rate calculated during this phase should be a conservative approximation of the failure rate until wear-out. The following mathematical models should be used to calculate the reliability metrics.

$$FIT = \frac{X^2_{(1-\alpha),(2*F+2)}}{2 * N * t_w * A_f} * 10^9$$

$$MTTF = \frac{1}{FIT} * 10^9$$

The acceleration factor (A_f) can be determined from the Arrhenius equation which is used to describe the physio-chemical reaction rates. It is an appropriate mathematical model for expressing the thermal acceleration of semiconductor device failure mechanisms. For field data, $A_f = 1$ as the data represents an un-accelerated operation of the device.

$$A_f = \frac{t_{use}}{t_{stress}} = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)}$$

X^2 = Statistical estimator or chi-square factor for (2*F + 2) degrees of freedom at (1 - α) probability
α = Confidence limit between 0 and 1 (Usually 60% for SiC semiconductor discrete)
F = Observed number of failures in field applications
N = Number of devices in field applications
t_w = Weighted average time of operation
t_{use} = Use time
t_{stress} = Accelerated stress time

E_a = Activation Energy (eV)
k = Boltzmann's constant (eV/K)
T_{use} = Use temperature (K)
T_{stress} = Accelerated Stress temperature (K)

The activation energy (E_a) can typically range from 0.3 eV to 1.3 eV depending upon the type of the failure mechanism. This value cannot be accurately determined for random field failures during the constant failure rate phase of the bathtub curve, so a conservative value of 0.6 eV is used by convention for calculating the reliability metrics. The following table provides typical values of the activation energy for different failure mechanisms during critical reliability tests in the laboratory.

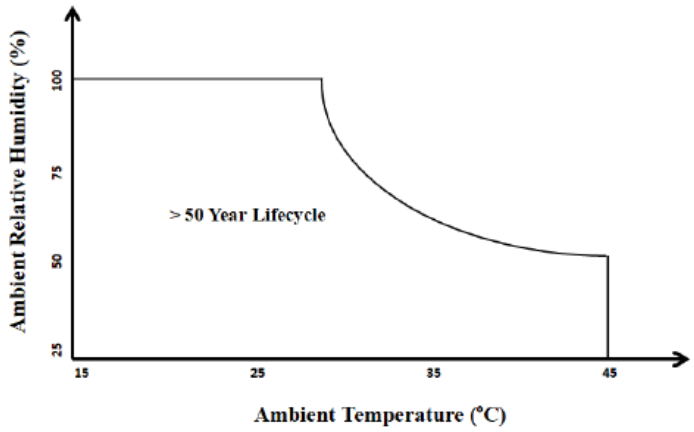
Failure Mechanism	Activation Energy	Testing Methodology
Electro-Chemical Defects and Corrosion	0.3 eV – 0.5 eV	High-Temperature Operating Life (HTOL), Highly Accelerated Stress Testing (HAST), and Voltage Stress
Assembly Defects	0.5 eV – 0.7 eV	Temperature Cycling, Mechanical Shock, and Environmental Stressing
Mask Defects	0.7 eV	HTOL and Voltage Stress
Charge Injection	1.3 eV	HTOL

** It should be noted that there are many more reliability tests performed on our devices and this table is only intended to provide a guideline for selection of the value of activation energy for reliability calculations.

For GeneSiC Semiconductor's SiC Power Diodes, the goal is to ensure that wear-out occurs well after the designed life-cycle. The dominant failure cause at wear-out would be driven by temperature as no significant degradation occurred during HAST and voltage stress testing. This temperature effect can be represented by associated thermal activation energy (E_a) derived by taking the ratio of the times t_{use} and t_{stress} at temperatures T_{use} and T_{stress} using the Arrhenius equation stated before.

Environmental Reliability

GeneSiC Semiconductor's SiC Power Diodes are designed to perform for more than 50 years in any climate controlled environment. However, in critical cases, the primary environmental failure cause is humidity related and it involves electro-chemical degradation due to moisture. The figure below shows the humidity-temperature envelope for SiC Schottky Diodes.



3 –Conclusion

This paper has presented a comprehensive approach to reliability assessment on GeneSiC Semiconductor's SiC power diodes and indicated a very low failure rate of the devices under various stress conditions. In the field, the **MPS** and **SLT** series have an estimated wear-out lifecycle of more than 50 years and recorded FIT values of 1.5 failures per billion device hours (or MTTF of $6.67 * 10^8$ hours at junction temperature limited to 175 °C) which is very competitive with the other established SiC power discrete technologies. In a nutshell, this data makes GeneSiC Semiconductor's SiC power diodes extremely reliable for high temperature and other stringent environmental conditions.

Additional Information

Contact: info@navitassemi.com