0 V Turn-Off of Navitas' 650 V Gen3 'Fast' Trench-Assisted Planar SiC MOSFETs

Silicon carbide (SiC) MOSFETs have garnered extensive application within the realm of power electronics due to their exceptional performance characteristics. The capability of SiC MOSFETs to turn off at a gate voltage of 0 V facilitates the simplification of gate drive circuit design, reduces system costs, and enhances overall system reliability. However, the occurrence of parasitic false turn-on (PTO) remains a pivotal challenge that significantly impacts the viability of utilizing a 0 V gate voltage for SiC MOSFET turn-off. This application note delves into the fundamental principles underlying the behavior of PTO and presents experimental evidence to elucidate the various influencing factors, including gate turn-off resistance, junction temperature, and the rate of drain-source voltage rise. Through rigorous analysis, this study conclusively establishes a correlation for the optimal matching of drive resistance, which is indispensable for ensuring the reliable operation of SiC MOSFETs during 0 V gate voltage turn-off.

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1. Introduction

With the swift evolution of power electronics technology, silicon carbide (SiC) MOSFETs have emerged as pivotal semiconductor devices, distinguished by their exceptional switching performance, minimal power losses, high-temperature endurance, and numerous other advantages. They are ideally suited for applications demanding high power density and efficiency, encompassing switch-mode power supplies, electric vehicles, photovoltaic inverters, and industrial motor drives.

The Miller capacitor-induced parasitic false turn-on (PTO) phenomenon typically manifests in circuits utilizing SiC MOSFET half-bridges. This issue not only poses risks of device malfunction but also significantly impacts the efficiency, stability, and reliability of power electronic systems that rely on 0V gate voltage turn-off. Traditionally, the recommendation has been to employ negative gate voltage for SiC MOSFET turn-off to mitigate this challenge. However, this approach complicates gate drive circuit design and elevates system costs. Consequently, exploring the feasibility of utilizing 0 V gate voltage for SiC MOSFET turn-off is of considerable significance. This method enhances gate drive design flexibility by eliminating the need for a negative voltage power supply, thereby simplifying circuit design and reducing costs.

In this application note, the principles underlying the PTO phenomenon have been analyzed. Subsequently, we investigate and experimentally validate the influencing factors for Navitas' 650 V 20.5 mΩ D2PAK-7L SiC MOSFET (part number G3F25MT06J[1]). Finally, we measure the gate resistance matching to serve as a reference for implementing 0V gate voltage turn-off.

The rest of this application note is organized as follows: Section II analyzes the fundamental principles of PTO. Section III examines the various factors influencing this phenomenon. Section IV presents comparative experimental analyses. Finally, Section V concludes the paper with key findings.

2. Principle of PTO

In converters utilizing a bridge configuration with SiC MOSFETs, rapid switching of these devices results in a swift rise in voltage across their drain and source terminals during turn-off. The rate of voltage change (dv_{ds}/dt) plays a crucial role here. A high dv_{ds}/dt can induce a current through the gate resistor (R_g) via the Miller capacitor (C_{gd}), leading to an excessive induced gate voltage ($V_{gs.ind}$). When this induced gate voltage surpasses the threshold voltage (V_{th}) of the SiC MOSFET, the PTO occurs.

To better understand this phenomenon, an analytical model of a half-bridge circuit for PTO analysis is employed, as illustrated in Fig. 1. The equivalent circuit for this model, valid only during the rising edge of the drain-source voltage of Q_2, is depicted in Fig. 2. When Q_2 is in the off state, its gate voltage is maintained at 0 V.

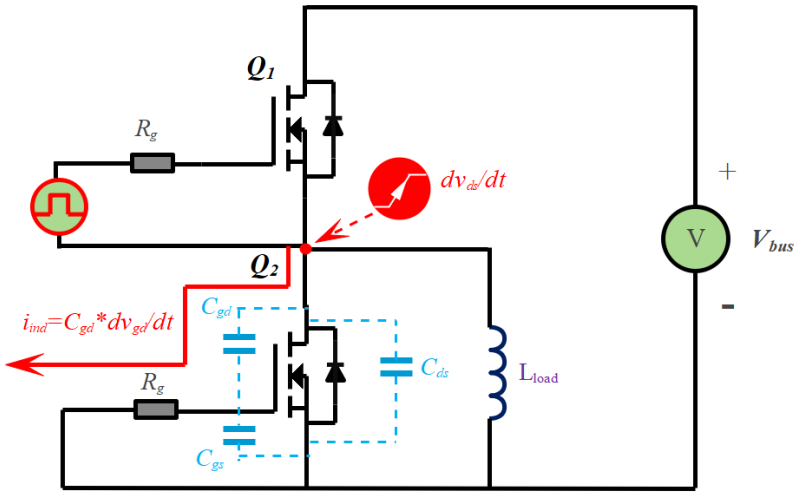

Fig. 1: Half-bridge model circuit for PTO

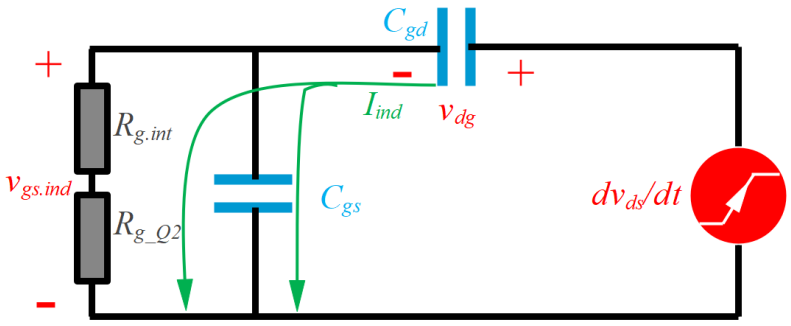

Fig. 2: Equivalent model circuit of the PTO

Using Kirchhoff's circuit laws, we can derive the voltage and current equations governing this circuit. These equations help us understand how the induced gate voltage arises and how it relates to the circuit parameters, including the Miller capacitor, gate resistor, and the rate of voltage change. By analyzing these equations, we can gain insights into the conditions under which PTO is likely to occur and develop strategies to mitigate this issue. The voltage and current equations are given by,

$$v_{ds} = v_{dg} + v_{gs.ind} \tag{1}$$

$$I_{ind} = C_{gd}\frac{dv_{dg}}{dt} = C_{gs}\frac{dv_{gs.ind}}{dt} + \frac{v_{gs.ind}}{R_{g\_Q2} + R_{g\,\mathrm{int}}} \tag{2}$$

where C_{gd} and C_{gs} are the miller capacitor or gate-drain capacitor and gate-source capacitor of the SiC MOSFET. R_{g_Q2} and R_{gint} are the external and internal gate resistances of Q_2 respectively. v_{ds}、v_{dg} and $v_{gs.ind}$ represent the drain-source voltage, drain-gate voltage, and induced gate-source voltage respectively.

Combining Eq. (1) and Eq. (2), the induced gate-source voltage can be derived as:

$$C_{gd}\frac{\left(dv_{ds}-dv_{gs.ind}\right)}{dt}=C_{gs}\frac{dv_{gs.ind}}{dt}+\frac{v_{gs.ind}}{R_{g\_Q2}+R_{g\,\mathrm{int}}} \tag{3}$$

$$C_{gd}\frac{dv_{ds}}{dt}=\left(C_{gd}+C_{gs}\right)\cdot\frac{dv_{gs.ind}}{dt}+\frac{v_{gs.ind}}{R_{g\_Q2}+R_{g\,\mathrm{int}}} \tag{4}$$

3. Analysis of Influencing Factors

3.1 Gate Resistance R_{g_Q2} of Q_2

Upon selection of a SiC MOSFET, the intrinsic parameters such as the gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), and internal gate resistance (R_{gint}) are established. An examination of Equation (4) reveals that the gate resistance of the MOSFET Q_2 in a half-bridge configuration, denoted as R_{g_Q2}, plays a pivotal role in influencing the induced gate-to-source voltage ($v_{gs.ind}$) when the rate of change of the drain-to-source voltage (dv_{ds}/dt) of Q_2 remains constant. Specifically, a positive correlation is observed between $v_{gs.ind}$ and R_{g_Q2}, indicating that as R_{g_Q2} increases, the magnitude of the induced gate voltage also increases. Consequently, this elevation in R_{g_Q2} exacerbates the phenomenon of the PTO, making it more pronounced and potentially detrimental to the stable operation of the SiC MOSFET-based converter circuit.

3.2 Junction Temperature T_j

The characteristics of SiC MOSFETs exhibit a notable correlation between V_{th} and the junction temperature (T_j). Specifically, as T_j increases, V_{th} decreases, demonstrating a negative correlation between these two parameters. This temperature-dependent behavior of V_{th} has significant implications for the operation of SiC MOSFET-based converter circuits. Since the reduction in V_{th} with increasing T_j lowers the threshold for triggering conduction, the risk of the PTO behavior correspondingly increases. Thus, careful consideration of thermal management and the impact of temperature on V_{th} is crucial to mitigate the potential for PTO and ensure the reliable performance of SiC MOSFET-based converter systems.

3.3 Drain-Source Voltage Rising Speed dv_{ds}/dt

The rate of change of the drain-to-source voltage (dv_{ds}/dt) of Q_2 in SiC MOSFET-based converter circuit is governed by the turn-on characteristics of Q1, which can be modulated by adjusting the gate resistor Rg_Q1. According to Equation (4), when Rg_Q2 is held constant, there is a direct relationship between the induced gate-to-source voltage (vgs.ind) and dvds /dt; specifically, vgs.ind increases as dvds /dt rises. The PTO occurs when vgs.ind surpasses the Vth of the SiC MOSFET, leading to unintended conduction. This PTO phenomenon becomes more pronounced as dvds /dt increases, highlighting the importance of carefully controlling dv_{ds}/dt and optimizing the gate resistor values to prevent such undesirable events and ensure stable converter operation.

Based on theoretical analysis, the occurrence of PTO in SiC MOSFETs depends critically on whether the induced gate-source voltage (vgs,ind) exceeds the V_{th}. However, in practical implementations, directly measuring the true gate voltage is infeasible due to package parasitic inductance and internal gate resistances. Instead, engineers typically measure the voltage between the gate terminal and driver-side source terminal of the SiC MOSFET package. This measured voltage, however, does not accurately represent the actual gate voltage due to the aforementioned parasitic components. Therefore, such measurements cannot reliably indicate PTO occurrence under real-world operating conditions.

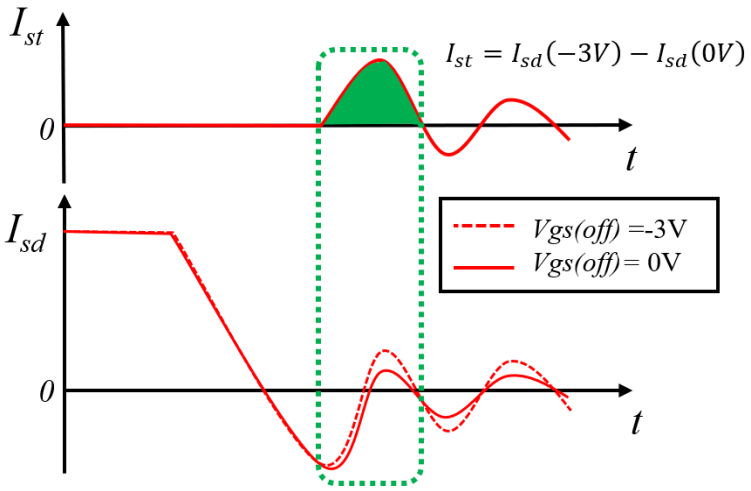

Fig. 3: Reverse recovery waveform diagram

It is imperative to recognize that Q_2 experiences PTO when $v_{gs.ind}$ surpasses V_{th}, resulting in the generation of a shoot-through current (I_{st}). I_{st} represents the difference in the turn-off current of Q_2 when the gate-to-source voltage during turn-off ($V_{gs(off)}$) is -3V compared to when it is 0 V. Fig. 3 illustrates the waveforms of I_{st} and the turn-off current (I_{sd}) of Q_2 in a SiC MOSFET under varying turn-off gate voltage conditions. As indicated by the green area in Fig. 3, PTO can be inferred when I_{st} exceeds 0A. Therefore, I_{st} serves as a practical and effective criterion for determining the occurrence of PTO in SiC MOSFET-based converter circuits.

4. Experimental Results and Analysis

To validate the theoretical analysis findings, a comprehensive double-pulse test platform setup has been established, as illustrated in Fig 4, specifically designed to assess the PTO behavior of the TO-263-7 Navitas' 650V, 20.5mΩ D2PAK-7L SiC MOSFET (G3F25MT06J).

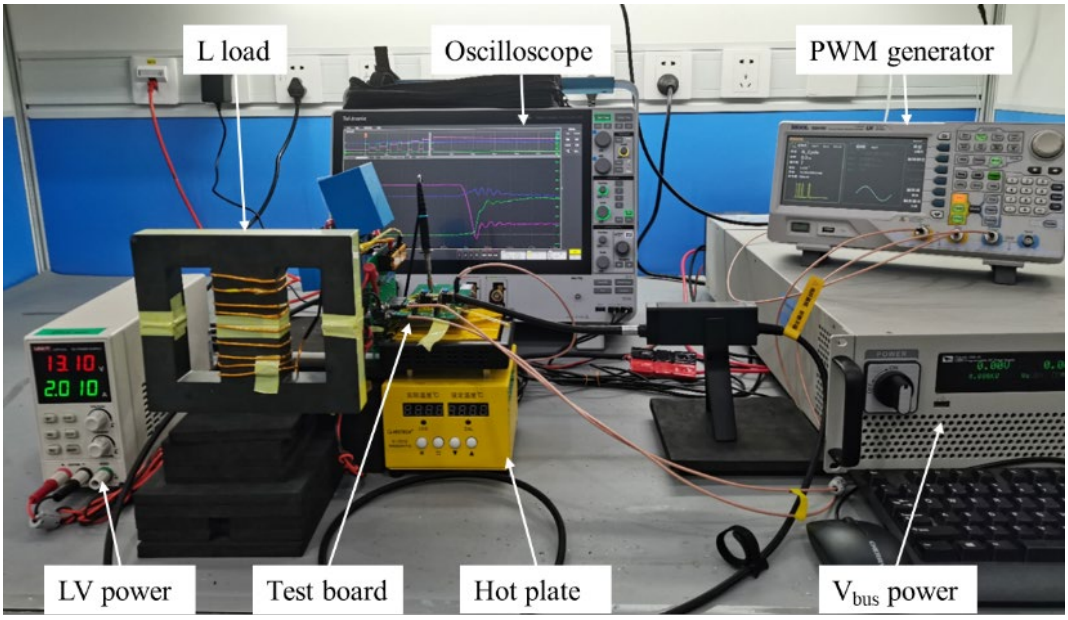

Fig. 4: Bench setup of the double-pulse test platform

Tables 1 and 2 provide detailed overviews of the absolute maximum ratings and pivotal electrical specifications of the G3F25MT06J SiC MOSFET, respectively [1]. In the experimental configuration, a bus voltage (V_{bus}) of 400V was utilized. All tests were conducted under two distinct gate turn-off voltage conditions: $V_{gs(off)}$ = 0V and $V_{gs(off)}$ = -3V, with the latter serving as a comparative reference. Notably, a significant number of G3F25MT06J devices were screened based on their threshold voltage characteristics.

Ultimately, the device exhibiting the lower threshold voltage of Vth(25C)=2.31 V and Vth(125C)=1.68V, which are closer to the minimum specification reported on the datasheet, was selected as the device under test to serve as the worst case for this analysis.

This meticulous experimental design ensures a robust framework for evaluating the PTO phenomenon in SiC MOSFETs, facilitating a deeper understanding of the intricate interplay between electrical parameters and device behavior.

Table 1 Absolute maximum rating values.

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µA	650	V
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +22	V
Gate-Source Voltage (Static)	$V_{GS(op)-ON}$ $V_{GS(op)-OFF}$	Recommended Operation	15 to 18 -5 to -3	V
Continuous Drain Current	I_D	T_C = 25°C, V_{GS} = -5 / +18 V T_C = 100°C, V_{GS} = -5 / +18 V T_C = 135°C, V_{GS} = -5 / +18 V	108 77 56	A
Pulsed Drain Current	$I_{D(pulse)}$	t_P ≤ 3µs, D ≤ 1%, V_{GS} = 18 V	175	A
Power Dissipation	P_D	T_c = 25°C	343	W
Non-Repetitive Avalanche Energy	E_{AS}	L = 36 mH, I_{AV} = 5 A	450	mJ
Operating Junction and Storage Temperature	T_j , T_{stg}		-55 to 175	°C

Table 2 Key electrical characteristic parameters.

Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	650			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V		1	100	µA
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 22 V V_{DS} = 0 V, V_{GS} = -10 V			100 -100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 15 mA	2.2	2.8	4.3	V
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 35 A V_{DS} = 10 V, I_D = 35 A, T_j = 175°C		19.2 19.3		S
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 18 V, I_D = 35 A V_{GS} = 18 V, I_D = 35 A, T_j = 175°C V_{GS} = 15 V, I_D = 35 A V_{GS} = 15 V, I_D = 35 A, T_j = 175°C		20.5 27 29 32	27.5	mΩ

4.1 Gate Resistance R_{g_Q2} of Q_2

Fig. 5 depicts the waveforms of the shoot-through current (I_{st}), the measured gate voltage (V_{gs}), and the turn-off current (I_{sd}) for the G3F25MT06J SiC MOSFET under the conditions of $V_{gs(off)}$ = -3 V and $V_{gs(off)}$ = 0 V. The green dashed line signifies the measured V_{th} of the G3F25MT06J. Notably, when $V_{gs(off)}$ is set to 0 V, the measured V_{gs} surpasses the V_{th} by 1V. Intriguingly, virtually no shoot-through current is observed under these circumstances. This observation highlights the limitation of relying solely on the measured V_{gs} to accurately predict the occurrence of the PTO, as discussed in detail in Section 3. Thus, additional metrics and methodologies may be necessary to comprehensively assess and mitigate PTO in SiC MOSFETs.

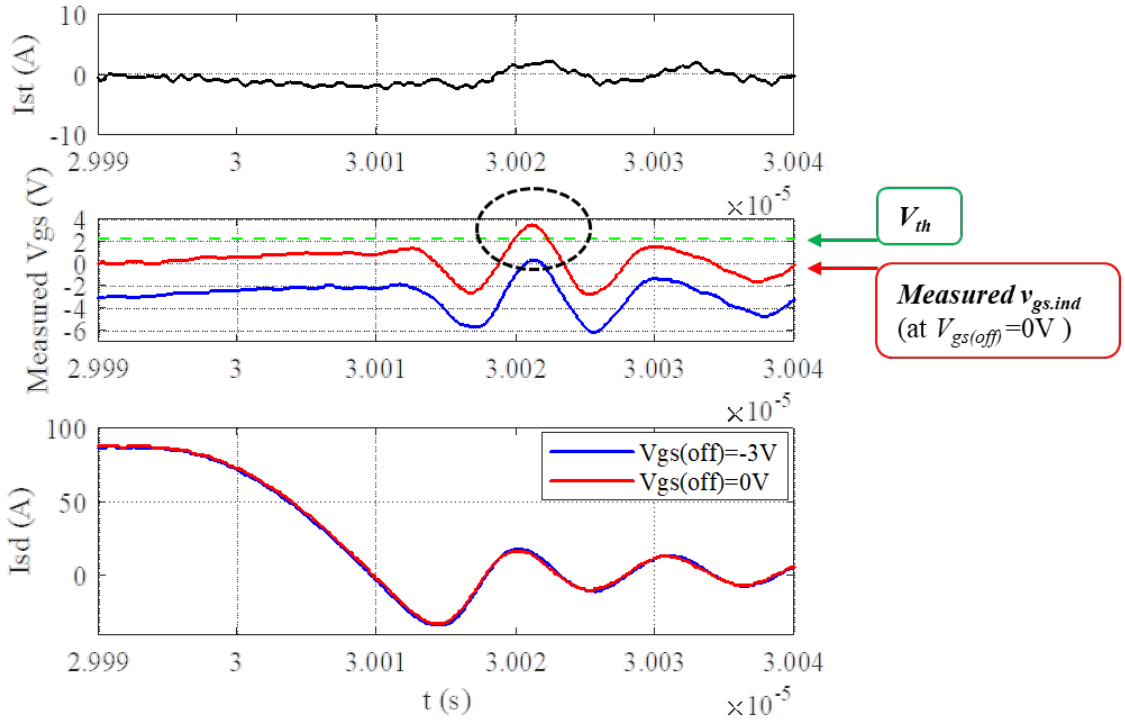

Fig. 5: Shoot-through current, measured $V_{gs(off)}$ and turn-off current waveforms of the G3F25MT06J. (V_{bus}=400 V, I_{sd}=88A, R_{g_Q1}=3.6Ω, R_{g_Q2}=0Ω, T_j=25 °C, $V_{gs(off)}$=0 V & -3 V)

The gate resistor R_{g_Q1} for device Q_1 is maintained at a constant value of 3.6Ω, whereas the gate resistor R_{g_Q2} for device Q_2 is varied to examine its influence on PTO. Fig 6 presents the waveforms of the I_{st} and the turn-off current (I_{sd}) for the G3F25MT06J SiC MOSFET across different values of R_{g_Q2}. Consistent with the analysis conducted in Section 3.1, R_{g_Q2} emerges as a pivotal factor in determining the occurrence and severity of PTO.

The experimental results illustrated in Fig 6 reinforce the theoretical insights presented in Section 3.1. As R_{g_Q2} increases, there is a corresponding augmentation in the severity of PTO. Specifically, when R_{g_Q2} is set to 0Ω, I_{st} remains minimal, indicating negligible instances of PTO. Conversely, with a gradual increase in R_{g_Q2}, I_{st} undergoes a substantial elevation, signifying a more pronounced manifestation of PTO.

Therefore, it is unequivocally concluded that a higher value of R_{g_Q2} correlates positively with an enhanced likelihood of PTO occurrence, thereby underscoring the importance of meticulously selecting gate resistor values to mitigate the risk of PTO in SiC MOSFET applications.

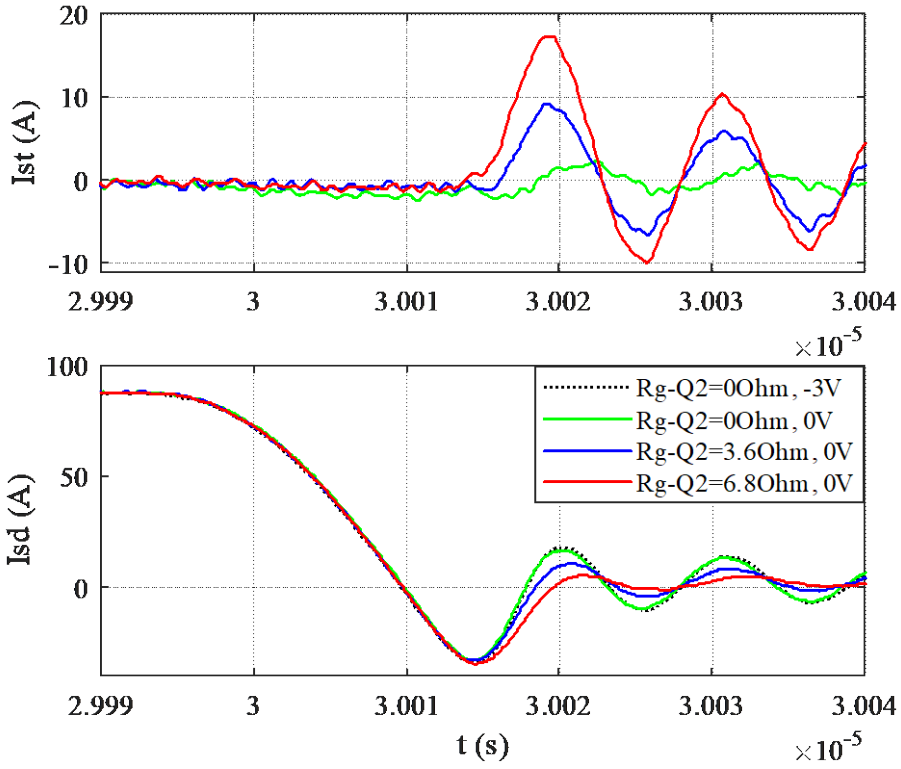

Fig. 6: Shoot-through current and turn-off current waveforms under different R_{g_Q2}. (V_{bus}=400 V, R_{g_Q1}=3.6Ω, T_j=25 °C, $V_{gs(off)}$=0 V)

4.2 Junction Temperature T_j

In the scenario where the gate resistance R_{g_Q1} for device Q_1 is fixed at 3.6Ω and the gate resistance R_{g_Q2} for device Q_2 is set to 6.8Ω, Fig. 7 exhibits the waveforms of the shoot-through current (I_{st}) and the turn-off current (I_{sd}) for the G3F25MT06J SiC MOSFET at various junction temperatures (T_j).

The graphical representation in Fig. 7 reveals a discernible trend: as the junction temperature T_j increases, the severity of parasitic turn-on (PTO) gradually intensifies. This phenomenon can be attributed to the decrease in the threshold voltage of SiC MOSFETs with rising T_j, which facilitates the occurrence of PTO.

From a practical engineering standpoint, the prolonged persistence of I_{st} leads to considerable additional losses, impacting the efficiency and reliability of the system. These losses can manifest as increased heat generation, potentially leading to thermal runaway and premature failure of the SiC MOSFETs.

Hence, it is conclusively established that the likelihood of PTO increases under conditions of elevated junction temperatures T_j. This understanding underscores the importance of considering temperature effects in the design and operation of SiC MOSFET-based circuits to minimize the risk of PTO and associated losses.

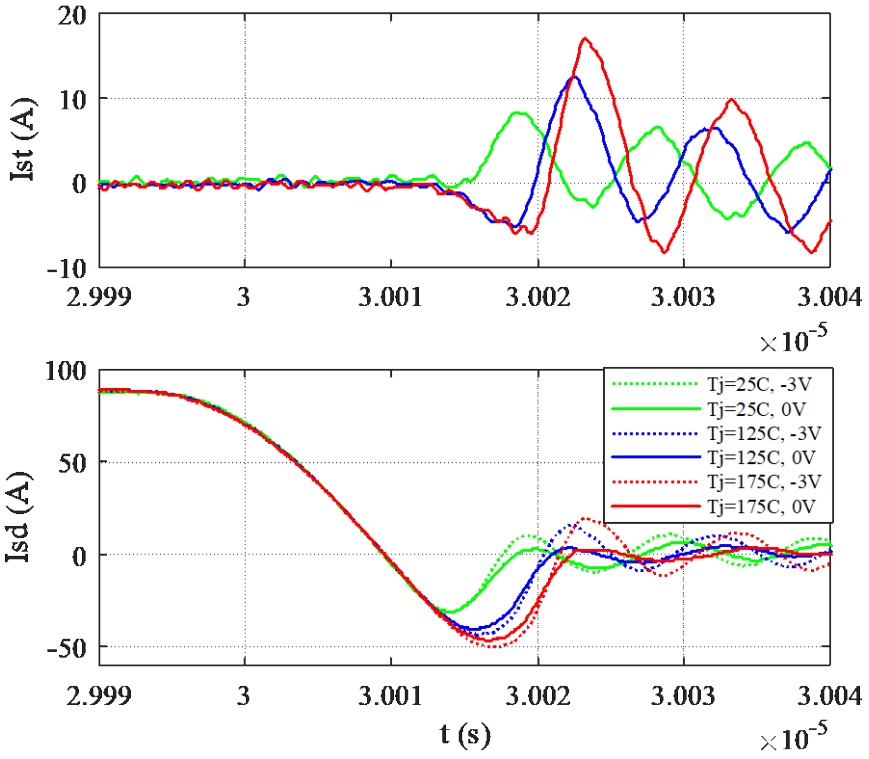

Fig. 7: Shoot-through current and turn-off current waveforms under different T_j (V_{bus}=400 V, R_{g_Q1}=3.6Ω, R_{g_Q2}=6.8Ω, $V_{gs(off)}$=0 V & -3 V)

4.3 Drain-Source Voltage Rising Speed of Q_2

Fig. 8 illustrates the waveforms of the shoot-through current (I_{st}) and the turn-off current (I_{sd}) for the G3F25MT06J SiC MOSFET, showcasing the impact of varying gate resistances R_{g_Q1}. The theoretical underpinning suggests that lower values of R_{g_Q1} result in a more rapid increase in the drain-source voltage rising speed (dv_{ds}/dt) of Q2, as evident in Fig. 8. This acceleration in dv_{ds}/dt can exacerbate the conditions conducive to PTO.

The experimental data presented aligns with these theoretical predictions. Specifically, as R_{g_Q1} decreases, the I_{st} waveform indicates a more pronounced PTO event, confirming that smaller gate resistances indeed enhance the likelihood of PTO.

This correlation between R_{g_Q1} and the occurrence of PTO underscores the critical role of gate resistor selection in SiC MOSFET-based circuits. By carefully tuning R_{g_Q1}, engineers can mitigate the risk of PTO, thereby enhancing the performance and reliability of their systems. This understanding is particularly pertinent in applications where rapid switching and high efficiency are paramount, such as in electric vehicle powertrains and renewable energy converters.

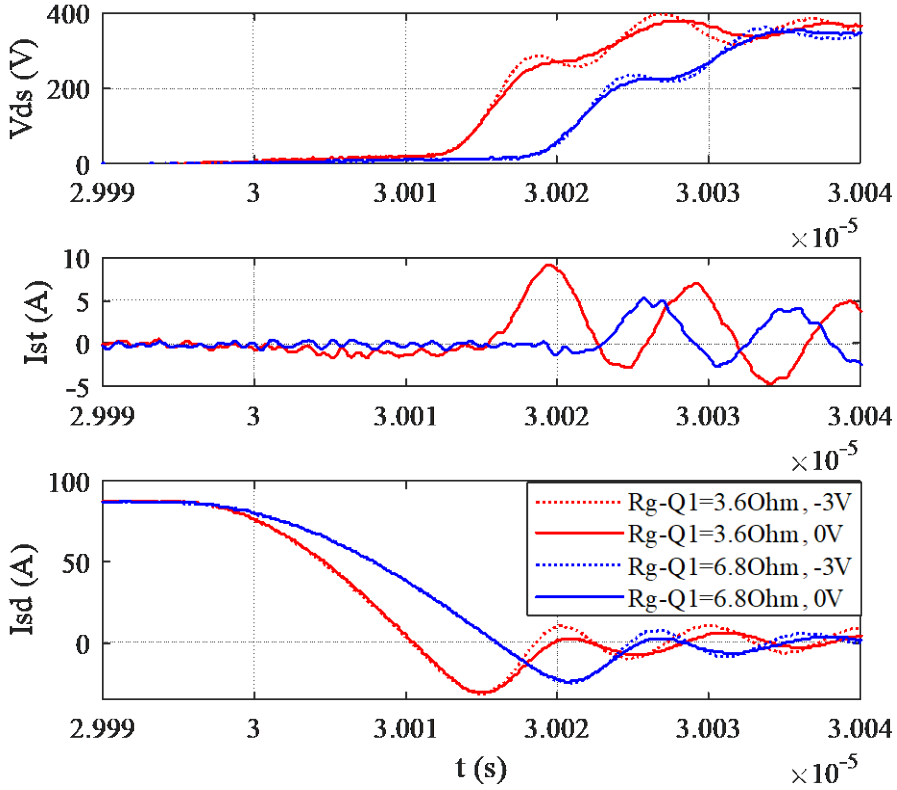

Fig. 8: Shoot-through current and turn-off current waveforms under different R_{g_Q1} (V_{bus}=400V, R_{g_Q2}=6.8Ω, T_j=25 °C, $V_{gs(off)}$=0V & -3V)

5. Advantages of Navitas' Gen3 'Fast' Trench-Assisted Planar SiC MOSFETs

To highlight the superior attributes of Navitas' Gen3 'Fast' Trench-Assisted Planar SiC MOSFETs, a comparative analysis was conducted with two additional planar SiC MOSFETs Gen3 'Fast' Trench-Assisted Planar. Table 3 delineates the key electrical specifications of the three SiC MOSFETs under consideration. A rigorous screening process was implemented, focusing on the threshold voltage characteristics of the G3F25MT06J devices.

Consequently, the device exhibiting the lowest threshold voltage values, specifically V_{th}(25°C) = 2.31V and V_{th} (125°C) = 1.68 V, was chosen for further examination. This device was deemed representative of the worst-case scenario for the analysis, ensuring a conservative and rigorous assessment of the parasitic turn-on (PTO) phenomenon in SiC MOSFETs.

Table 3 Key electrical characteristic parameters

DUT		NVTS	Vendor A	Vendor B
Technology		Trench-Assisted Planar	Planar	Planar
Package		TO-263-7	TO-263-7	TO-263-7
Vds.max		650V	650V	650V
Vgs(on)		+18V	+15V	+18V
Vth (typ.)	**25℃**	2.8V	2.3V	2.8V
	125℃	2.25V	2.0V	—
Vth (DUT)	**25℃**	2.31V	2.32V	2.78V
	125℃	1.68V	1.99V	2.28V

The gate charge characteristics of the three investigated devices are presented in Fig. 9. Upon examination of these results, it becomes evident that the NVTS G3F25MT06J device exhibits the smallest *Qgd* value. The comparison results of the parameters *Qgd/Qgs* are displayed in Table 4. Notably, the *Qgd/Qgs* ratio of 0.536 for the NVTS G3F25MT06J device is lower compared to 0.768 and 0.714 reported for the devices from Vendors A and B, respectively, representing 30% and 25% reduction. This lower *Qgd/Qgs* ratio is advantageous in mitigating the Miller effect during the switching process, ultimately leading to enhanced switching speed and reduced switching losses.

Table 4 The parameter *Qgd/Qgs* comparison results for three DUTs
(V_{bus}=400 V, *Ids*=40A, T_j=25°C)

	NVTS	Vendor A	Vendor B
Qgd	18.267 nC	23.618 nC	19.978 nC
Qgs	34.080 nC	30.752 nC	27.981 nC
Qgd/Qgs	0.536	0.768	0.714

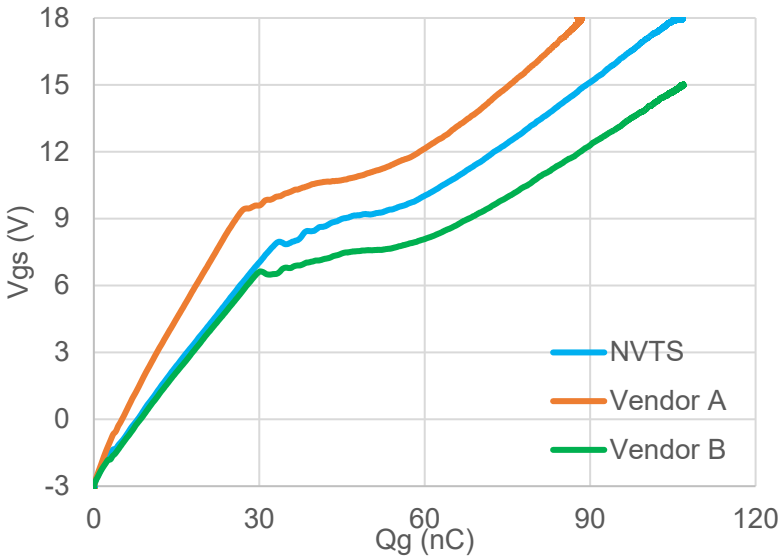

Fig. 9: The typical gate charge characteristics for three DUTs
(V_{bus}=400 V, Ids=40A, T_j=25 °C)

Furthermore, the charge Q_{st} and the generated loss $P_{d.st}$ are calculated as:

$$Q_{st} = \int I_{st} \cdot t \tag{5}$$

$$P_{d.st} = V_{bus} \cdot Q_{st} \cdot f_{sw} \tag{6}$$

where f_{sw} is the switching frequency (f_{sw} =75kHz in this paper).

An in-depth comparative analysis of the PTO generated losses ($P_{d.st}$) and drive resistance values at specific operating conditions of 400V and 80A, with a turn-off gate voltage of 0V, is provided in Fig. 10 and Table 5. Notably, the NVTS G3F25MT06J device demonstrates the lowest $P_{d.st}$ and minimal PTO compared to Vendor A and Vendor B under these identical test conditions. This suggests that the NVTS device offers superior performance in terms of reducing losses and mitigating PTO, which are critical factors in achieving efficient and reliable power conversion.

Table 5 Partial $P_{d.st}$ comparison results for three DUTs
(R_{gon}=4R, T_j=25°C)

	R_{goff}=0R	R_{goff}=3R6	R_{goff}=6R8
NVTS	0.437W	0.926W	1.979W
Vendor A	0.637W	3.395W	7.658W
Vendor B	1.842W	4.508W	6.806W

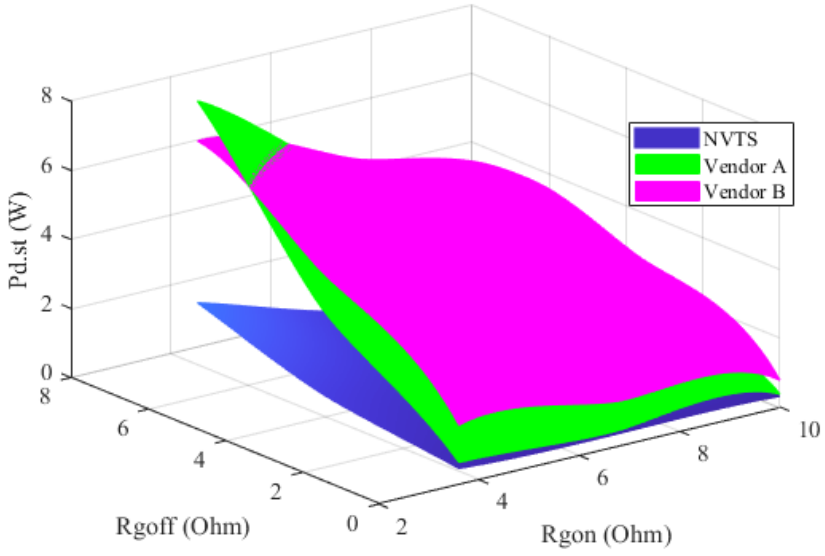

Fig. 10: The relationship between $P_{d.st}$ and drive resistance values at 25C

Fig. 11 and Table 6 further elaborate on the relationship between $P_{d.st}$ and drive resistance values for the NVTS G3F25MT06J device under varying junction temperatures (T_j). The experimental results reveal that the $P_{d.st}$ remains below 1W when the turn-off gate resistance (R_{goff}) is set to 0Ω and the turn-on gate resistance (R_{gon}) ranges from 3.6Ω to 10Ω. This finding is particularly significant as it provides a practical guide for selecting appropriate drive resistance values when implementing 0V gate voltage turn-off in engineering applications.

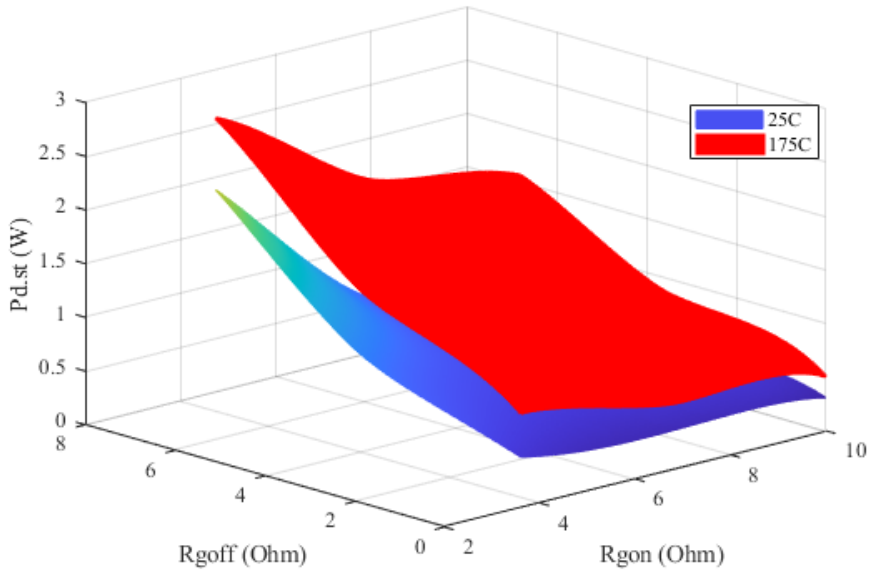

Fig. 11: The relationship between $P_{d.st}$ and drive resistance values under different T_j

Table 6 The generated loss $P_{d.st}$ comparison results under different T_j

	R_{gon}=4R			R_{gon}=6R		
	R_{goff}=0R	R_{goff}=1R	R_{goff}=2R	R_{goff}=0R	R_{goff}=1R	R_{goff}=2R
25℃	0.437W	0.575W	0.680W	0.360W	0.465W	0.523W
175℃	0.871W	1.149W	1.288W	0.675W	0.910W	1.060W

By adhering to this matching relationship, engineers can optimize the performance of SiC MOSFET-based circuits by minimizing losses and ensuring stable operation. This understanding is essential for the development of high-efficiency power converters and other power electronics systems, where minimizing losses and maintaining reliability is paramount. Overall, the presented data serves as a valuable reference for drive resistance selection in practical engineering applications utilizing 0 V gate voltage turn-off.

6. Conclusion

This application note presents an experimental analysis of the factors influencing PTO in the G3F25MT06J SiC MOSFET device. The study focuses on three key parameters: gate turn-off resistance, junction temperature, and drain-source voltage rising speed. The experimental results offer valuable insights into how these factors interact to affect PTO.

Firstly, it is observed that an increase in gate turn-off resistance exacerbates PTO. This finding highlights the importance of carefully selecting the gate resistance to minimize the risk of PTO and ensure stable operation of the SiC MOSFET.

Secondly, the study reveals that junction temperature also plays a significant role in PTO. As the junction temperature rises, the likelihood of PTO increases. This underscores the need for effective thermal management strategies to maintain the junction temperature within safe limits and prevent PTO.

Lastly, the application note demonstrates that the drain-source voltage rising speed is another critical factor influencing PTO. A faster-rising speed leads to a higher likelihood of PTO, emphasizing the importance of controlling the *dv/dt* during switching to mitigate PTO.

Based on these experimental results, the study establishes a clear relationship for matching drive resistance, which is crucial for the reliable operation of SiC MOSFETs with a 0V turn-off gate voltage. This matching relationship provides essential guidance for engineers in selecting the appropriate driving resistance to maintain operational reliability. By adhering to these guidelines, engineers can optimize the performance of Navitas' trench-assisted planar SiC MOSFET-based circuits and ensure their stable and efficient operation in various applications.

References

1. https://navitassemi.com/wp-content/plugins/gb-navitas-stock-checker/product_files/G3F25MT06J.pdf

Appendix

Table 7 Navitas' 650 V Gen3 'Fast' Trench-Assisted Planar SiC MOSFETs

Part No.	Rdson (mW)	Id_DC (A) @25C	Package	Datasheet
G3F25MT06L	20.5	125	TOLL	G3F25MT06L
G3F33MT06L	28.5	90	TOLL	G3F33MT06L
G3F33MT06J	28.5	80	TO-263-7	G3F33MT06J
G3F45MT06L	42	61	TOLL	G3F45MT06L
G3F45MT06J	42	39	TO-263-7	G3F45MT06J
G3F60MT06L	55	48	TOLL	G3F60MT06L
G3F60MT06J	55	31	TO-263-7	G3F60MT06J

Additional Information

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