Board Assembly Guidelines for TOLT package

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1. Introduction

This application note provides guidelines for the handling and board mounting of Navitas' TOLT package including recommendations for printed-circuit board design and heatsink considerations. Information on heatsink and thermal interface material considerations is also provided as guidance for customer-specific thermal simulations.

2. Scope

This application note contains information on actual board mounting conditions including board design as validated by Navitas Semiconductor. Optimization of the board assembly process is still required to ensure a reliable solder joint on components within the board. IPC and JEDEC Industry standards including best practices in the board assembly environment are good references to fine-tune board design and mounting process. Heatsink and thermal interface material (TIM) stack-up references are added in this document for consideration in optimizing thermal structures in actual applications.

3. TOLT Package

3.1 Package Description

TOLT (TO-Leaded Top-side cooling package) is a surface mount gull-wing type plastic package. This is a thermally-enhanced SMD configured for top-side heat dissipation to enable the highest power densities and with gull-wing leads for superior board-level reliability. HDSOP-16 is the registered package designator under JEDEC.

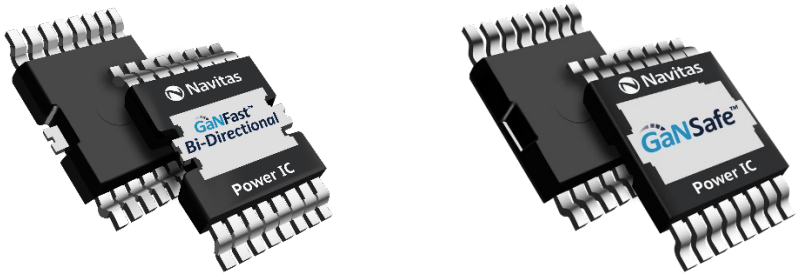
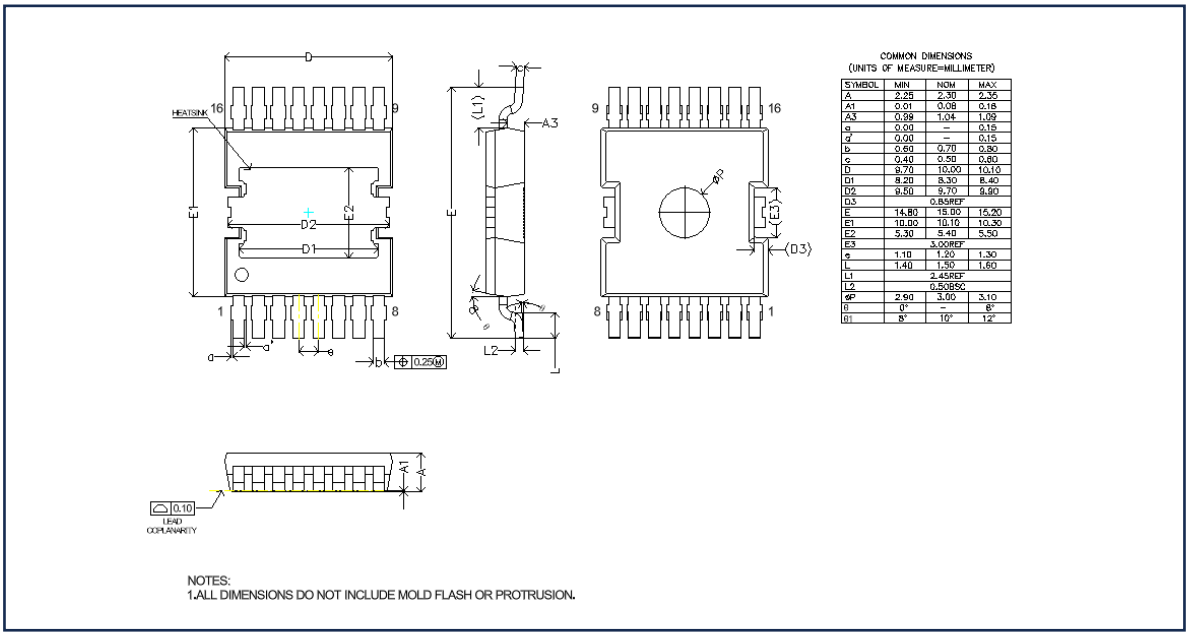


Fig. 1: Navitas TOLT 16L Package (GaNFast™ Bi-Directional & GaNSafe™)

3.2 Package Dimension

The package is designed with a negative stand-off and the top exposed pad is plated with Ni-NiP. These package features guarantee flatness on the top surface (See Figures 2 & 3) after board mounting which is critical for heatsink mounting on applications requiring optimum thermal benefit. The TOLT Package Outline drawing with dimension details as shown, must be referred to when designing the PCB layout:



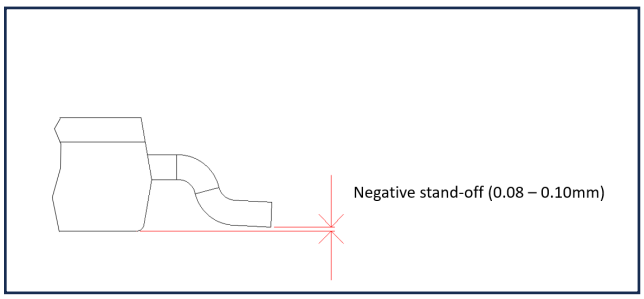


Fig. 2: Negative Stand-off

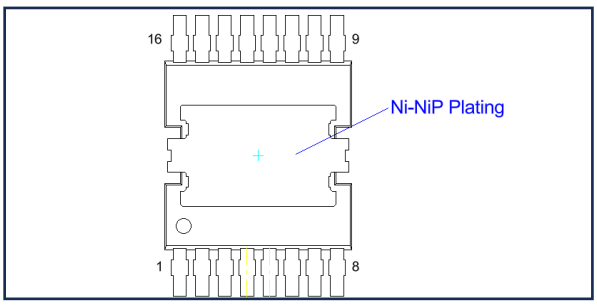


Fig. 3: Top Exposed Plating

4. PCB Guidelines

4.1 PCB Layout

PCB layout is critical for proper operation of the power IC and thermal management. Recommended Cu pad dimensions and stencil tooling will ensure sufficient solder coverage between the package and the Printed Circuit Board (PCB).

The following rules should be followed carefully during the design of the PCB layout:

• Do not run power SOURCE current through the SK pin.

• System-level thermal design for top-cooled packages must observe co-planarity and electrical isolation requirements when multiple power devices are cooled by the same heatsink (Cold Plate). Since the majority of heat is transferred through the top-side thermal pad, placing a Cu pad below the package is optional unless used as added mechanical support. Caution has to be taken when adding a Cu pad under the package as this will add to the stand-off variation of the package that may affect soldering quality. Fig. 4 shows the pad layout without the Cu pad under the package while Fig. 5 shows the layout with Cu pad under the package. Note however that the maximum allowable Cu pad thickness is based on a 2oz Cu board design.

• Refer to the device datasheet for other layout requirement to optimize performance of the device.

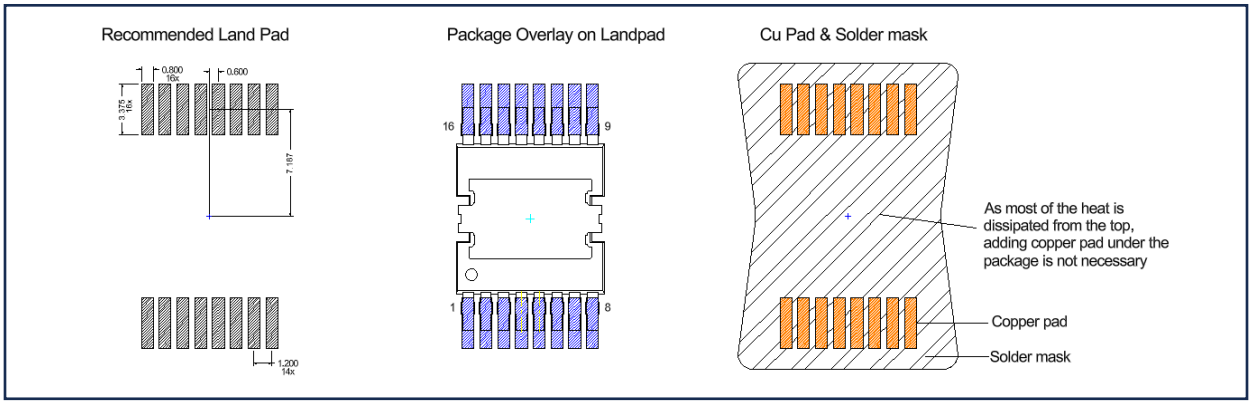


Fig. 4: Recommended Land Pad Layout (without Cu pad under the package)

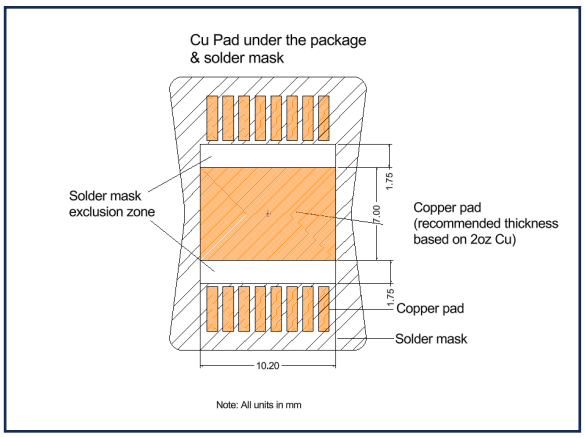


Fig 5: Recommended Land Pad Layout with Cu pad under the package

5. Board Assembly

5.1 Stencil Design

A proper PCB layout and stencil design is critical to ensure the quality of the surface mount assembly and subsequent electrical and mechanical performance of the mounted package in its final application. The negative stand-off dimension of the package requires a thicker stencil to create an appropriate solder connection to the device pins. Good results can be achieved with a 200 µm stencil thickness on recommended footprints. Refer to Fig. 6 for the recommended stencil aperture opening dimensions used by Navitas in actual board mount studies. A typical solder connection of the TOLT package using SAC305 alloy (Indium 8.9HF/T4 with 88.5% metal loading) with 200 µm stencil thickness is shown in Fig 7.

For board designs requiring smaller components with finer pitch besides the TOLT package, the stencil thickness can be adjusted to accommodate both TOLT and smaller components. Equivalent stencil thickness for TOLT package must be at 150 µm minimum. Step-stencil can also be an option to consider. Final mounted units need to be checked to ensure proper solder coverage and fillet formation on the leads.

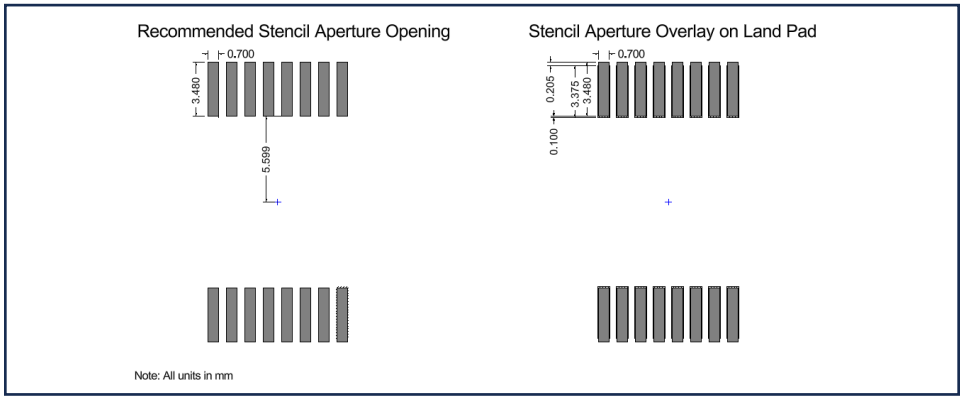


Fig. 6: Recommended stencil design

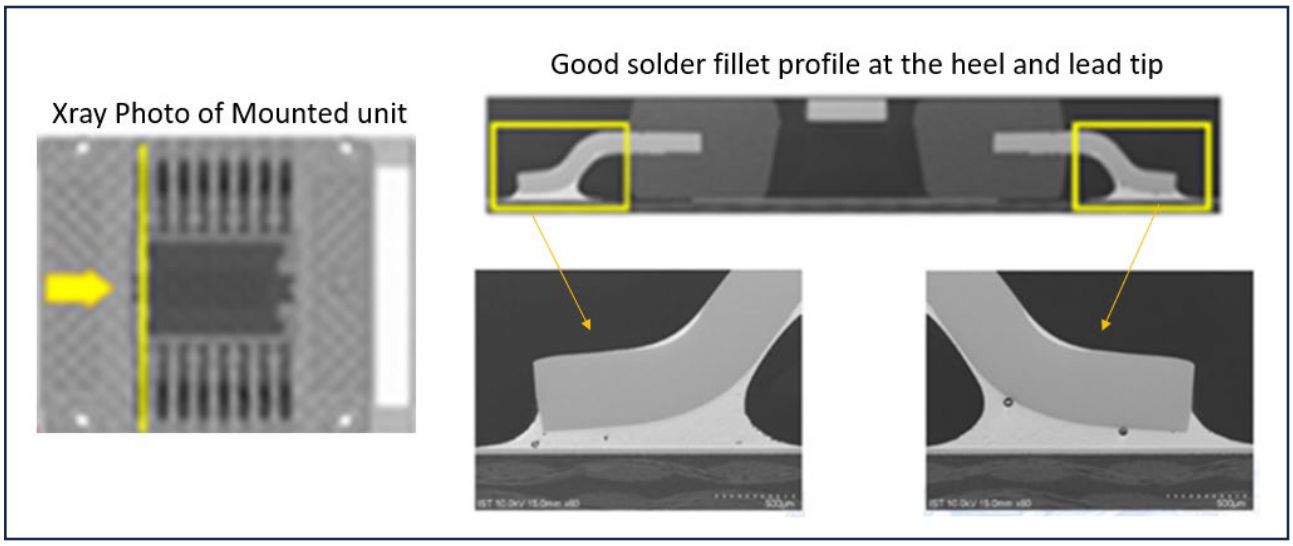


Fig. 7: Cross-section Photo of TOLT package after board mounting

5.2 Recommended Reflow Profile

The recommended reflow profile is normally provided by the solder paste suppliers. Actual temperature measurements on various locations within the PCB are needed to ensure components are subjected to temperatures within the recommended guideline in Fig 8.

Recommended reflow time and temperature:

	Pb-free Solder Profile
Minimum Soak Temperature	150°C
Maximum Soak Temperature	200°C
Soak Time	60 - 120 seconds
Liquidous Temperature	217°C
Time Above Liquidous	60 - 150 seconds
Peak Package Body Temperature	245°C (T2Pak, TO-263) 260°C (TOLL, TOLT, TO-252, QFN)
Max Ramp Up Rate - Liquidous to Peak	3°C / second max
Time at Peak Temperature (+/- 5°C)	30 seconds
Max Ramp Down Rate - Peak to Liquidous	6°C / second max

Typical Reflow profile for surface-mount components:

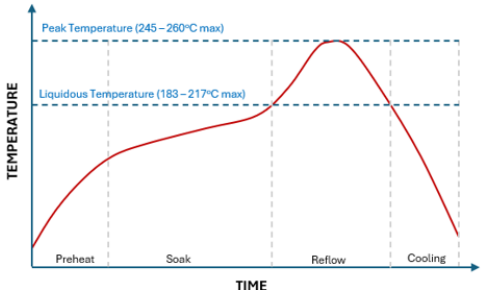
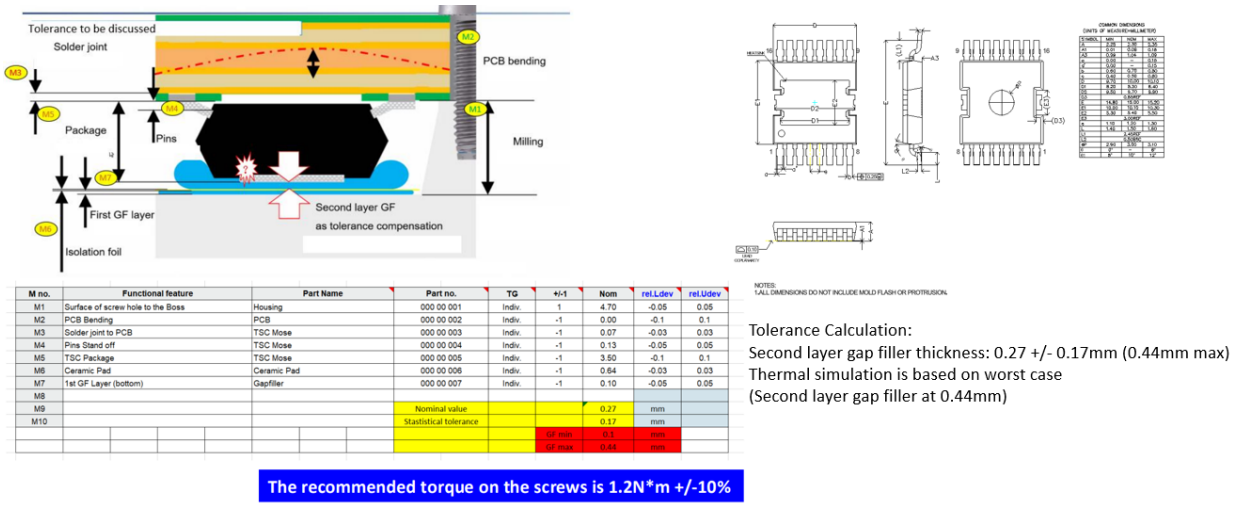


Fig. 8: Recommended reflow time and temperature

6. Heatsink & TIM Considerations

Thermal interface materials (TIMs) are being used to improve the contact between the component and the heatsink. Given the rough surfaces of the component and the heatsink, there will be air gaps between the interfaces that will limit heat dissipation. The use of thermally conductive interface material fills this gap, thus, improving heat transfer from the package to the heat dissipating component. The thickness of TIM) is a critical parameter to ensure good dissipation of heat from the package to the heatsink. Screws are provided to help anchor the package to the board while consistently dissipating heat through the heatsink. Bending of the PCB normally happens due to thermal cycling conditions encountered by the board in actual application. Recommended torque on

the screw is 1.2N*m (+/-10%). Fig 9 shows the computation for worst-case TIM thickness at 440 µm considering all stack tolerances.



M no.	Functional feature	Part Name	Part no.	TG	+/-1	Nom	rel.Ldev	rel.Udev
M1	Surface of screw hole to the Boss	Housing	000 00 001	Indiv.	1	4.70	-0.05	0.05
M2	PCB Bending	PCB	000 00 002	Indiv.	-1	0.00	-0.1	0.1
M3	Solder joint to PCB	TSC Mose	000 00 003	Indiv.	-1	0.07	-0.03	0.03
M4	Pins Stand off	TSC Mose	000 00 004	Indiv.	-1	0.13	-0.05	0.05
M5	TSC Package	TSC Mose	000 00 005	Indiv.	-1	3.50	-0.1	0.1
M6	Ceramic Pad	Ceramic Pad	000 00 006	Indiv.	-1	0.64	-0.03	0.03
M7	1st GF Layer (bottom)	Gapfiller	000 00 007	Indiv.	-1	0.10	-0.05	0.05
M8								
M9			Nominal value			0.27	mm	
M10			Stastistical tolerance			0.17	mm	
					GF min	0.1	mm	
					GF max	0.44	mm	

Tolerance Calculation:
Second layer gap filler thickness: 0.27 +/- 0.17mm (0.44mm max)
Thermal simulation is based on worst case
(Second layer gap filler at 0.44mm)

The recommended torque on the screws is 1.2N*m +/-10%

Fig. 9: Heatsink Mounting Tolerance Calculation

A schematic view of the layers in contact to the package up to the housing shows varying thermal properties per layer that is affecting the efficiency of heat dissipation from device to the heatsink. From this thermal management structure (Fig 10), the Rth case-coolant should be within 1.4 K/W.

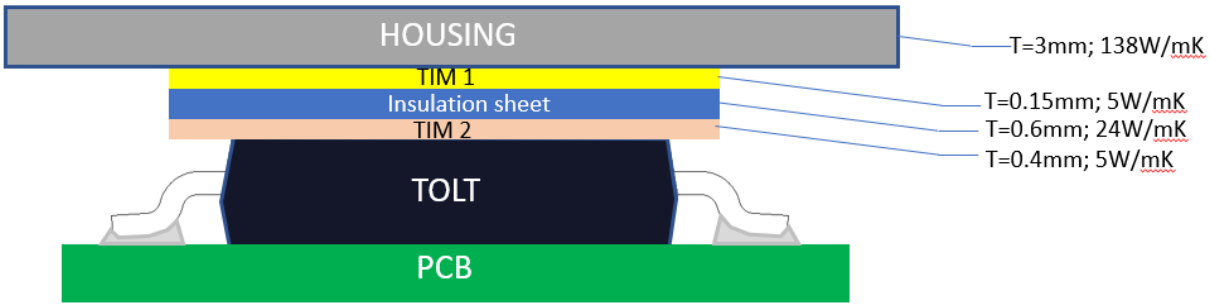


Fig. 10: Thermal Management Structure

Additional Information

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Contact: info@navitassemi.com