Design Guide for AHB Circuit With Controller NV9801

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1. Introduction

NV9801 is an Asymmetrical Half-Bridge (AHB) flyback controller that can implement high-efficiency and high-density AC/DC power supplies.

The whole control strategy contains four operation modes, namely ZSM/VSM/DCM/Burst mode, to achieve better conversion efficiency in each load segment.

When the system works under heavy load, NV9801 realizes zero-voltage turn-on of the main FET by adaptively controlling the conduction width of the auxiliary FET.

As the load decreases, NV9801 works in VSM mode. In this mode, the current magnetizing inductor is discontinuous. By the unique valley turn-on control, NV9801 can minimize the switching loss.

As the load decreases further, NV9801 will enter DCM mode. In this mode, the chip only retains valley turn-on control due to the very low switching frequency.

If the output load is extremely light, the chip will enter burst mode. In this mode, most of the block circuits of NV9801 are disabled to save quiescent current and thus reduce the standby power loss of the system.

Together with GaNSense™ technology (loss-less current sensing), NV9801 provides higher system reliability and better system efficiency.

2. Product Highlights

Operation Mode

- Zero-voltage switch mode (ZSM) at heavy load
- Valley-voltage switch mode (VSM) at middle load
- Discontinuous conduction mode (DCM) at light load
- Burst mode at extremely light load/standby operation

Power Supply

- Built-in high voltage start-up function
- Integrated Boost power supply for VCC
- Integrated LDO for half-bridge
- Integrated power switch for PFC stage power supply

Key Features

- X-Capacitor discharge
- PFC enable/disable control
- Built-in Main FET soft start
- Resonant valley lock in VSM mode
- Peak current jitter for better EMI performance
- Programmable resonant period
- Slope compensation during high duty-cycle switching
- High switching frequency up to 1MHz

Protection

- Brown-in/out
- CS pin open/short protection
- Output overload protection
- Output OVP/UVP
- Auxiliary FET I_{SAT} protection
- Programmable external over-temperature protection
- Short-circuit protection

Package

- SOP14

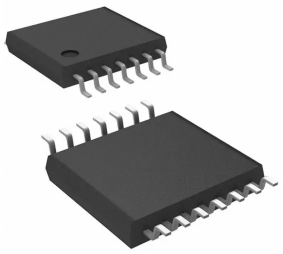


Fig. 1: Package SOP14

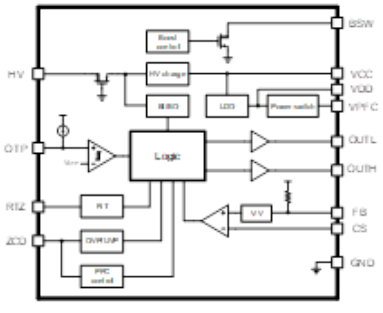


Fig. 2: Simplified schematics

3. AHB Circuit Operation Principle

3.1 AHB Topology Operating Mode

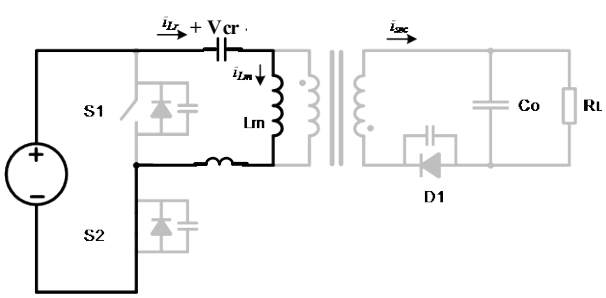


Fig. 3: working mode1

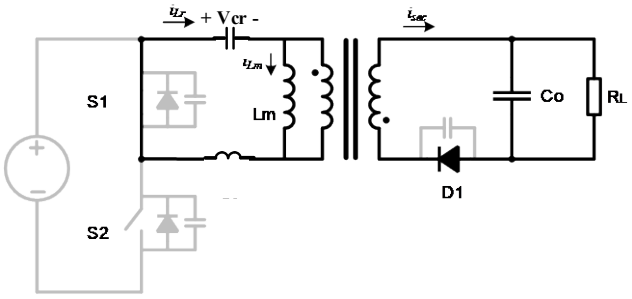


Fig. 4: working mode2

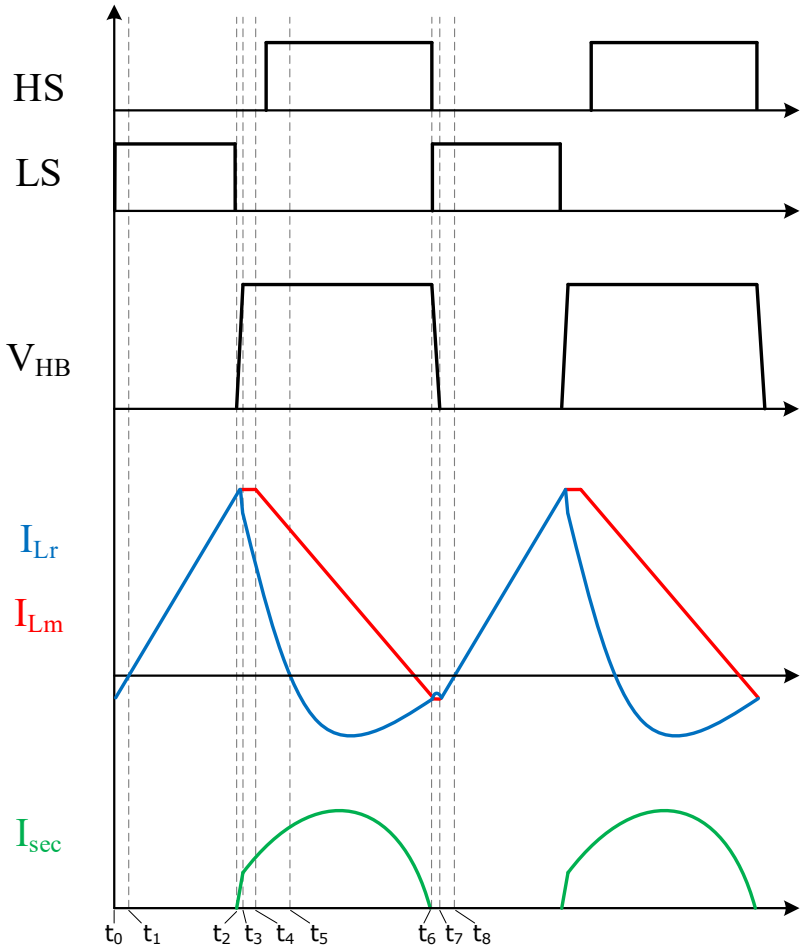


Fig. 5: working waveform

[1] Due to the volt-second balance of Lm:

$$\frac{1}{T}\int_0^T v_{Lm}dt = 0$$

So we could obtain:

$$\frac{V_{in}-V_{cr}}{L_m+L_r}DT = \frac{V_{cr}}{L_m+L_r}(1-D)T \quad \Rightarrow:$$

$$v_{cr} = DV_{in}$$

When S1 turn on and Lm>>Lr:

$$V_{out} = \frac{L_m}{L_m+L_r}\frac{v_{cr}}{n} \approx \frac{v_{cr}}{n}$$

So we could obtain the gain equation for Vin and Vout:

$$V_{out} = \frac{DV_{in}}{n}$$

[2] Due to the ampere-second balance of Cr:

$$\frac{1}{T}\int_0^T i_{Cr}dt = 0$$

So, we could obtain:

$$\frac{1}{T}\int_0^T i_{Lm} - \frac{i_{sr}}{n}dt = 0 \quad \Rightarrow:$$

$$\int_0^T i_{Lm}dt = \int_0^T \frac{i_{sr}}{n}dt$$

$$I_{Lm\_av} = \frac{1}{T}\int_0^T i_{Lm}dt = \frac{1}{T}\int_0^T \frac{i_{sr}}{n}dt = \frac{I_{out}}{n}$$

So, we could obtain the average current equation between I_{Lm} and I_{out}:

$$I_{out} = n\frac{I_{Lm\_\max} + I_{Lm\_\min}}{2}$$

4. NV9801 Peripheral Circuit Design

4.1 Pin Configuration

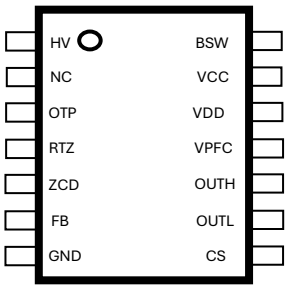


Fig. 6: NV9801 pinout

Pin		I/O	Description
Number	Symbol		
1	HV	P	High voltage start-up pin for the IC. It also implements X-cap discharge and BI/BO functions at the same time.
2	NC		No connection.
3	OTP	I/O	External temperature sensing pin. Connecting an NTC resistor in series with a normal resistor to this pin to set the appropriate temperature protection threshold. It also determines the selection of high/low frequency applications.
4	RTZ	I/O	Set the resonant period of SW node. Also, it can set dead time from OUTH turn off to OUTL turn on at the same time.
5	ZCD	I/O	Auxiliary winding voltage sensing pin. It has multiple functions, such as OVP/UVP protection, PFC boost control, etc. Also, it decides when to turn off OUTH at the same time.
6	FB	I/O	Feedback voltage from opto-coupler connected pin. The voltage is used to implement whole control loop and operation mode switching.
7	GND	G	Ground pin.
8	CS	I	Current sensing pin. Connecting to the sensing resistor of the transformer to implement peak current mode control loop.
9	OUTL	I/O	Main FET driving signal output pin. Besides, it combines OUTH ISAT protection at the same time.
10	OUTH	O	Auxiliary FET driving signal output pin.
11	VPFC	P	PFC boost power supply.
12	VDD	P	LDO output pin for half bridge driver IC power supply.
13	VCC	P	Power supply pin for IC.
14	BSW	P	Switching node voltage input pin of the Boost power supply circuit.

(1) I=Input, O=Output, P=Power, G=Ground

4.2 Peripheral Circuit Design

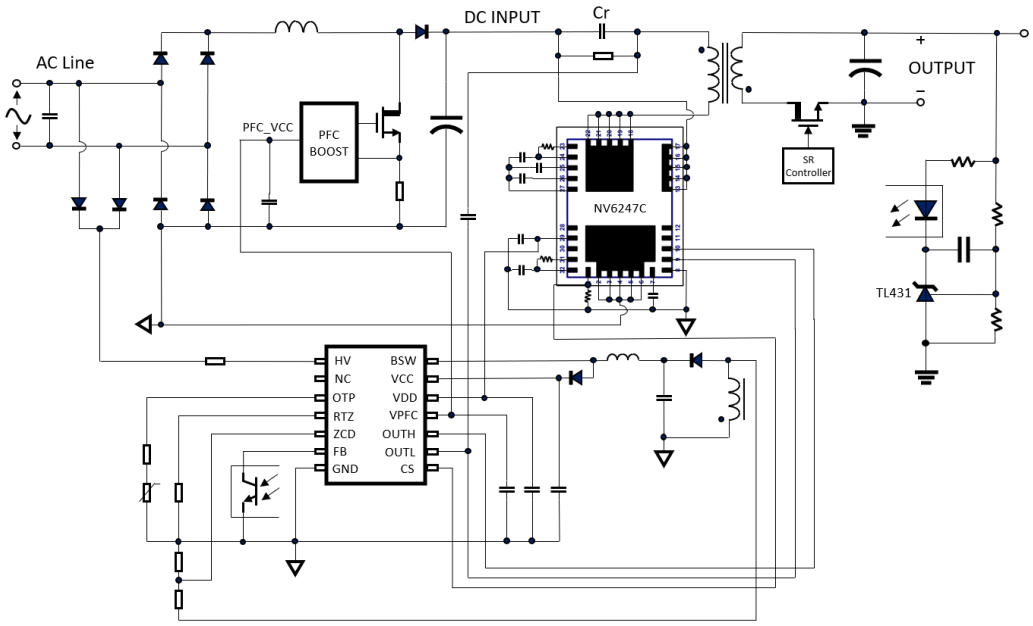
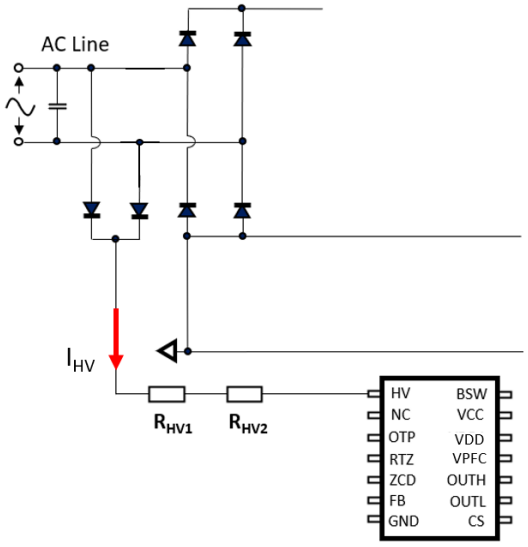


Fig. 7: application schematic

1. HV Pin BI/BO Detection



1) Function: High voltage start-up pin for the IC. It also implements X-cap discharge and BI/BO functions at the same time.

I_{HV_BI}	HV Current Threshold for Brown in	1.1	1.17	1.25	mA	
I_{HV_BO}	HV Current Threshold for Brown out	0.92	1	1.08	mA	
T_{DEB_BO}	Debounce Time for Brown-Out	36	40	44	ms	

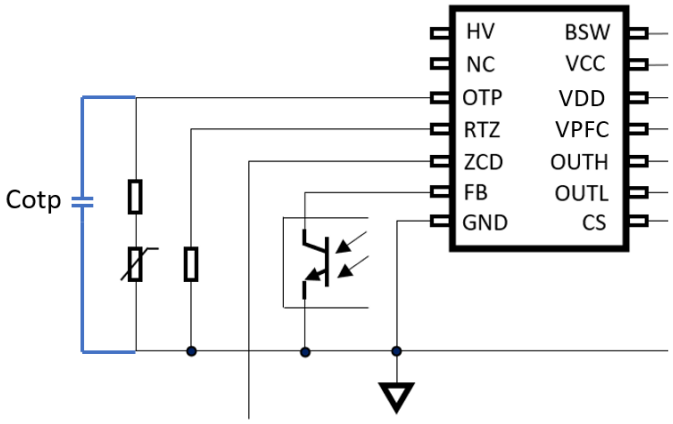
2) Brown-in setting voltage: V_{BI}=1.17mA*(R_{HV1}+ R_{HV2})

Brown-out setting voltage: V_{BO}=1.0mA*(R_{HV1}+ R_{HV2})

3) BI condition: Detect I_{HV} every 2 ms until I_{HV}>1.17mA is detected

4) BO condition: Detect I_{HV}<1mA and debounce for 40ms

2. OTP Pin



1) Function: External temperature sensing pin. And it combines the selection of high/low frequency applications.

2) NV9801 OTP pin provides 60μA current

3) Trigger OTP: V_{otp} is below 0.55V for 100μs

4) Use C_{otp} to set low frequency or high frequency

If F_{sw} >300kHz, it needs to place C_{otp} and C_{otp} > 2.2nF

If F_{sw}<300kHz, C_{otp} is not required

3. RTZ Pin

1) Function: RTZ pin is used to set a reference time referring to the resonant time after ILM cross zero.and Also, it can set dead time from OUTH turn off to OUTL turn on at the same time.

2) The larger is the RTZ, the smaller the Ineg will be.

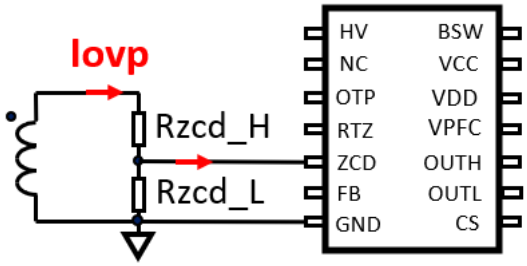
The smaller is the RTZ, the greater the Ineg will be.

3) For low frequency application; Rtz = Tring/5*0.8 to achieve good ZVS result.

For high frequency application; Rtz = Tring/5 to avoid larger Ineg.

T_{ring}: the resonance period of Lm and equivalent capacitance

4. ZCD PIN – Output ovp



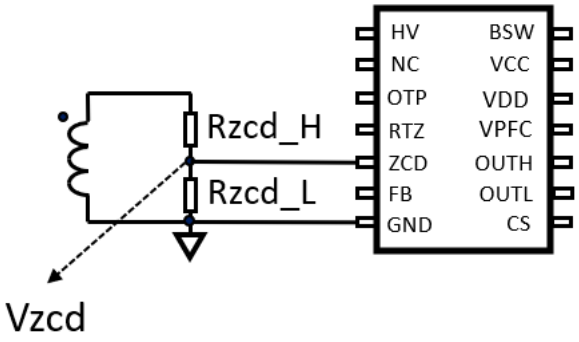
1) Function: ZCD pin can be be used to detect Output OVP.

When NV9801 starts to detect OVP, Rzcd_L will be shorted to GND. And it will detect the Iovp through Rzcd_H

$$V_{OUT\_OVP} = 500\mu A \times R_{zcd\_H} \cdot \frac{N_S}{N_A}$$

2) Trigger condition: 3 cycles to trigger during the on-time of OUTH

5. ZCD PIN – Output uvp and PFC EN



1) Function: ZCD pin can be used to detect Output UVP and enable PFC stage.

When OUTL turns off, NV9801 starts to detect Vzcd

And If Vzcd < 0.25V for 3cycles, it will trigger UVP

And If Vzcd > 1V for 1cycle, it will immediately enable PFC. Once the PFC is triggered, it will be enabled for at least 200ms.

$$V_{OUT\_UVP} = 0.25 \times \frac{(R_{zcd\_H} + R_{zcd\_L}) \cdot N_S}{R_{zcd\_L} \cdot N_A}$$

$$PFC\ EN = 1 \times \frac{(R_{zcd\_H} + R_{zcd\_L}) \cdot N_S}{R_{zcd\_L} \cdot N_A} = 4V_{OUT\_UVP}$$

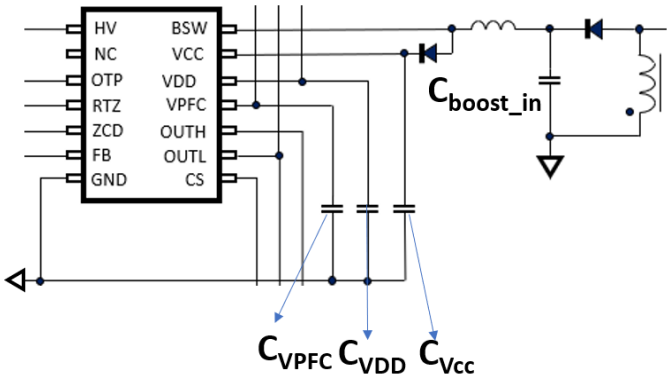
6. FB AND CS PIN

1) FB Rise, Burst →DCM →VSM →ZVS

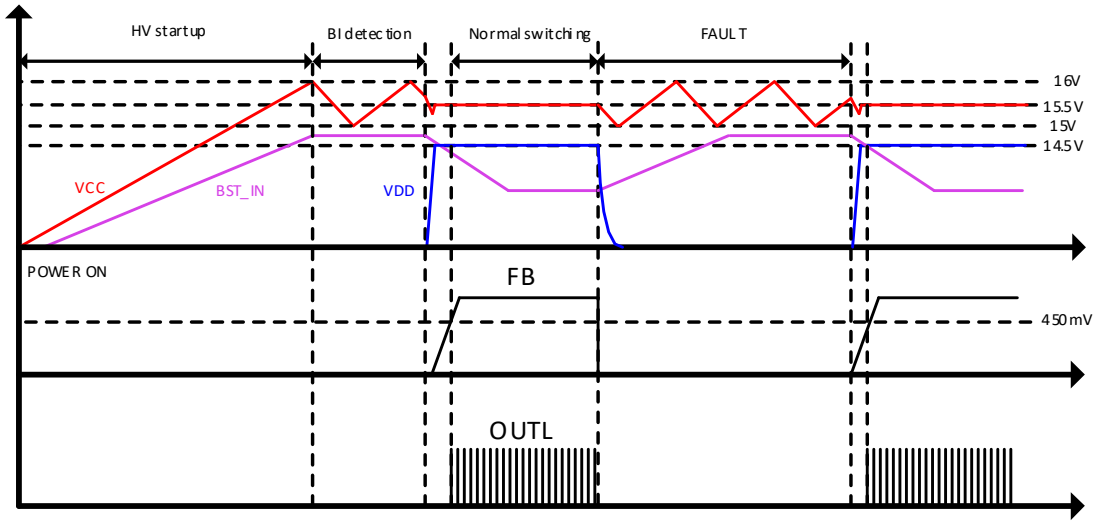
FB Fall, ZVS →VSM →DCM →Burst

Vcs_max = 0.6V FB_max=3.6V and if FB exceeds 3.6V for 80ms, it will trigger OLP protection

7. VCC、VDD、BSW and VPFC



1) Startup waveform



2) Maximum rating

V_{BSW} and VCC are 75V;VDD and VPFC are 20V

3) VCC, VDD and VPFC

The typical Vcc is 16V when boost works. And the UVLO of VCC is 10V. NV9801 integrated LDO and the typical VDD voltage is 14.5V. the maximum load capability of LDO is 48mA. NV9801 integrated PFC control circuit and the typical VPFC is 14.5V.

Tips for capacitance Relationship:

$C_{vcc} > 4C_{Vdd}$

$C_{Vdd} > 4CV_{pfc}$

This can help keep Vcc and VDD more stable.

4) Integrated Boost circuit

If VCC voltage is below 15.5V, boost circuit will be enabled. The working frequency is 1.5MHz and peak current is 300mA.In burst mode, Boost circuit will enter LPM mode to improve efficiency.

a) LPM mode: peak current will be reduced from 300mA to 200mA.

b) LPM mode: Fsw will be reduced from 1.5MHz to 500kHz.

LPM mode: if boost-Vin drops very low and triggers 500ns T_{ONMAX} for 5 consecutive cycles, the boost will stop operating and recover after the next OUTL pulse comes.

Tips 1. L_{boost} will affect the minimum V_{boost_in}

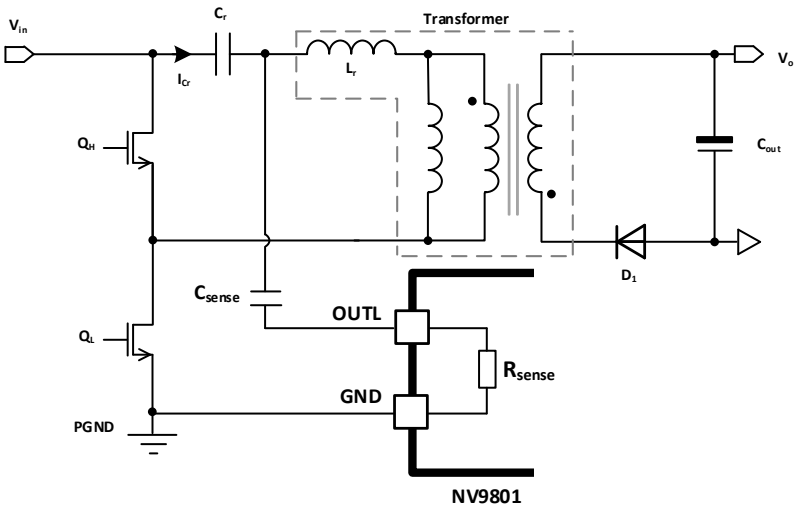
$$V_{boost\_in} = L_{boost}\frac{i_{boost}}{T_{on\_\max}} = L_{boost}\frac{0.2}{0.5}$$

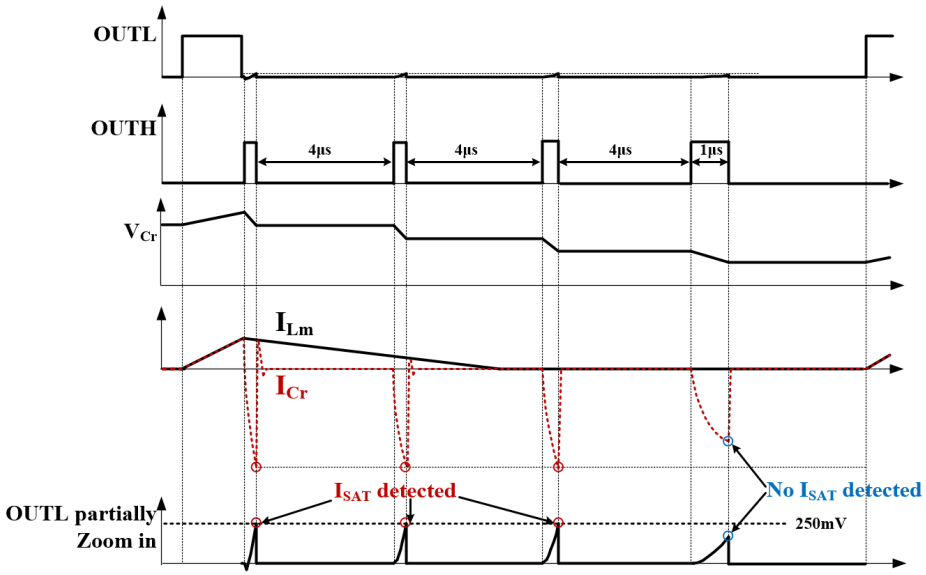
L_{boost}=4.7uH, Minimum V_{boost_in} = 1.9V during LPM

L_{boost}=10uH, Minimum V_{boost_in} = 4V during LPM

Tips 2. Na: Ns>1.5 to improve boost efficiency.

7. OUTL-I-SAT PROTECTION





I-sat protection:

[1] Function: OUTL is PWM signal of low-side switch and it combines ISAT-protection at the same time.

[2] If it works in low frequency mode, the R_{sense} is 2k, if it works in high frequency mode, the R_{sense} is 1k.

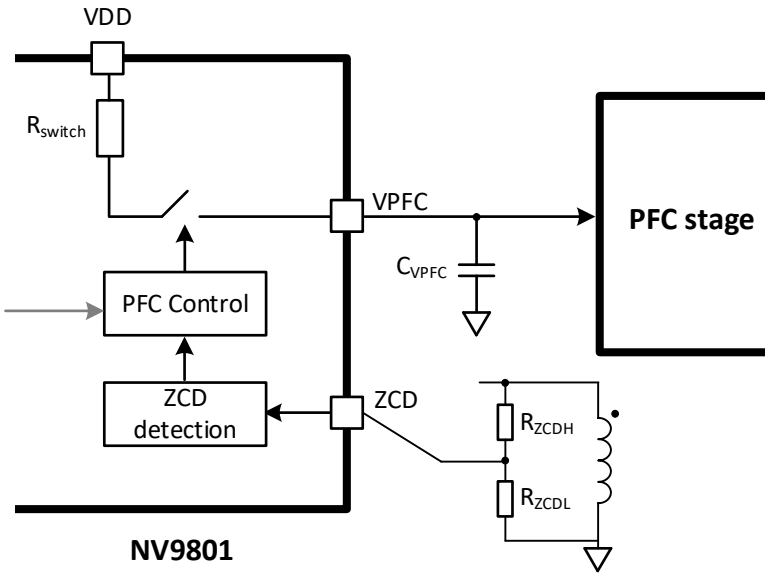
[3] I-sat protection enable condition:

1) Startup and OUTL>0.25.

2) FB<200mV debounce 5ms and OUTL>0.25.

3) Maximum discharge cycle:10*7.

8. PFC EN CONTROL



1) VPFC is used to supply external PFC stage.
2) PFC Enable condition:
   a) In startup, PFC will be enabled for 200ms
   b) In normal work, the PFC enable condition is Vzcd>1V
   c) once PFC is enabled, PFC will debounce for 200ms.

5. AHB Main Circuit Design

5.1 Design Tool Introduction

Step.1 System Information Input			
VO_MAX	Max nominal output voltage	20	V
PO_MAX	Max nominal output power	100	W
VIN_MIN	Min input voltage	260	V
VIN_MAX	Max input voltage	400	V
VIN_selected	Select the input voltage	260	V
VDS_SR	Expected SR drain-to-source voltage rating	100	V
K_VDS_SR	SR drain-to-source voltage de-rating factor	0.85	
D_MAX	Max suggested duty cycle	0.7	
AE	Selected transformer AE	98	mm^2
B_MAX	Designed max flux density	0.3	T
Coss_T	Total equivalent Coss of primary side	150	pF
Tring	Resonant period of SW node, Need to be adjusted according to Fre	1.6	μS
Td	Expected dead time from HS to LS @CRM	480	ns
C_SR	Total equivalent Cds of SR	2200	pF

Step.2: Parameters design of NV9801_INPUT			
Brown-in	Brown-in voltage/DC Voltage	100	V
Brown-out	Brown-out voltage/DC Voltage	85.47	V
Aux ratio_selected	turn ratio between Naxu and Ns/Naux:Ns	1.50	
Naux	Winding turns for Aux	6.00	Ts
Output OVP	OVP setting voltage	24	V
Output UVP	UVP setting voltage	2.5	V
PFC EN	The PFC enables setting voltage	10.00	V
I-sat Current	Max iLr current to trigger I-sat protection	10	A

INPUT	
OUTPUT	Selected

5.2 140W AHB Design Example

Basic system information:

1) Maximum output power:140W
2) Output voltage:5V-28V Maximum output current:5A
3) Bus voltage:300V-400V
4) SR MOS: the breakdown voltage of SR is 100V
5) Maximum duty cycle:0.75
6) AHB TX core: ATQ23.7, JPP95, AE=100mm^2
7) Bmax:0.3T
8) HB GaN: NV6257; CS ratio=3200; $Coss_{eq}$=150pF
9) Brown-in setting voltage:100V (BO will be 85V)
10) Naux:Ns=1.5 (Np:Naux:Na=22:6:4)
11) Ovp setting voltage:33V
12) Uvp setting voltage:2.5V (PFC EN voltage will be 10V)
13) The target iLr current to trigger I-sat protection:10A
14) HB GaN: NV6257;CS ratio=3200;$Coss_{eq}$=200pF

System Calculation and parameters design

1. Calculate the maximum N_{ps}:

$$N_{ps} \le \frac{D_{max} \times V_{bus\_min}}{V_{out\_max}} = \frac{0.75 \times 300}{28} = 8$$

Calculate the minimum N_{ps}:

$$N_{ps} \ge \frac{V_{bus\_max}}{k \times V_{SR}} = \frac{400}{0.85 \times 100} = 4.7$$

N_{ps} is turn ratio between primary winding and secondary winding.In this case,N_{ps} is chosen to be 5.5 to achieve better efficiency.and Ns is chosen to be 4, which is suitable for the ATQ23.7's bobbin.

So we can obtain the final turn ratio of AHB TX:

Np: Ns=22:4

2. Calculate the negative L_m current--i_{Lm_neg}:

$$i_{Lm\_neg} = \frac{Coss_{eq} \times V_{bus\_max}}{T_{dead}} = \frac{400 \times 150 \times 10^{-12}}{450 \times 10^{-9}} = 0.13A$$

$Coss_{eq}$=150pF;T_{dead}=450ns

Calculate the peak L_m current--i_{Lm_peak}:

$$i_{Lm\_peak} = \frac{2 \times I_{out}}{N_{ps} \times \delta} + i_{Lm\_neg} = \frac{2 \times 5}{5.5 \times 0.9} + 0.13 = 2.15A$$

&:The correction coefficient of dead time

3. Maximum allowed magnetic inductance--L_{m_max}

$$L_m \le \frac{N_p \times AE \times B_{max}}{i_{Lm\_peak}} = \frac{22 \times 100 \times 0.3}{1.95} = 338\mu H$$

In this case, Lm is chosen to be 300μH.

4. Calculate the switching frequency:

$$T_{on\_HS} = \frac{L_m \times (i_{Lm\_peak} + i_{Lm\_neg})}{N_{ps} \times V_{out}} = \frac{300 \times (2.15 + 0.13)}{5.5 \times 28} = 4.44\mu s$$

$$T_{on\_LS} = \frac{L_m \times (i_{Lm\_peak} + i_{Lm\_neg})}{V_{bus} - N_{ps} \times V_{out}} = \frac{300 \times (2.15 + 0.13)}{400 - 5.5 \times 28} = 2.78\mu s$$

$$T_{sw} = T_{on\_HS} + T_{on\_LS} + T_{dead} = 4.44 + 2.78 + 0.45 = 7.67us$$

$$F_{sw} = \frac{1}{T_{sw}} = 130kHz$$

5. Calculate the resonant capacitor:

L_k=3μH (the leakage inductance of TX, based on measured value)

$$T_{on\_LS} = \frac{(1.1 \times T_{on\_HS})^2}{4\pi^2 \times L_k} = \frac{1.21 \times 4.44^2}{3.14^2 \times 3} = 0.81uF$$

In this case, Lm is chosen to be 820μF.

6. Calculate the HV charge resistor:R_{HV1}; R_{HV2}

$$R_{HV1} = R_{HV1} = \frac{V_{brown\_in}}{I_{BI} \times 2} = \frac{100}{1.17 \times 2} = 42.7k\Omega$$

7. Calculate the upper divided resistor of ZCD pin:

$$R_{zcd\_H} = \frac{V_{ovp} \times N_{as}}{I_{ovp}} = \frac{33 \times 1.5}{0.5} = 99k\Omega$$

8. Calculate the lower divided resistor of ZCD pin:

$$R_{zcd\_L} = \frac{V_{zcd\_uvp} \times R_{zcd\_H}}{V_{uvp} \times N_{as} - V_{zcd\_uvp}} = \frac{0.25 \times 100}{2.5 \times 1.5 - 0.25} = 7.1k\Omega$$

9. Calculate the RT resistor of RTZ pin:

$$T_{ring} = 2\pi\sqrt{L_m C_{oss\_eq}} = 2 \times 3.14 \times \sqrt{300 \times 10^{-6} \times 200 \times 10^{-12}} = 1.54\mu s$$

$$R_{tz} = \frac{T_{ring} \times 1000}{5} \times 0.8 = 246k\Omega$$

10. Calculate the Rcs resistor of cs pin:

$$GaNsense\_ratio = 3200$$

$$R_{CS} = \frac{V_{cs\_limit} \times GaNsense\_ratio}{1.1 \times i_{Lmpeak}} = \frac{0.6 \times 3200}{1.1 \times 2.15} = 811\Omega$$

11. Calculate the C_{sense} to trigger I-sat protection:

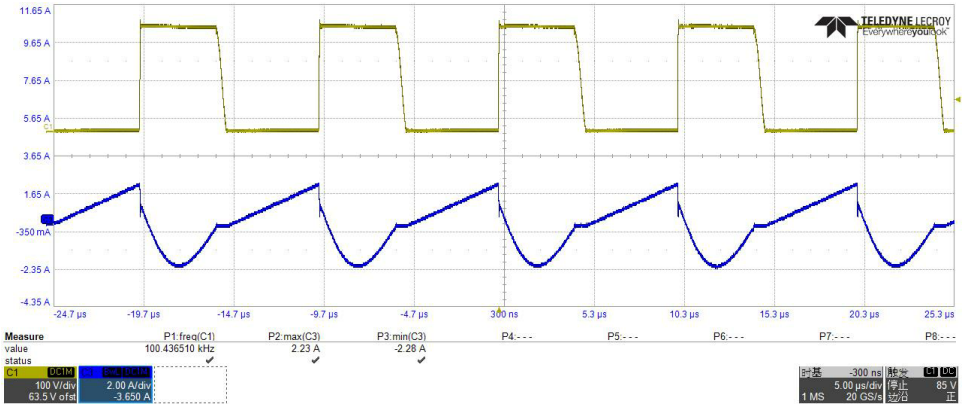
$$R_{CS} = \frac{0.25 \times C_r \times 2 \times 1.4}{I_{sat} \times R_{sense}} = \frac{0.25 \times 0.82 \times 2 \times 1.4}{10 \times 2000} \times 10^6 = 28.7pF$$

12. Cotp: Fsw<300kHz, we did not need to place Cotp and If the fsw exceeds 300kHz, we suggest placing 3.3nF Cotp.

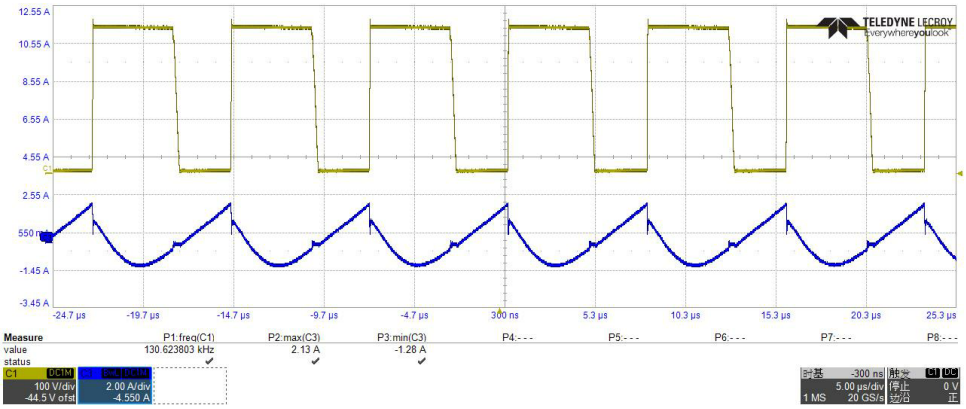
In our 140W demo, the actual parameters are as follows:

AHB transfomer	Lm=300uH; Np:Na:Ns=22:6:4
Cr	470nF/250V MLCC *4
RHV1、RHV2	43kΩ
Rzcd_H	100 kΩ
Rzcd_L	6.8 kΩ
Rtz	250kΩ
Rcs	820Ω
Csense	30pF/1000V

Demo board working waveform



115Vac 28V5A



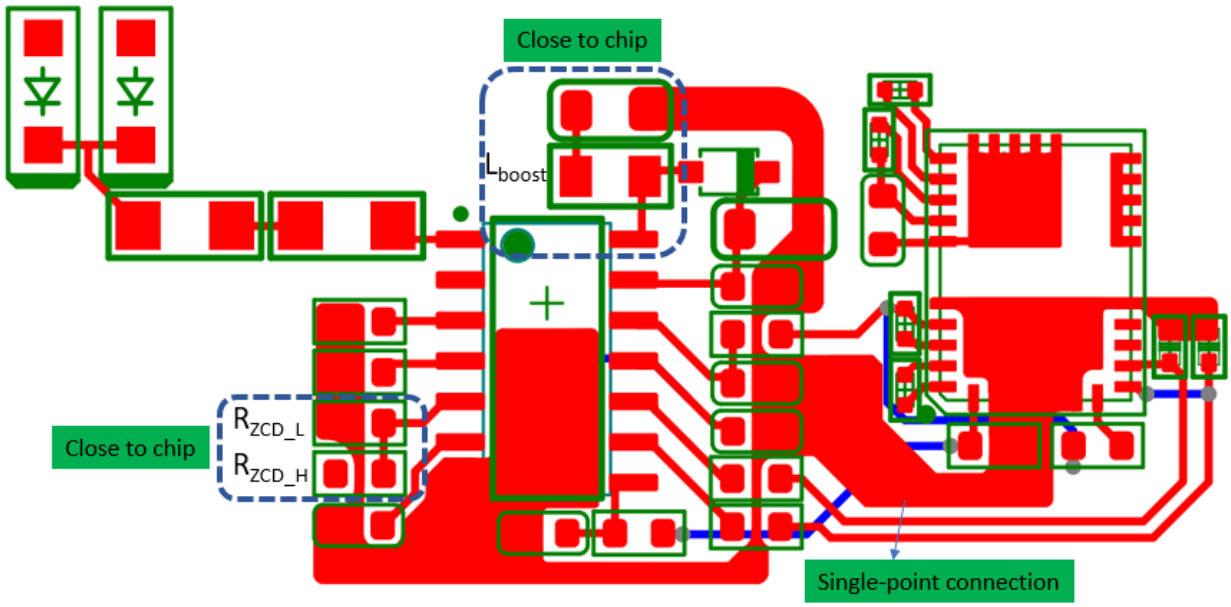
230Vac 28V5A

6. PCB Layout Guideline

Efficient PCB layout is critical for stable operation and EMI performance. In this chapter, we will give some layout suggestions and practical examples.

PCB layout Tips:

1) High frequency power loop should be as small as possible.
2) Rzcd_H and Rzcd_L should be close to NV9801.
3) External Boost inductor should be close to NV9801.
4) FB and CS signal should be kept away from switching node.
5) It is best to use single-point connection to improve loop-stability.



Additional Information

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