Unveiling the Avalanche Capability of SiC MOSFETs Through Unclamped Inductive Switching (UIS) Testing: A Comparative Market Perspective

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1. Abstract

Silicon Carbide (SiC) MOSFETs are a compelling alternative to traditional silicon-based power devices, offering superior performance characteristics such as higher switching speeds, lower on-resistance, and enhanced thermal conductivity. A critical aspect of their reliability and ruggedness is their ability to withstand overvoltage events, particularly those that induce avalanche breakdown. This white paper delves into the inherent avalanche capability of SiC MOSFETs, elucidating the underlying physical mechanisms and highlighting the significance of Unclamped Inductive Switching (UIS) testing as the industry-standard methodology for their evaluation and characterization. Understanding the theoretical underpinnings and the practical testing procedures is crucial for engineers to effectively utilize SiC MOSFETs in demanding power electronic applications like motor drives. Furthermore, this paper provides a comparative overview of commercially available 1200V planar, trench, and trench-assisted planar SiC MOSFETs from leading manufacturers, offering a deeper understanding of their avalanche characteristics and robustness.

2. Introduction

The increasing demand for efficient and compact power electronic systems across various sectors, including electric vehicles, industrial motor drives, and renewable energy inverters, has driven significant interest in wide-bandgap semiconductors like Silicon Carbide (SiC). SiC MOSFETs offer

substantial advantages over their Silicon (Si) counterparts, enabling higher power densities and improved system efficiency. However, the robustness of these devices under transient overvoltage conditions is paramount for ensuring long-term reliability. One such critical condition arises from inductive switching events, where the rapid interruption of current through an inductor can generate significant voltage spikes, potentially forcing the MOSFET into avalanche breakdown. This paper focuses on the avalanche capability of SiC MOSFETs and the Unclamped Inductive Switching (UIS) test, which serves as the primary method for assessing this crucial performance parameter. It also presents a detailed comparison of the avalanche characteristics of SiC MOSFETs from key manufacturers, based on our comprehensive UIS testing.

3. Avalanche Breakdown in Semiconductors

Avalanche breakdown is a phenomenon that occurs in semiconductor devices when a high reverse bias voltage across a p-n junction accelerates minority carriers to energies sufficient to cause impact ionization. These high-energy carriers collide with the crystal lattice, generating electron-hole pairs. These newly generated carriers are then accelerated by the electric field, leading to a chain reaction and a rapid increase in current.

In power MOSFETs, avalanche breakdown typically occurs across the body diode when the drain-source voltage (V_{DS}) exceeds the device's rated breakdown voltage (V_{DSS}). While traditionally viewed as a failure mechanism in Si devices, controlled avalanche operation can be tolerated by some power MOSFETs for short durations, provided the energy dissipated within the device remains below a critical threshold.

4. The Superior Avalanche Capability of SiC MOSFETs

SiC possesses intrinsic material properties that contribute to its enhanced avalanche capability compared to Si:

- **Wider Bandgap:** SiC's wider bandgap (approximately 3.2 eV compared to 1.12 eV for Si) allows for higher breakdown voltages and a reduced intrinsic carrier concentration at elevated temperatures. This translates to a more robust ability to withstand high electric fields without initiating thermal runaway during avalanche.
- **Higher Critical Electric Field:** SiC can sustain electric fields about ten times higher than Si before dielectric breakdown occurs. This allows for thinner and more heavily doped drift layers, leading to lower on-resistance ($R_{DS,ON}$) for a given breakdown voltage and a greater margin for handling overvoltage transients.
- **Higher Thermal Conductivity:** The superior thermal conductivity of SiC facilitates more efficient heat dissipation generated during avalanche events, preventing localized hot spots that can lead to device failure.

These inherent advantages enable SiC MOSFETs to potentially withstand higher avalanche energies and currents compared to similarly rated Si devices. This enhanced ruggedness is a significant benefit in applications where inductive load switching and transient overvoltage events are common.

5. Unclamped Inductive Switching (UIS) Testing: Methodology and Significance

The Unclamped Inductive Switching (UIS) test is an industry-standard method for evaluating the avalanche ruggedness of power MOSFETs. The basic test circuit typically consists of a DC voltage source (V_{DD}), an inductor (L), and the MOSFET under test (DUT). The test sequence involves the following steps:

a) **Turn-on Phase:** The MOSFET is turned on, allowing current to build up through the inductor. The current ramps up linearly with time, determined by the applied voltage and the inductance ($I_L = \frac{V_{DD}}{L} t$).

b) **Turn-off Phase:** The MOSFET is abruptly turned off. Due to the inductive kickback effect, the current through the inductor cannot instantaneously cease. This forces the drain-source voltage (V_{DS}) of the MOSFET to rise rapidly, exceeding V_{DD}.

c) **Avalanche Phase (if triggered):** If the voltage exceeds the MOSFET's breakdown voltage (VDSS), the device enters avalanche breakdown. The energy stored in the inductor ($E = \frac{1}{2} L I_{ds,pk}^2$, where $I_{ds,pk}$ is the peak current before turn-off) is then dissipated within the MOSFET as it clamps the voltage.

d) **Device Recovery:** After the energy is dissipated, the voltage across the MOSFET returns to the DC bus voltage.

During the UIS test, critical parameters are monitored, including:

- **Peak Avalanche Current ($I_{ds,pk}$):** The maximum current flowing through the device during avalanche.
- **Peak Drain-Source Voltage ($V_{ds,pk}$):** The maximum voltage reached across the device during the switching transient.
- **Avalanche Energy (E_{AS}):** The amount of energy the device can withstand during a single non-repetitive avalanche event without failure. This is a key figure of merit for avalanche capability and is often specified in the device datasheet. It can be calculated by integrating the instantaneous power dissipated in the MOSFET during the avalanche phase.
- **Device Temperature:** Monitoring the junction temperature (T_J) is crucial to ensure it remains within the device's safe operating area.

Significance of UIS Testing:

- **Reliability Assessment:** UIS testing provides a direct measure of a MOSFET's ability to survive overvoltage transients caused by inductive loads, which are prevalent in many power electronic applications.
- **Design Margin Verification:** The UIS rating helps engineers determine the appropriate design margins to ensure the MOSFET can withstand unexpected voltage spikes without catastrophic failure, enhancing system reliability.
- **Device Comparison:** UIS test results allow for a direct comparison of the avalanche ruggedness of different MOSFETs, aiding in device selection for specific applications.
- **Quality Control:** UIS testing is often performed as part of the manufacturing process to ensure the quality and reliability of the produced MOSFETs.

6. Factors Influencing SiC MOSFET Avalanche Capability

Several factors can influence the avalanche capability of SiC MOSFETs:

- **Epitaxial Layer Design:** The doping concentration and thickness of the drift layer significantly impact the breakdown voltage and the electric field distribution during avalanche.
- **Device Geometry and Layout:** The physical layout of the device, including cell design and termination structures, plays a crucial role in distributing the current and heat generated during avalanche, preventing localized failures.
- **Gate Driver Characteristics:** While the UIS test focuses on the device's inherent capability, the gate driver's turn-off speed can influence the magnitude of the voltage overshoot and the stress on the MOSFET.
- **Operating Temperature:** Avalanche capability can be temperature dependent. Generally, higher temperatures can reduce the device's ability to withstand avalanche events due to increased carrier generation and reduced thermal conductivity.
- **Repetitive vs. Non-Repetitive Avalanche:** Datasheet specifications often differentiate between single-pulse (non-repetitive) and repetitive avalanche conditions. Repetitive avalanche stresses the device thermally over time and typically results in lower allowable energy dissipation per pulse.

7. Trench-assisted Planar Technology

Navitas' GeneSiC™ SiC MOSFET product line features a proprietary, no compromise trench-assisted planar technology. Traditional designs using legacy planar or trench techniques must compromise between manufacturability, performance, and/or reliability. Although a trench MOSFET has a potential of lower specific on-resistance ($R_{ON,SP}$), it requires about 40% more process steps than planar

thus increasing the cost and lowering the yield. Navitas's patented trench-assisted planar gate design is a no-compromise, next-generation solution; high-yield manufacturing, fast and cool operation, and extended, long-life reliability. It enables the lowest $R_{DS,ON}$ at high temperature and the lowest energy losses at high speeds. This enables unprecedented, industry-leading levels of performance, robustness and quality. Additionally, all GeneSiC SiC MOSFETs have the highest-published 100% production tested avalanche capability.

To delve deeper into this topic, please refer to the comprehensive details available regarding trench-assisted planar SiC MOSFET technology.

8. Comparative Analysis of SiC MOSFET Avalanche Capability in the Market

Table 1. Key information of devices under test from different manufacturers.

Manufacturer	**A**	**B**	**Navitas**	**D**	**E**
Gate Technology	Asymmetric Trench	Double Trench	Trench-assisted Planar	Planar	Planar
Generation	Gen 2	Gen 4	Gen 4	Gen 3	Gen 4
Voltage Rating (V)	1200	1200	1200	1200	1200
BV_{DSS} (V) at V_{GS} = 0V *	1486	1550	1696	1532	1609
Current Rating (A)	56.7	42	70	74	84.3
$R_{DS,ON}$ (mΩ) at 25°C	12.2	18	12.5	14	13
$R_{ON,SP}$ (mΩ·cm²)	1.9	2.4	2.6	3.3	3
BV_{DSS}^2/ $R_{ON,SP}$	1.16E+06	1.00E+06	1.11E+06	7.11E+05	8.63E+05
Q_{GD} (nC)	34	52	82	98	102
Q_{GD} x $R_{ON,SP}$ (nC·mΩ·cm²)	64.6	124.8	213.2	323.4	306
$V_{GS,th}$ (V) *	4.3	4.2	2.6	2.7	2.6
$V_{GS,ON}$ / $V_{GS,OFF}$ (V)	+18/0	+18/0	+18/-5	+18/-3	+15/-4

Notes: 1. Gate technology, generation, voltage rating, current rating, $R_{DS,ON}$, Q_{GD} and $V_{GS,ON}$ /$V_{GS,OFF}$ are from the application notes or datasheets of the manufacturers. 2. All other parameters with * label are based on the average values of 5 samples tested at room temperature.

Table 1 summarizes the key information for the devices under test (DUTs). We selected the latest generation trench SiC MOSFETs from two manufacturers: Manufacturer A (asymmetric trench technology) and Manufacturer B (double trench technology). We also included the latest generation trench-assisted planar SiC MOSFETs from Navitas, and the latest generation planar SiC MOSFETs

from two other distinct manufacturers, D and E. All DUTs had a blocking voltage rating of 1200V. As noted earlier, the trench-assisted planar technology used in Navitas devices offers several advantages over traditional planar technology, including lower $R_{ON,SP}$, Q_{GD} , $Q_{GD} \times R_{ON,SP}$. While trench technology offers a lower $R_{ON,SP}$, Navitas's trench-assisted planar technology delivers a superior FOM (Figure of Merit) considering both BV_{DSS} and $R_{ON,SP}$ ($BV_{DSS}^2 / R_{ON,SP}$). Its performance surpasses that of planar technology and is comparable to trench technology. Furthermore, it boasts lower costs and improved reliability, and robustness compared to trench technology.

To ensure a fair comparison, the active areas of all DUTs were determined through optical measurement following decapsulation. Then the UIS results were normalized based on their active areas. The avalanche capability is evaluated using an unclamping inductive switching (UIS) setup shown in Fig. 1. For the UIS test, a 1.0mH inductor was employed. Each DUT was subjected to progressively increasing inductor current, with increments of approximately 1A per step, until either destructive or parametric failure occurred. The maximum current attained immediately before failure is recorded as the single-pulse avalanche current, $I_{ds,pk}$.

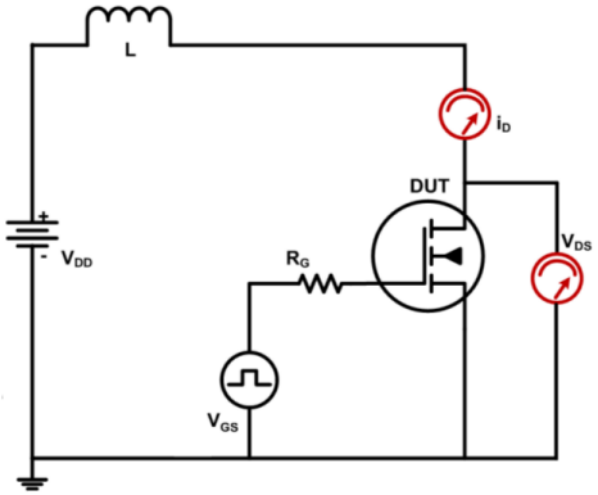

Fig. 1. UIS test circuit schematic [DOI: 10.1109/WiPDA.2016.7799921].

Fig. *2* illustrates the normalized avalanche energy density (E_{AS} / Active Area) and normalized avalanche current density ($I_{ds,pk}$ / Active Area) for all DUTs at 175 °C. Notably, the planar and trench-assisted planar devices demonstrate the higher energy handling capability per unit area, suggesting a more efficient structure for dissipating avalanche energy than the trench devices. This trend of greater robustness in planar devices is further supported by the data in Fig. *3*, which shows the percentage change in normalized avalanche energy density and normalized avalanche current density from 25°C to 175°C, indicating a lower reduction in these parameters for planar and trench-assisted planar devices compared to trench devices at elevated temperatures. Sample B, a Double trench MOSFET, demonstrated poor avalanche capability among all the technologies, indicating inadequate shielding at the trench bottom/corner.

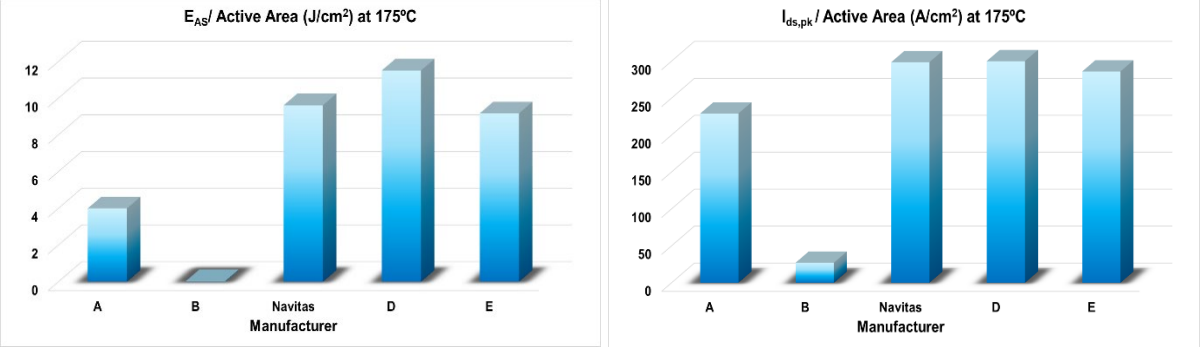

Fig. 2. (left) normalized avalanche energy density (E_{AS} / Active Area); (right) normalized avalanche current density ($I_{ds,pk}$ / Active Area)

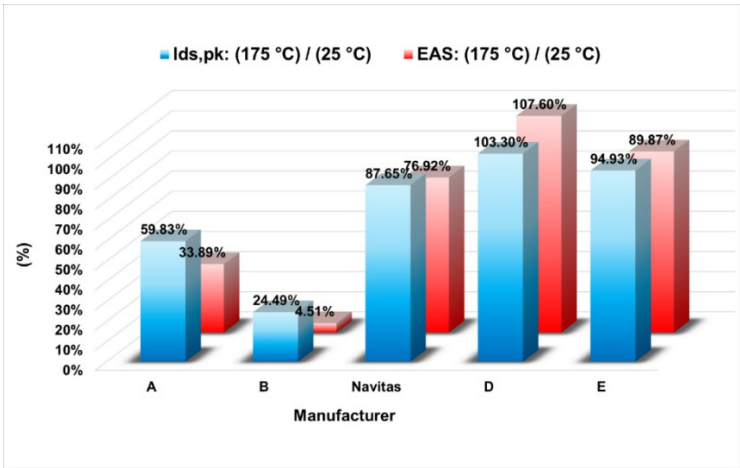

Fig. 3. Percentage change in normalized avalanche energy density and normalized avalanche current density from 25°C to 175°C

These results generally show that the trench SiC MOSFET technology exhibits lower avalanche robustness compared to the planar and trench-assisted planar SiC MOSFETs due to several key design and operational characteristics:

- **Higher Electric Field Concentration at Trench Corners/Bottom:**
    - In a trench MOSFET, the gate oxide is vertical and extends deep into the drift region. This unique structure inherently leads to higher electric field concentrations at the corners and bottom of the trench during high voltage operation, especially during avalanche breakdown.
    - This localized high electric field can accelerate impact ionization in these specific regions, leading to concentrated current flow and excessive heat generation.

- Although SiC MOSFETs use various techniques to shield trench corners and bottoms, even minor mask misalignment during lithography can weaken shield protection in double trench technology or narrow the current spread layer (CSL) in asymmetric trench technology which results in higher $R_{ON,SP}$ and lower yield as illustrated in Fig. 4.

- Planar and trench-assisted planar MOSFETs, with their more spread-out junction, tend to have a more uniform electric field distribution, reducing these localized hot spots.

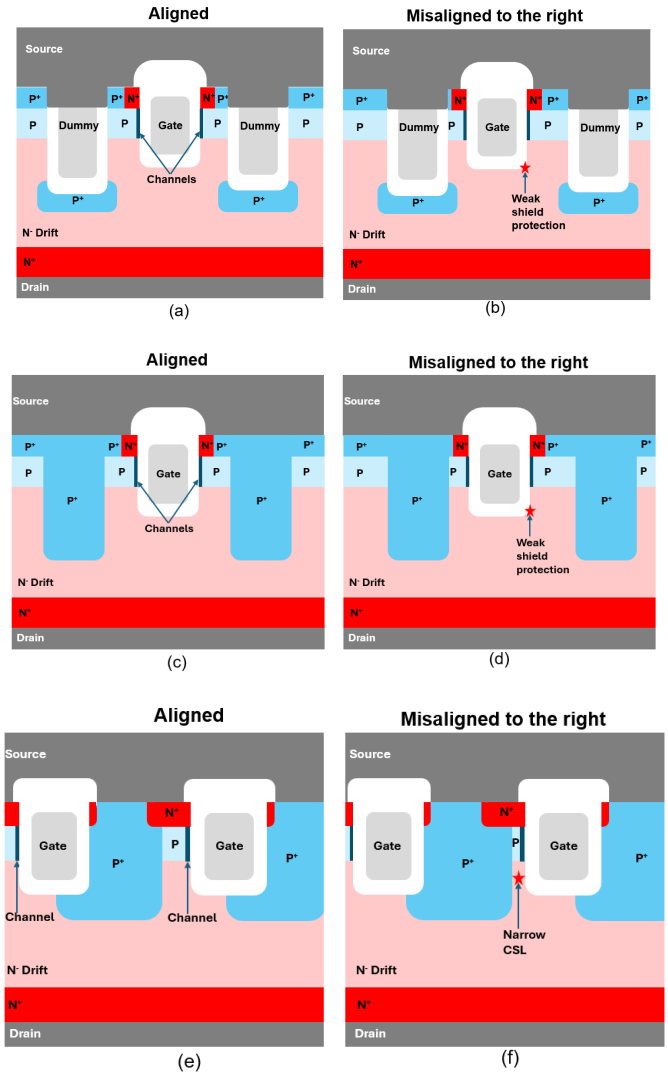

Fig. 4. Schematic cross-sectional view of various trench technologies to shield trench corners and bottoms. (a) and (b) aligned and misaligned in a double trench technology utilizing double dummy trenches followed by P^+ implantation to shield the bottom and corners of the gate. (c) and (d) aligned and misaligned in a double trench technology utilizing multi steps P^+ implantation to make a double deep P^+ regions to shield the bottom and corners of the gate. (e) and (f) aligned and misaligned in an asymmetric trench technology.

- **Gate Oxide Reliability:**
    - In trench designs, the gate oxide on the trench sidewalls and especially at the corners is exposed to very high electric fields during avalanche. This elevated stress can lead to gate oxide degradation or breakdown, which is a common failure mechanism during avalanche events.
    - Planar and trench-assisted planar devices typically have less direct and intense electric field stress on their gate oxide during breakdown.
- **Smaller Chip Size for the Same Rating:**
    - One of the primary advantages of trench MOSFETs is their ability to achieve a lower $R_{ON,SP}$ for a given chip area, allowing for smaller, more compact designs.
    - Lower $R_{ON,SP}$ in trench MOSFETs results in a smaller active area. It means that any given amount of dissipated power (such as during an avalanche event) is concentrated over a smaller volume. This results in a higher power density and a faster rise in junction temperature, making the device more prone to thermal runaway and failure.
    - Planar devices, with their larger die sizes for comparable ratings, have more area to dissipate the energy generated during avalanche, thus offering better thermal management during such events.
- **Current Crowding and Filamentary Conduction:**
    - During avalanche, current tends to crowd in localized regions where the electric field is highest and impact ionization is most prevalent.
    - In trench MOSFETs, these current paths can become highly localized and lead to filamentary conduction, where current flows through very narrow, high-temperature channels. This localized heating can quickly melt the metallization, leading to device destruction.

Fig. 2 and Fig. 3 confirm that Navitas's trench-assisted planar Technology strikes an excellent balance, offering several key advantages:

- **Robust avalanche capability:** It achieves higher avalanche robustness than trench technology and comparable levels to planar technology.
- **Lower static and dynamic resistance:** This technology boasts lower $R_{ON,SP}$, Q_{GD} , and Q_{GD} × $R_{ON,SP}$ compared to planar technology.
- **Superior Figure of Merit (FOM):** It exhibits a higher BV_{DSS}^2/ $R_{ON,SP}$ FOM than planar technology and a comparable FOM to trench technology.

These combined advantages allow Navitas devices to deliver low static and dynamic resistance, fast switching, and superior reliability and robustness compared to competing solutions.

9. Conclusion

The avalanche capability of SiC MOSFETs is a critical parameter that underscores their robustness and suitability for demanding power electronic applications. The inherent material properties of SiC contribute to their superior performance under overvoltage stress compared to Si devices. Unclamped Inductive Switching (UIS) testing serves as the fundamental methodology for characterizing and quantifying this crucial capability. By understanding the principles of avalanche breakdown, the UIS test procedure, and the factors influencing device performance, engineers can effectively leverage the benefits of SiC MOSFETs while ensuring the reliability and longevity of their power electronic systems. Continued advancements in SiC material quality, device design, and testing methodologies will further enhance the avalanche ruggedness and overall performance of these promising power semiconductors.

Our UIS testing reveals a clear advantage in avalanche ruggedness for planar and trench-assisted planar SiC MOSFETs compared to their trench counterparts. The planar and trench-assisted planar devices not only exhibit a higher energy handling capability per unit area at elevated temperatures but also demonstrate a less significant degradation in avalanche performance from room temperature to 175 °C. These findings suggest that the structural differences in both planar and trench-assisted planar technologies contribute to a more robust and temperature-stable avalanche capability, which is a critical factor for demanding power electronic applications like motor drives. **Navitas devices, by leveraging trench-assisted planar technology, gain a significant advantage: they offer avalanche capability comparable to traditional planar technology (and superior to trench technology), coupled with notably improved $R_{ON,SP}$, Q_{GD}× $R_{ON,SP}$, and BV_{DSS}^2/ $R_{ON,SP}$ values compared to planar designs. Ultimately, these advancements provide Navitas devices with low static and dynamic resistance, fast switching speeds, and enhanced reliability and robustness over competitors.**

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