Paralleling Discrete GeneSiC™ Devices in Half-bridge Configurations for Higher-Power Applications

Silicon carbide (SiC) MOSFETs have emerged as critical switching components in high-power applications, including electric vehicle (EV) fast charging, data center power supplies, and renewable energy systems. To enhance current capacity and power density, parallel configurations of multiple SiC MOSFETs have gained significant attention. This paper presents a comprehensive analysis of the parallel operation characteristics of two different gate driver circuit topologies and experimentally validates their feasibility. The experimental results demonstrate that, compared to a unified gate driver network, employing an independent gate driver for each SiC MOSFET ensures more uniform current distribution among paralleled devices, significantly reduces current oscillations, and eliminates loop currents. Furthermore, the study confirms that parallel-connected SiC MOSFETs maintain stable performance even at elevated junction temperatures.

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1. Introduction

Silicon Carbide (SiC) MOSFETs have become indispensable switching components in high-power applications, including electric vehicle (EV) fast charging, data center power supplies, renewable energy systems, energy storage, industrial equipment, and grid infrastructure. To achieve higher current capacity and power density, engineers typically consider two primary approaches: (1) utilizing larger single-device packages or (2) parallel configurations of multiple SiC MOSFETs. This study demonstrates the advantages of the latter, demonstrating superior performance over single-device solutions that require larger footprints.

Key Advantages of Parallel SiC MOSFET Configurations:

- Scalable Current Rating: Parallelization enables modular current scaling without increasing package dimensions, preserving system form factor while additively enhancing current-handling capability.
- Improved Thermal Management: Heat dissipation is distributed across multiple devices, reducing localized thermal flux density and mitigating hotspot formation. This aligns with SiC's inherent high-temperature operational capabilities, enhancing system reliability.
- Design Continuity and Standardization: Identical MOSFETs can be used across multiple system variants, enabling component reuse and retaining existing thermal solutions (e.g., heat sinks, TIMs). This streamlines the upgrade process.

From a power system design perspective, although a parallelized SiC MOSFET architecture will reduce the robustness of the system, it provides enhanced flexibility. Moreover, modular circuit board footprints can be engineered to accommodate varying numbers of SiC MOSFETs, enabling scalable power output without significant redesign efforts. This modular approach reduces development time and facilitates component reuse across multiple system models, improving cost efficiency.

To validate these principles experimentally, we evaluated GeneSiC™ 1200V G3F34MT12K MOSFETs (TO-247-4 package) under parallel operation. A comparative analysis of two gate driver circuit topologies was conducted to assess their impact on switching characteristics. The results offer critical insights for optimizing high-current, high-power designs in applications such as electric vehicles, renewable energy systems, and industrial power electronics.

2. Circuit Description

2.1 Isolated Gate Driver Power Supply

An isolated DC-DC converter module (Fig. 1) powers the gate driver circuits, employing a dual-output configuration with a common return to ensure galvanic isolation between input and output stages. Designed for a +15V input, the converter delivers two isolated outputs: +18V and -3V. These dual-polarity outputs are specifically routed to the high-side and low-side power switching devices in the bridge configuration, respectively. The +18V rail ensures fast turn-on of the SiC MOSFETs, while the -3V rail guarantees reliable turn-off by suppressing Miller effect-induced delays, thereby enhancing switching performance and noise immunity.

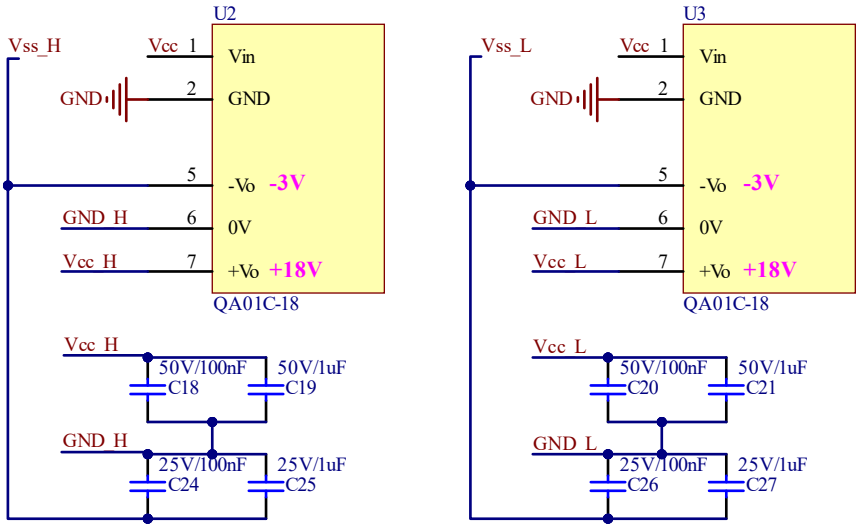


Fig. 1: Isolated gate driver power supply.

2.2 Paralleling SiC MOSFETs in a Half-Bridge Circuit

The parallel half-bridge configuration (Fig. 2) integrates SiC MOSFET pairs QH1/QH2 (high-side) and QL1/QL2 (low-side). The high-side MOSFET drains connect directly to the DC bus voltage (Vin), while the low-side sources terminate at power ground (PGND). A shared switching node (SW) links both half-bridges. For precise current measurements, low-inductance shunt resistors are placed in series with the MOSFET source terminals. These shunts generate voltage drops proportional to device currents, which are monitored via BNC-connected oscilloscopes to capture dynamic switching behavior.

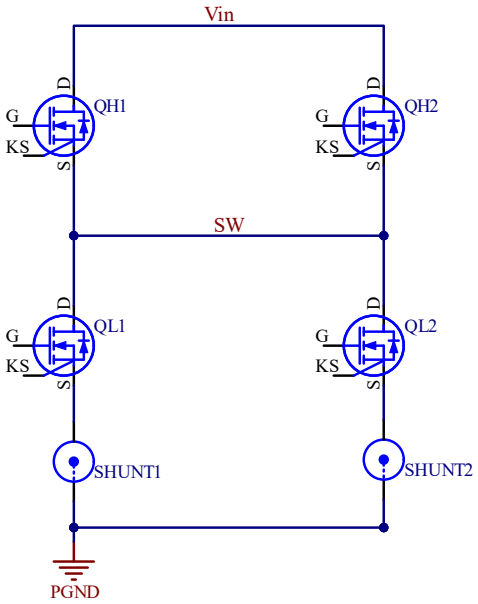


Fig. 2: Paralleling SiC MOSFETs in a half-bridge circuit.

2.3 Gate Drive Circuit Design

Based on the structural characteristics of paralleling SiC MOSFET configurations, the gate drive circuit design can be categorized into two distinct topologies:

2.3.1 Setting 1: Unified gate driver network

The output stage of the gate driver circuit (Setting 1, Fig. 3) utilizes a dual-channel isolated gate driver IC with 4 A peak current capability to drive each parallel-connected high-side and low-side MOSFET pair. The gate driver network is symmetrically distributed across all parallel devices in both upper and lower half-bridges to ensure uniform switching performance.

Critical consideration in this topology pertains to parasitic current paths in the auxiliary power connections. While the primary current flow follows the intended conduction path (highlighted in green), alternative current paths may emerge between the gate terminals and Kelvin source terminals. These unintended loop currents (depicted by the red dashed line in Fig.3), lacking sufficient impedance damping, can induce gate oscillations. Such oscillations may exceed acceptable thresholds, potentially leading to device instability or abnormal operation of the SiC MOSFETs.

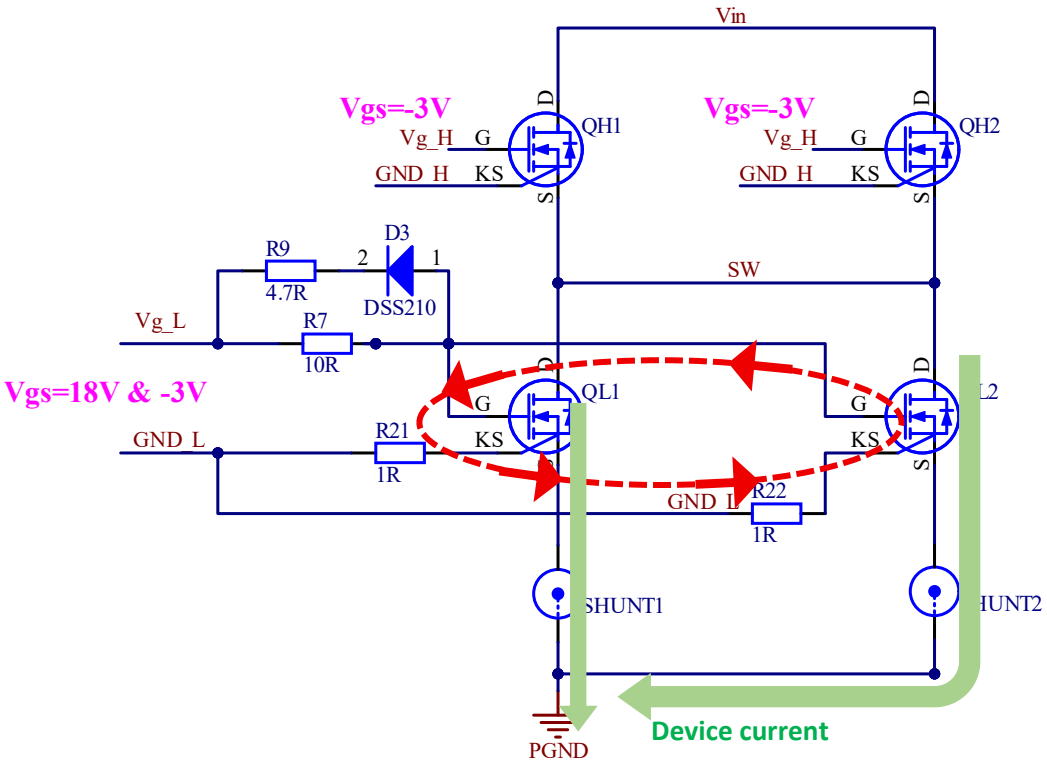


Fig. 3: Setting 1: Unified gate driver network.

2.3.2 Setting 2: Dedicated gate drive networks

To address the aforementioned constraints, Setting 2 employs a decentralized gate drive architecture, as illustrated in Fig. 4. Within this design framework, each parallel-connected MOSFET in both the upper and

lower half-bridges is equipped with an independent gate drive network. The integration of series gate resistors establishes localized impedance networks that effectively suppress parasitic loop currents. Notably, the SK-series resistors (R21, and R22) provide optimized impedance matching between QL1 and QL2 in the parallel half-bridges, significantly improving current distribution uniformity.

This segmented approach reduces gate oscillation amplitudes compared to Setting 1. The impedance-matched drive networks ensure stable gate-source voltage regulation, thereby maintaining reliable switching performance across all parallel devices.

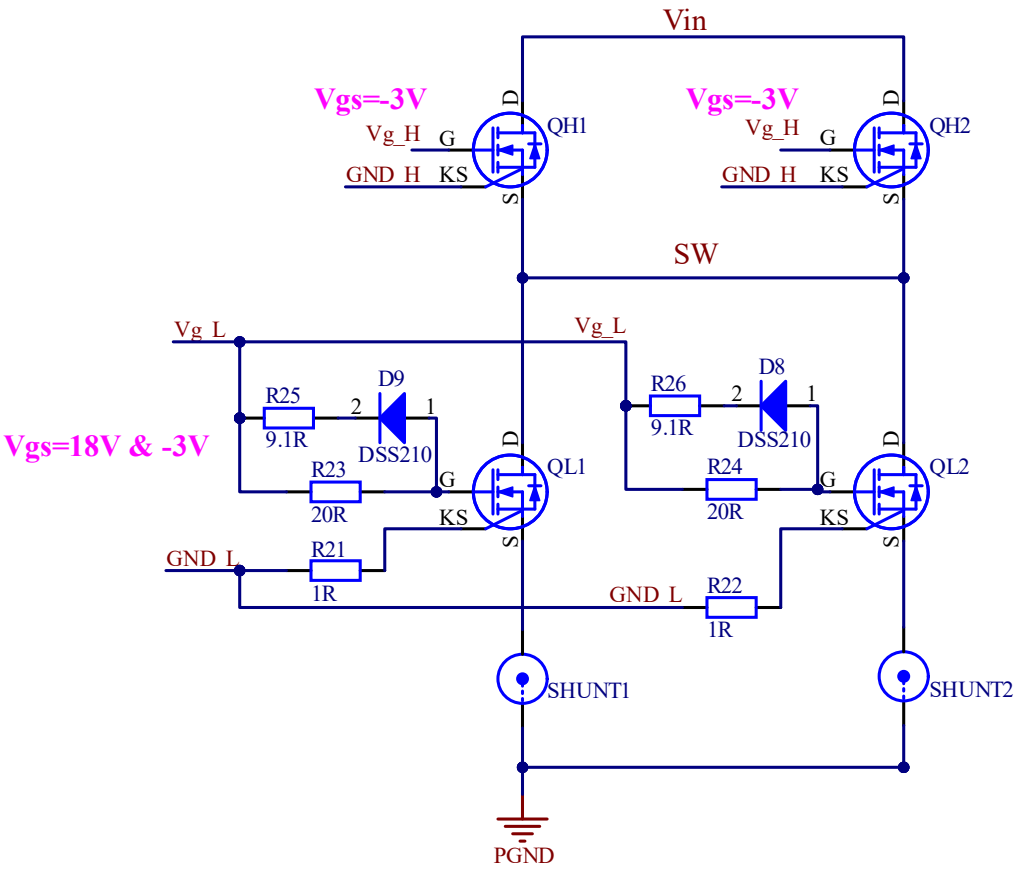


Fig. 4: Setting 2: Dedicated gate drive networks.

3. SiC MOSFET Device and PCB Information

3.1 SiC MOSFET Device

The TO-247-4 packaged Navitas' 1200V, 34mΩ GeneSiC™ MOSFET (G3F34MT12K) is used in this study. Tables 1 and 2 provide detailed overviews of the absolute maximum ratings and pivotal electrical specifications of the G3F34MT12K SiC MOSFET, respectively [1].

Table 1: Absolute maximum rating values.

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µA	1200	V
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +22	V
Gate-Source Voltage (Static)	$V_{GS(op)-ON}$ $V_{GS(op)-OFF}$	Recommended Operation	18 -5 to -3	V
Continuous Drain Current	I_D	T_C = 25°C, V_{GS} = -5 / +18 V T_C = 100°C, V_{GS} = -5 / +18 V T_C = 135°C, V_{GS} = -5 / +18 V	63 45 33	A
Pulsed Drain Current	$I_{D(pulse)}$	t_P ≤ 3µs, D ≤ 1%, V_{GS} = 18 V	156	A
Power Dissipation	P_D	T_c = 25°C	263	W
Non-Repetitive Avalanche Energy	E_{AS}	L = 36 mH, I_{AV} = 6 A	648	mJ
Operating Junction and Storage Temperature	T_j , T_{stg}		-55 to 175	°C

Table 2: Key electrical characteristic parameters.

Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	1200			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V		1	50	µA
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 22 V V_{DS} = 0 V, V_{GS} = -10 V			100 -100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 18 mA	2.2	2.8	4.3	V
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 26 A V_{DS} = 10 V, I_D = 26 A, T_j = 175°C		14.4 15.7		S
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 18 V, I_D = 26 A V_{GS} = 18 V, I_D = 26 A, T_j = 175°C		34 63	45	mΩ
Input Capacitance	C_{iss}	V_{DS} = 800 V, V_{GS} = 0 V f = 500 KHz, V_{AC} = 25mV		2418		pF
Output Capacitance	C_{oss}			89		
Reverse Transfer Capacitance	C_{rss}			6.9		
C_{oss} Stored Energy	E_{oss}			35		µJ
C_{oss} Stored Charge	Q_{oss}			126		nC
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			109		pF
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			158		
Gate-Source Charge	Q_{gs}	V_{DS} = 800 V, V_{GS} = -5 / +18 V I_D = 26 A Per JEDEC JEP-192		29		nC
Gate-Drain Charge	Q_{gd}			28		
Total Gate Charge	Q_g			104		
Internal Gate Resistance	$R_{G(int)}$	V_{GS} = 18 V, f = 1 MHz, V_{AC} = 25 mV		1.0		Ω

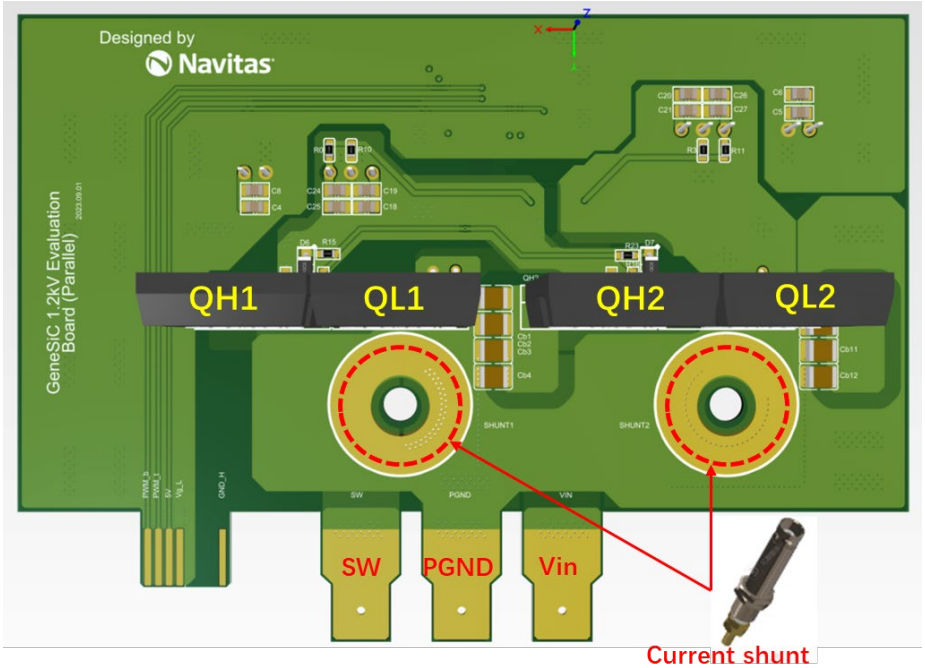
3.2 Evaluation Board Layout

Fig.5 presents the layout of the parallel PCB evaluation board designed for SiC MOSFET paralleling operations. The evaluation board is structured into five sections: the connector assembly, main power switches, isolated gate driver integrated circuit (GDIC), isolated gate driving power supply, and current shunt.

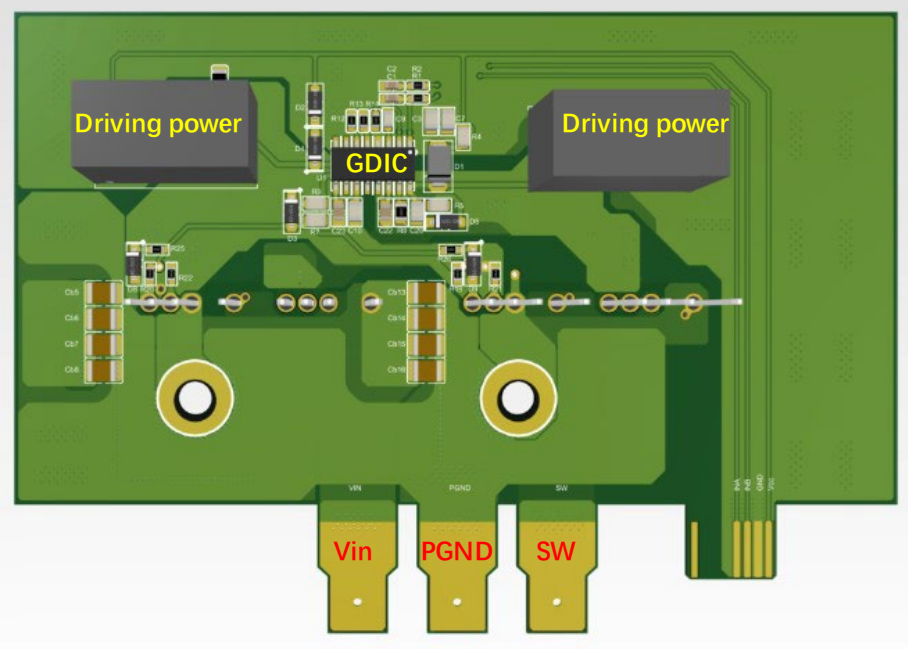
The GDIC employed is a dual-channel isolated gate driver (SiLM8243-AQ) with 4A peak output current capability and 100V/ns common-mode transient immunity. Two independent isolated gate driving power supplies (QA01C-18) provide +18V/-3V bias voltages to the upper and lower bridge power switches, respectively, ensuring proper turn-on/-off characteristics.

Two 15mΩ current shunts (SSDN-015) serve as critical measurement components for real-time device current monitoring. This current shunt features a BNC interface (50Ω impedance), enabling high-fidelity current waveform observation through a 1GHz bandwidth oscilloscope (Tektronix MSO64B).

The gate driver circuit layout prioritizes mitigation of parasitic inductance effects and related parameters. This design focus aims to minimize parasitic influences on gate drive signal integrity, ensuring reliable and efficient operation of the paralleled SiC MOSFET system.



(a) Top view



(b) Bottom view

Fig. 5: PCB evaluation board layout.

4. Experimental Results and Analysis

To investigate the characteristics of parallel-connected SiC MOSFET devices, a comprehensive double-pulse test platform operating at 800 V bus voltage has been meticulously constructed, as illustrated in Fig. 6.

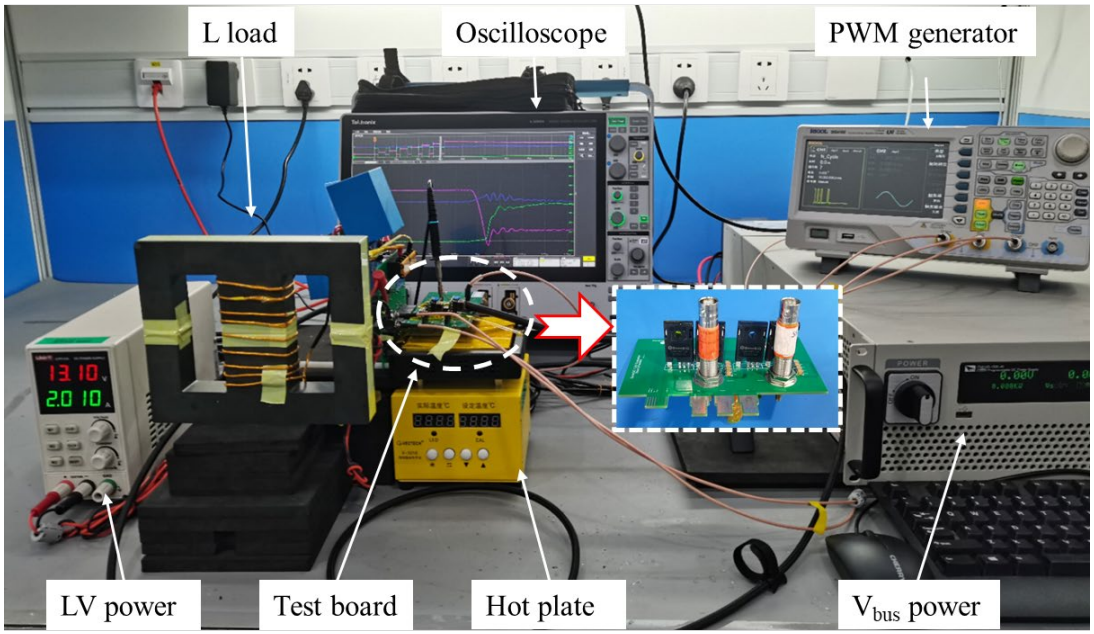


Fig. 6: Bench setup of the paralleling double-pulse test platform.

It is worth emphasizing that a substantial number of G3F34MT12K devices were rigorously screened according to their threshold voltage characteristics. Eventually, two groups of devices with significantly disparate threshold voltages were selected as the devices under test (DUTs). These devices represent the worst-case scenario for this analysis. For detailed information, please consult Table 3. This approach enables systematic evaluation of parallel challenges under extreme parameter variation.

Table 3: Threshold voltage of the device under test

Half-bridge		Serial	Vth @Id=18mA	Rds(on) @Ids=35A,Vgs=18V
#1	Upper device	QH1	3.426V	41.209m
	Lower device	QL1	3.405V	40.189m
#2	Upper device	QH2	2.864V	37.756m
	Lower device	QL2	2.930V	38.532m

Note: Vth min.=2.2V, Vth max.=4.3V (for G3F34MT12K)

This carefully planned experimental design establishes a solid foundation for assessing the parallel characteristics of SiC MOSFETs. It enables a more profound comprehension of the complex interactions between electrical parameters and device performance.

4.1 Performance Analysis Between Setting1 and Setting2

Building on the gate driver circuit analysis in Section 2.3, this study conducted a comparative evaluation of both driver configurations. Through careful selection of gate resistors, we matched the equivalent turn-on and turn-off resistances between both circuits, ensuring controlled experimental conditions. Complete gate resistance parameters are provided in Table 4. In addition, the SK series resistors R21 and R22 are 1Ohm.

Table 4: Gate drive resistance setting

Half-bridge		Serial	Setting 1		Setting 2	
			Turn-on	Turn-off	Turn-on	Turn-off
#1	Lower device	QL1	R7=10 Ohm	R9=4.7 Ohm	R23=20 Ohm	R25=9.1 Ohm
#2	Lower device	QL2	R7=10 Ohm	R9=4.7 Ohm	R24=20 Ohm	R26=9.1 Ohm

Figs. 7 and 8 present the comparative analysis of double-pulse test waveforms under the two specified operating conditions. Fig. 9 illustrates the current difference Δids (defined as ids(QL1) – ids(QL2)) between the conducting currents of power devices QL1 and QL2 under these conditions.

During the turn-on transient (Fig. 7), QL2 exhibits a faster current rise rate than QL1, attributed to its lower threshold voltage (Vth). As shown in Fig. 9, the current distribution between QL1 and QL2 remains non-uniform even after both devices reach full conduction, with Δids peaking at 3 A for Setting 1. This imbalance may result in unequal switching losses between the parallel-connected devices, potentially inducing localized thermal stress and degrading long-term reliability in high-power operation.

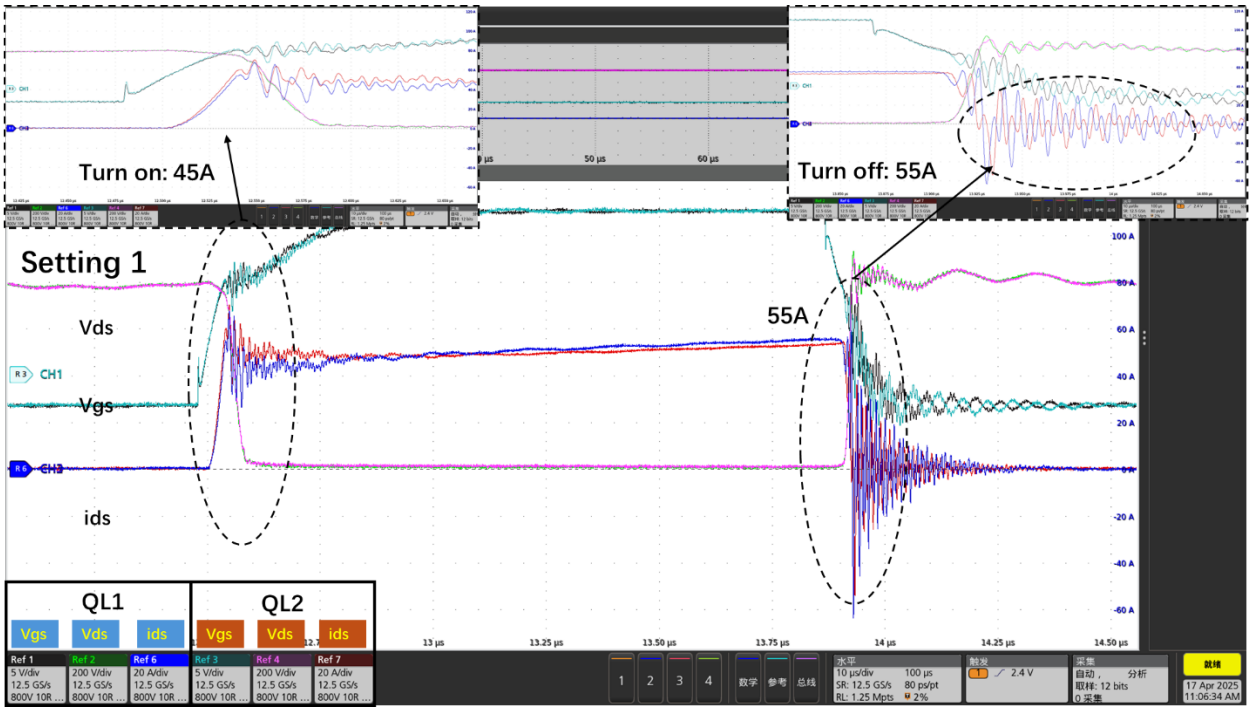


Fig. 7: The double-pulse switching waveform under Setting 1. (Tj=25℃)

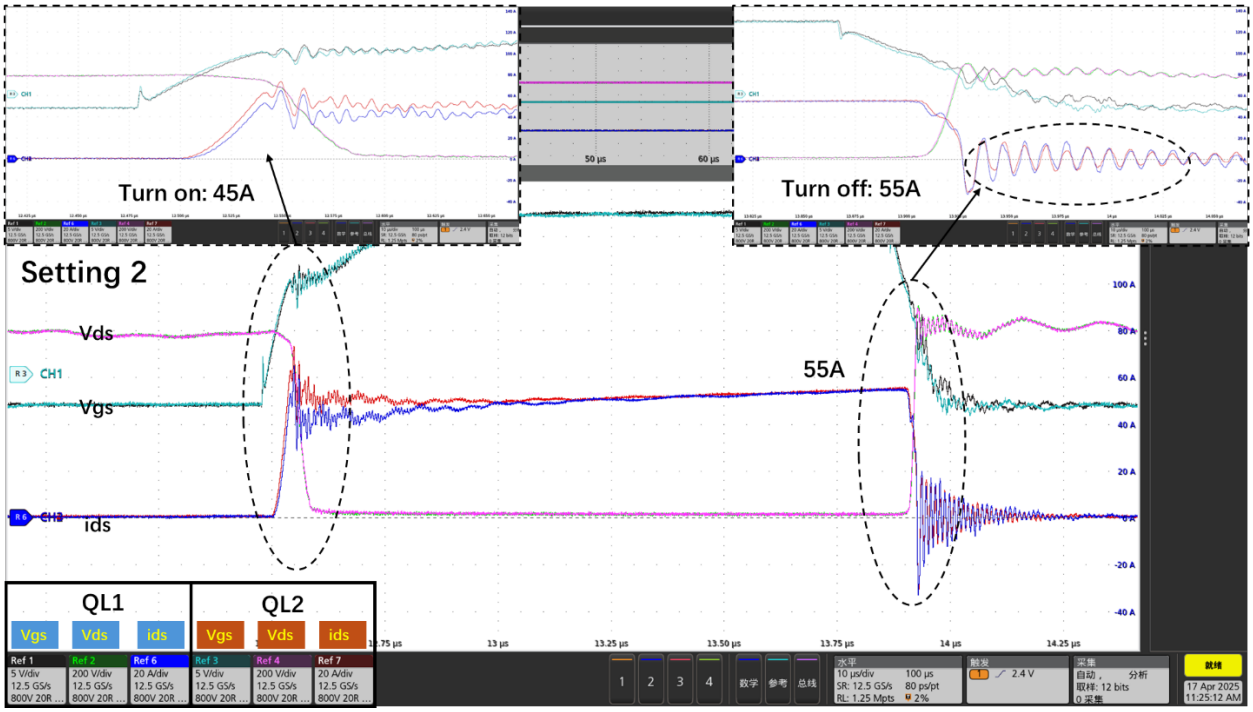


Fig. 8: The double-pulse switching waveform under Setting 2. (Tj=25℃)

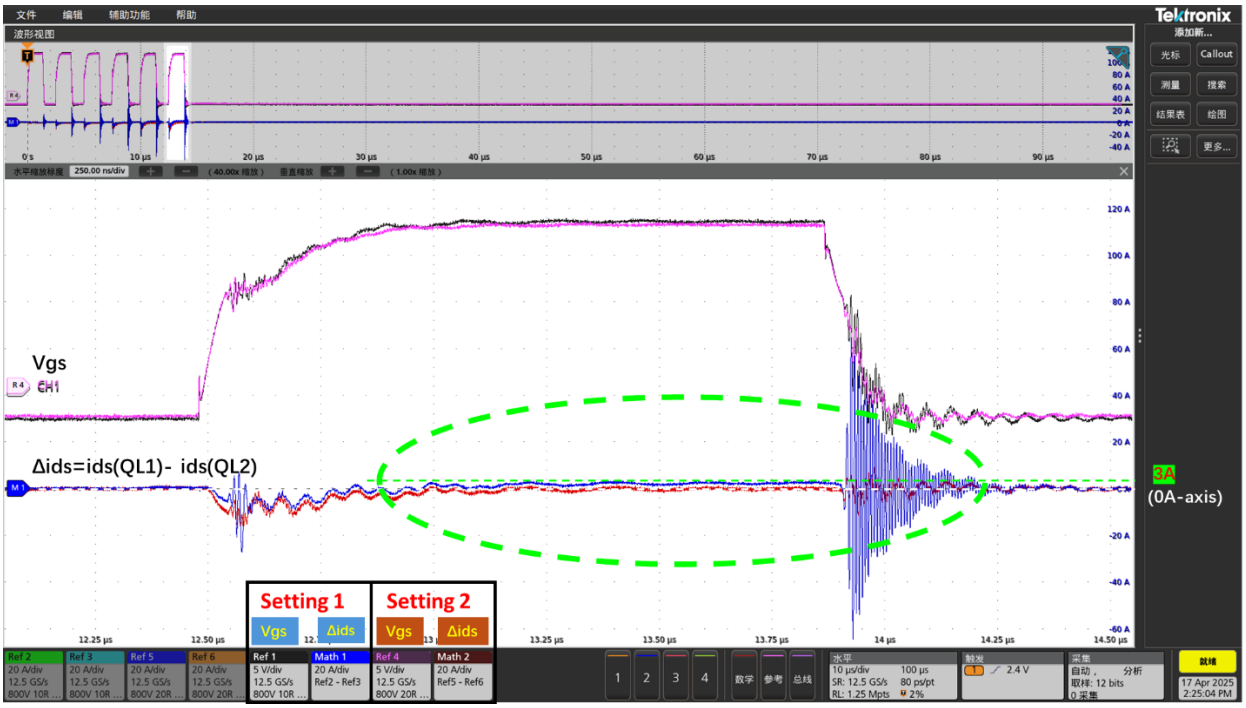


Fig. 9: The comparison of Δids waveforms. (Tj=25℃)

Notably, the gate-to-source (Vgs) and drain-to-source (Vds) voltages of both devices demonstrate synchronized switching transients with minimal discrepancies. However, during turn-off, a measurable phase offset emerges in their current waveform oscillations. This phase disparity suggests the presence of a gate drive loop current, corroborating the theoretical analysis in Section 2.3.

In contrast to Setting 1, Figs. 8 and 9 reveal that Setting 2 achieves balanced current sharing between the devices. Additionally, the turn-off current oscillations of QL1 and QL2 remain in-phase under Setting 2. These results empirically validate that independent gate drive circuits for the upper and lower half-bridge devices effectively suppress parasitic loop currents, improving current-sharing uniformity and overall system robustness.

Table 5: Switching characteristic parameters comparison

Serial		Turn-on (ids=45A)				Turn-off (ids=55A)			
		dv/dt (V/ns)	di/dt (A/ns)	Ipeak (A)	Eon (mJ)	dv/dt (V/ns)	di/dt (A/ns)	Vpeak (V)	Eoff (uJ)
Setting 1	QL1	17.36	1.59	67.50	1.483	50.46	2.47	933.15	236.20
	QL2	16.82	1.69	70.30	1.676	52.80	2.57	901.09	159.04
Setting 2	QL1	16.73	1.60	64.67	1.436	52.26	2.44	906.51	193.17
	QL2	16.71	1.60	73.28	1.696	52.22	2.55	896.58	200.18

Figs. 10 and 11 present comparative double-pulse waveforms for QL1 and QL2 under the two different gate drive configurations, with corresponding switching characteristic parameters summarized in Table 5. The results indicate nearly identical turn-on behavior between the two settings, demonstrating consistent performance during this phase.

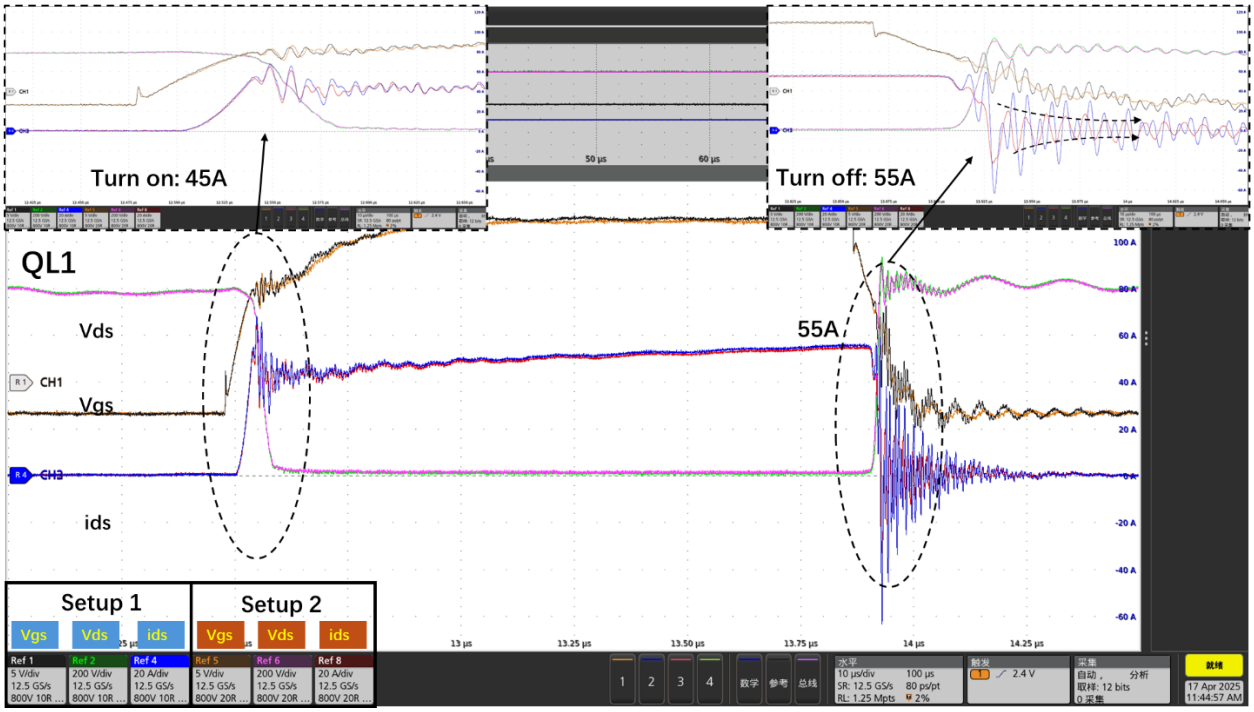


Fig. 10: The comparison of double-pulse waveforms of QL1. (Tj=25℃)

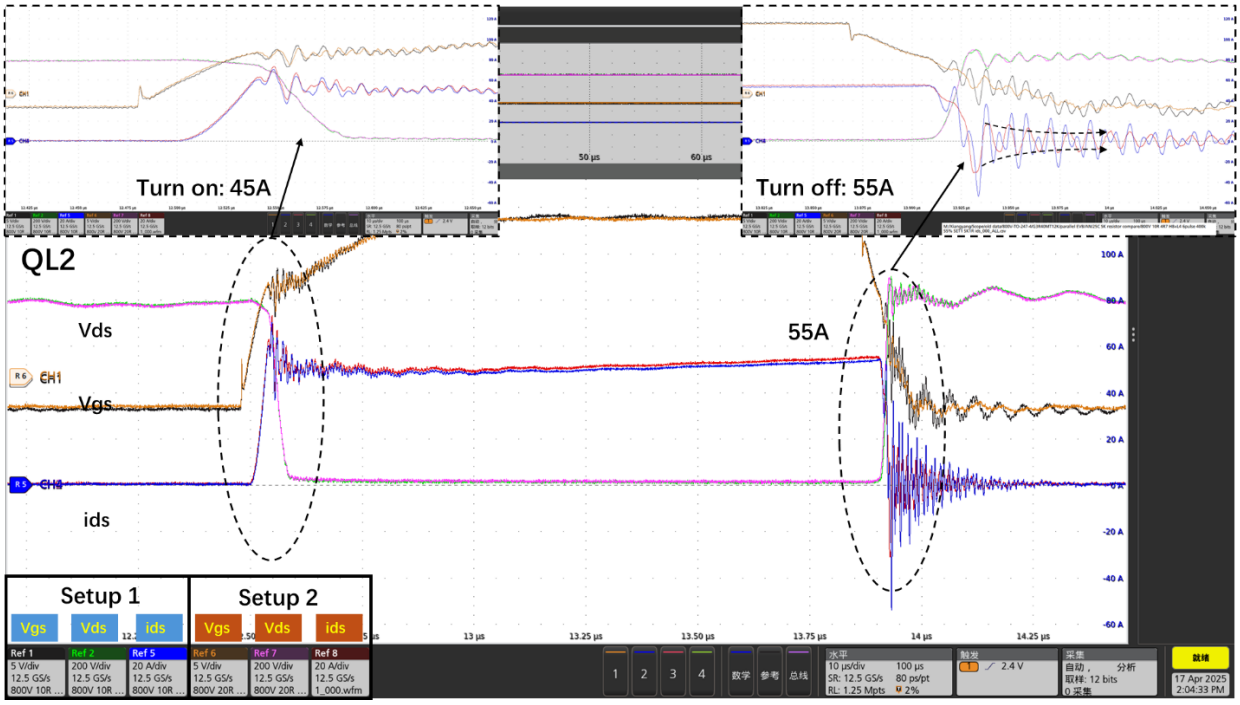


Fig. 11: The comparison of double-pulse waveforms of QL2. (Tj=25℃)

Table 6 Turn-off current ringing characteristic parameters comparison

Serial		Turn-off current ringing		
		Undershoot (A)	Overshoot (A)	Ringing time (ns)
Setting 1	QL1	-63.61	38.02	219.97
	QL2	-54.07	36.12	211.38
Setting 2	QL1	-33.09	19.89	144.02
	QL2	-30.88	16.96	133.44

However, significant differences emerge during turn-off. Setting 1 exhibits pronounced current ringing, posing substantial electromagnetic compatibility (EMC) challenges. As detailed in Table 6, Setting 2 demonstrates marked improvement, with turn-off current overshoot and undershoot amplitudes reduced by approximately 50% compared to Setting 1. Additionally, the ringing frequency is lower in Setting 2, and the current settling time (to ±10% of ids) is reduced by approximately 100 ns, as indicated by the white dashed-line arrows in the figures.

Notably, Setting 2 effectively eliminates the gate voltage oscillations observed in Setting 1. This suppression is critical for reliable device operation, as gate voltage oscillations may induce unintended switching events, compromising circuit stability and long-term reliability.

These findings conclusively demonstrate the necessity of implementing independent gate driver networks for each power device. The improved performance in Setting 2, characterized by reduced current ringing, faster settling time, and stable gate voltage, validates this design approach for enhancing both EMC performance and operational reliability.

4.2 Performance Analysis of the Influence of SK Series Resistance

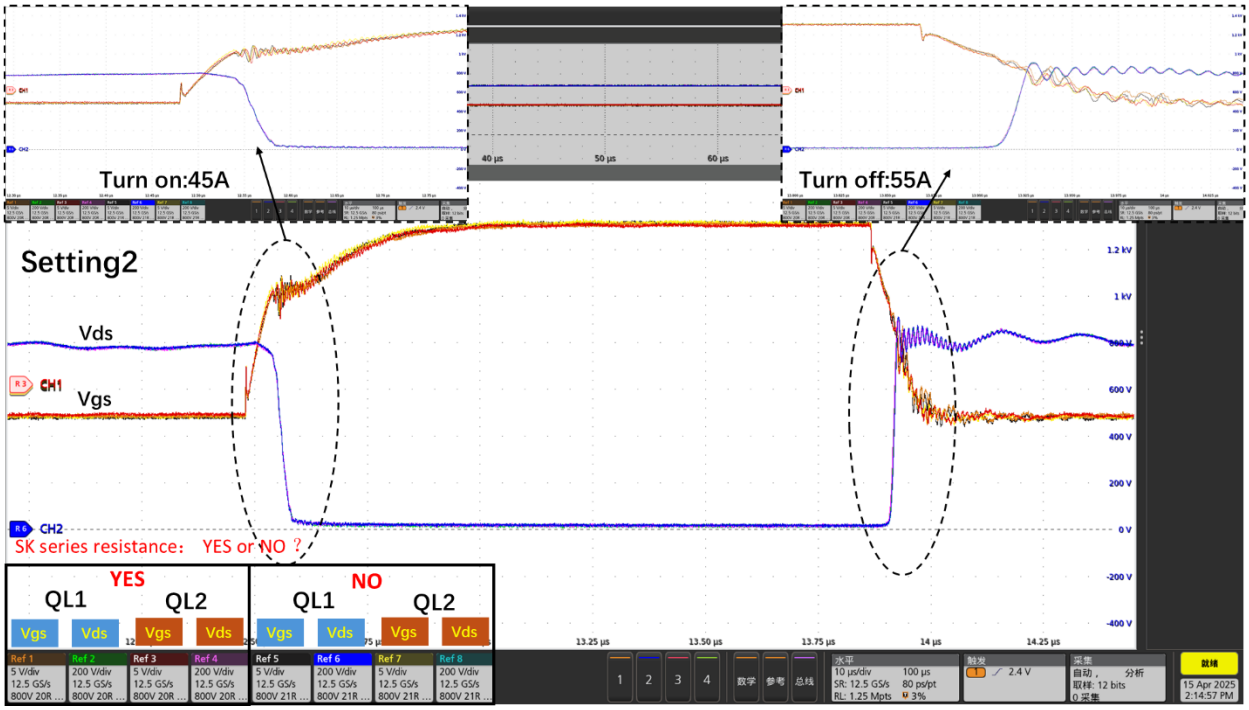
To investigate the impact of the SK series resistance, the equivalent turn-on and turn-off resistances of the gate drive circuits were equalized through a judicious selection of the gate drive turn-on and turn-off resistances. For detailed parameter settings of the gate driver resistances, please refer to Table 7.

Table 7: Gate drive resistance for Setting 2

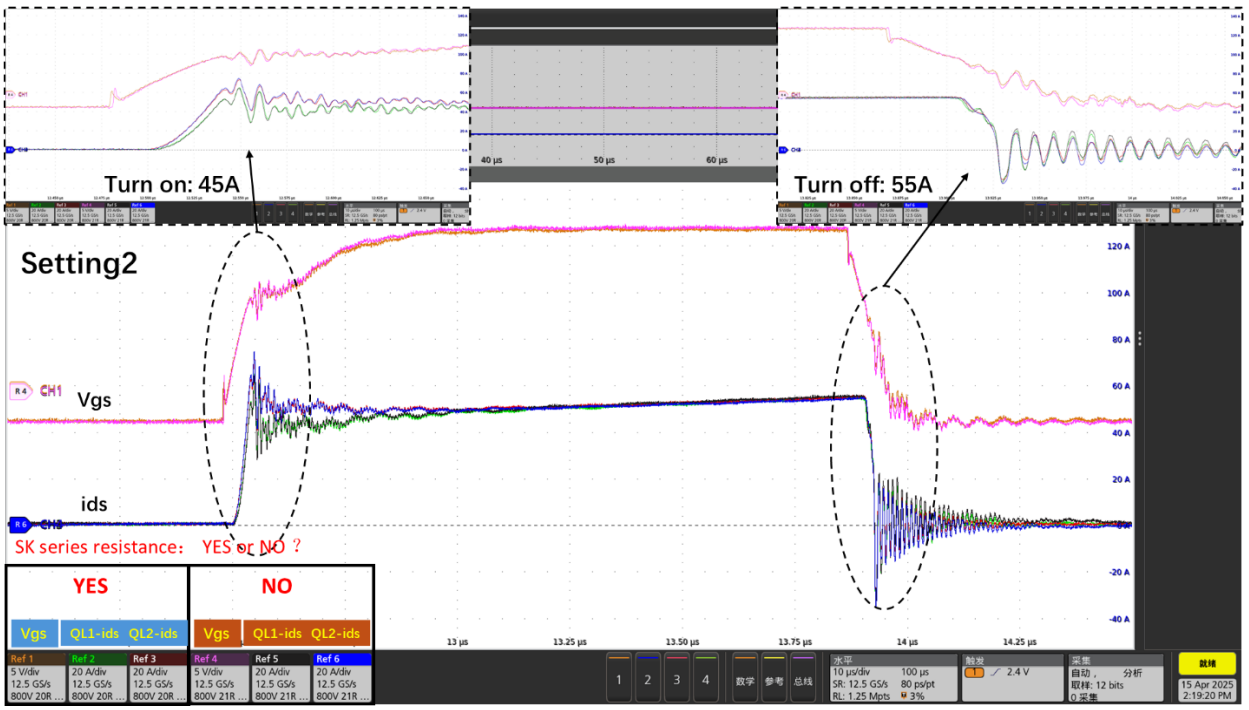
Setting 2		Serial	SK series resistance: YES			SK series resistance: NO		
			Turn-on (Ohm)	Turn-off (Ohm)	SK (Ohm)	Turn-on (Ohm)	Turn-off (Ohm)	SK (Ohm)
#1	Lower device	QL1	R23=20	R25=9.1	R21=1	R23=21	R25=10	R21=0
#2	Lower device	QL2	R24=20	R26=9.1	R22=1	R24=21	R26=10	R22=0

Fig. 12 compares double-pulse waveforms with and without SK series resistance, while Fig. 13 shows the conduction current difference Δids (defined as ids(QL1)-ids(QL2)) between power devices QL1 and QL2.

As evident from Fig. 12(a), the drain-source voltage (Vds) of both devices remains unaffected by the presence of SK series resistance during turn-on and turn-off transitions. Fig. 12(b) reveals nearly identical ids waveforms during turn-on, with in-phase current oscillations during turn-off for both configurations.



(a). The comparison of Vds waveforms.



(b). The comparison of ids waveforms.

Fig. 12: The comparison of double-pulse waveforms for SK series resistance or not. (Tj=25℃)

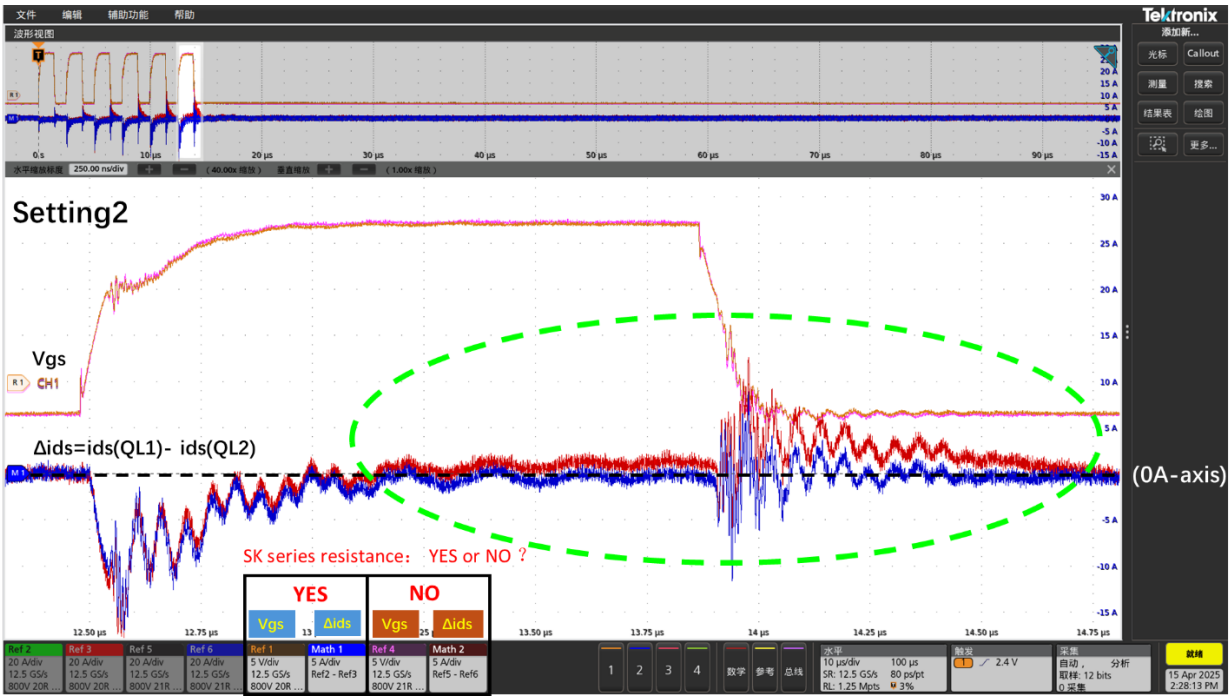


Fig. 13: The comparison of Δids waveforms for Setting2. (Tj=25℃)

However, Fig. 13 demonstrates significant current imbalance without SK series resistance. The persistent positive Δids during full conduction indicate uneven current sharing between QL1 and QL2. This imbalance leads to unequal switching losses in the parallel devices, potentially causing excessive temperature rise in one device and compromising operational reliability under high switching loss conditions.

In contrast, after the inclusion of SK series resistance, it can be seen that the difference Δids in the conduction current through QL1 and QL2 remains at the 0A-axis. This is because the incorporation of SK series resistors (such as R21 and R22) facilitates improved impedance matching between QL1 and QL2 in the two half-bridges, thereby enhancing the uniformity of current distribution.

These results conclusively demonstrate that SK series resistance is critical for achieving current sharing balance in gate drive circuit design.

4.3 Performance Analysis under High Tj

While previous analysis demonstrated satisfactory current sharing between QL1 and QL2 at 25°C junction temperature (Tj), the behavior at elevated temperatures requires examination. Figure 14 presents the double-pulse switching waveforms under Setting 2 at Tj = 150°C with the SK series resistors R21 and R22 are 1Ohm.

The results reveal that increased junction temperature does not compromise device paralleling performance. The system maintains both: (1) balanced current distribution, and (2) phase-synchronized turn-off current oscillations.

Therefore, these findings demonstrate that individual gate driver networks enable robust parallel operation of SiC MOSFETs across the entire specified temperature range.

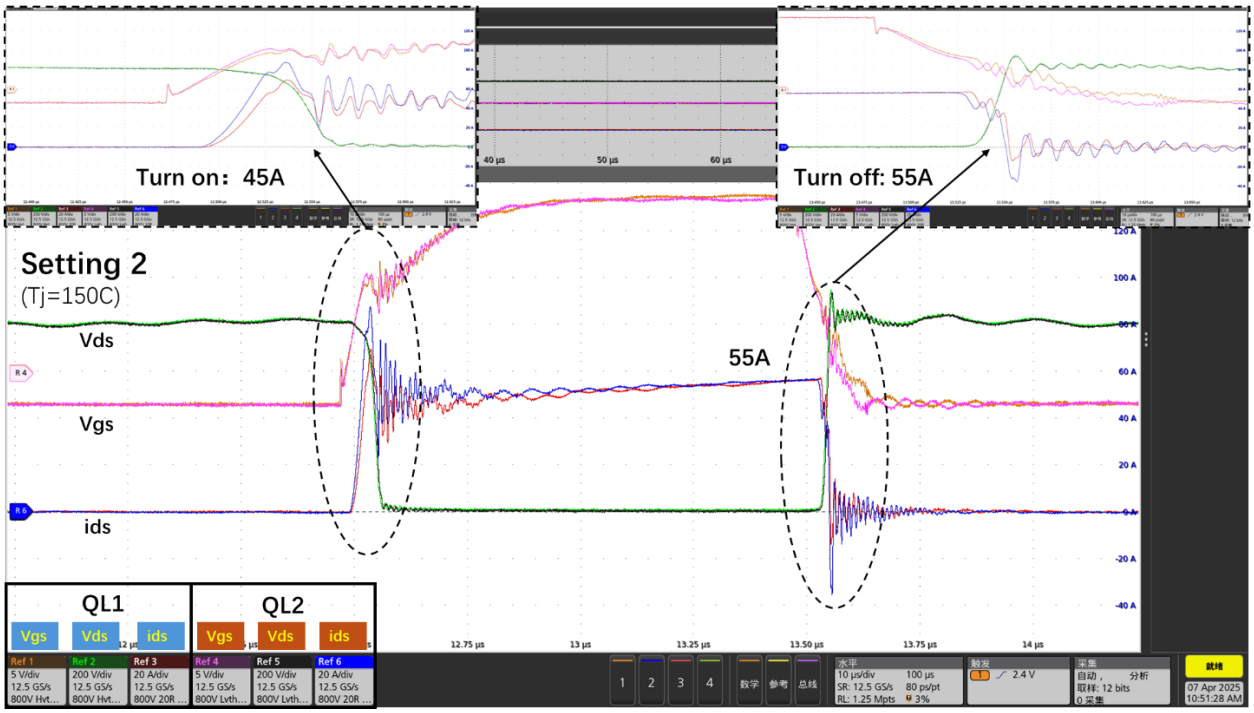


Fig. 14: The double-pulse switching waveform under Setting 2. (Tj=150℃)

5. Conclusion

This experimental study demonstrates the viability of parallel-connected SiC MOSFETs, through comprehensive investigations. A detailed analysis examines the operational characteristics of two distinct gate driver circuit configurations. The results reveal that implementing independent gate driver networks for each SiC MOSFET achieves: (1) uniform current distribution among paralleled devices, and (2) significant suppression of current oscillations.

Furthermore, the parallel-connected SiC MOSFETs exhibit synchronized switching behavior without observable loop currents. Subsequent experiments confirm that integrating SK series resistors improves impedance matching between QL1 and QL2 in the half-bridge configuration, thereby optimizing current-sharing performance. Additionally, the system maintains stable operation even at elevated junction temperatures (up to 150°C), demonstrating excellent thermal robustness.

Based on analytical and experimental results, this study provides critical insights for engineers designing gate driver circuits to ensure reliable parallel operation of SiC MOSFETs. Although the investigation focuses on two-device paralleling, the proposed driver architecture is inherently scalable and applicable to systems incorporating multiple parallel-connected SiC MOSFETs.

6. Reference

[1] https://navitassemi.com/wp-content/plugins/gb-navitas-stock-checker/product_files/G3F34MT12K.pdf

7. Revision history

Data	Status	Notes
June 16, 2025	Preliminary	Rev 1.1 Initial version

Additional Information

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