Wave Soldering Design Guide on WDPak-4L Package

Table of Contents

1. Introduction

This application note provides guidelines for wave soldering application of Navitas WDPak-4L package with bottom exposed pads including recommendations for printed-circuit board design as well as wave soldering condition.

2. Scope

Optimization of board assembly process is still required to ensure reliable solder joints on components considering moisture sensitivity level 3 (MSL3).

While this application note helps minimize unexpected failures, following the guidance in this document does not guarantee perfect assembly results. Outcomes may vary depending on machine capability, ambient conditions, materials, and other factors.

3. WDPak-4L Package

3.1 Package Description

WDPak-4L is a surface mount, gull-wing type plastic package with bottom-exposed pads as Fig.1. It is designed to maximize lead pitch and spacing for a stable wave soldering process including matte tin plating on the exposed pad and leads which is widely adopted for wave soldering applications due to its excellent cost-performance. Additionally, it is designed to maximize the exposed pad size for stable wave solder coverage and efficient heat dissipation of GaN and IC devices used in 400 V consumer applications.

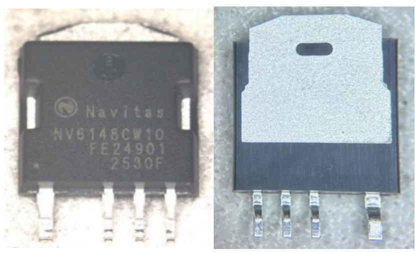
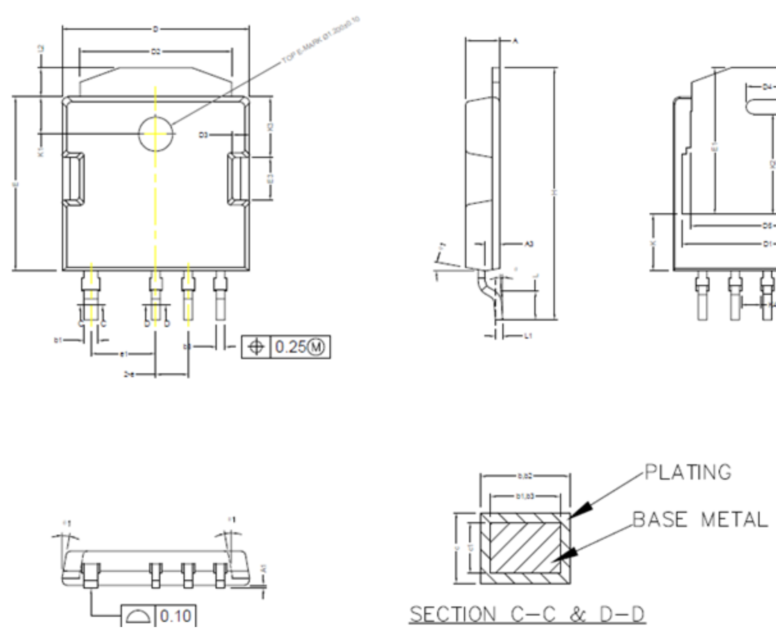


Fig. 1: Navitas WDPak-4L (6.6 x 6.1 x 1.2 mm)

3.2 Package Dimensions

WDPAK-4L package outline drawing must be referred to when designing the PCB layout. The lead frame thickness (0.25T) and signal lead width (0.3T) are designed to be thinner than those of a general DPak to maximize lead pitch and spacing. The package thickness (1.2T) is also reduced to minimize assembly cost but package body size is the same with the general one as shown in Fig.2



(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	–	0.15
A3	0.45	0.50	0.55
b	0.46	–	0.59
b1	0.45	0.50	0.55
b2	0.28	–	0.37
b3	0.27	0.30	0.33
c	0.24	–	0.31
c1	0.23	0.25	0.27
D	6.50	6.60	6.70
D1	5.80	6.00	6.20
D2	5.23	5.33	5.43
D3	0.50	0.60	0.70
D4		1.50REF	
D5	5.20	5.40	5.60
E	6.00	6.10	6.20
E1	4.94	5.14	5.34
E2		0.50REF	
E3	1.40	1.50	1.60
e	1.04	1.14	1.24
e1	2.18	2.28	2.38
H	8.64	8.84	9.04
K	1.83	–	–
K1	1.20	1.30	1.40
K2		3.52REF	
K3	2.02	2.12	2.22
K4	0.63	–	–
L	0.90	1.00	1.10
L1		0.25REF	
L2	0.92	1.02	1.12
θ	0°	–	8°
θ1	8°	10°	12°

NOTES:
1.ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Fig.2: WDPak-4L package dimensions

4. PCB Guidelines

4.1 PCB Material and Surface finishing

The substrates used for mounting packages can be fabricated from various materials with distinct properties, such as FR4, FR5, bismaleimide-triazine resin (BT), and flexible polymers (e.g., polyimides or polyamide).

There are no specific constraints for wave soldering applications, provided that the board can withstand the required wave soldering temperatures.

Common surface finishes include electroless nickel immersion gold (ENIG), organic solderability preservative (OSP), immersion tin (Sn), and hot air solder leveling (HASL). While these finishes may exhibit different appearances after soldering and some may demonstrate superior wetting characteristics, all standard finishes are acceptable as long as they comply with applicable specifications (e.g., IPC-A-610).

4.2 Solder Mask Design

There are two kinds of solder pad and solder resist design which are SMD (solder mask defined) and NSMD (non-solder mask defined).

SMD is a method of designing the solder resist to partially overlap the copper (Cu) landing pattern on the PCB. NSMD designs feature a gap between the solder resist and the Cu landing pattern on the PCB. These two types are described in more detail in Fig.3

For wave soldering, any of the solder mask configurations can be used without significant impact on the soldering outcome. NSMD is recommended in this document because it is an easier PCB manufacturing method. In the actual evaluation by Navitas, the SMD design showed a slightly better trend in reducing solder bridge risk among signal leads, but the difference was not significant.

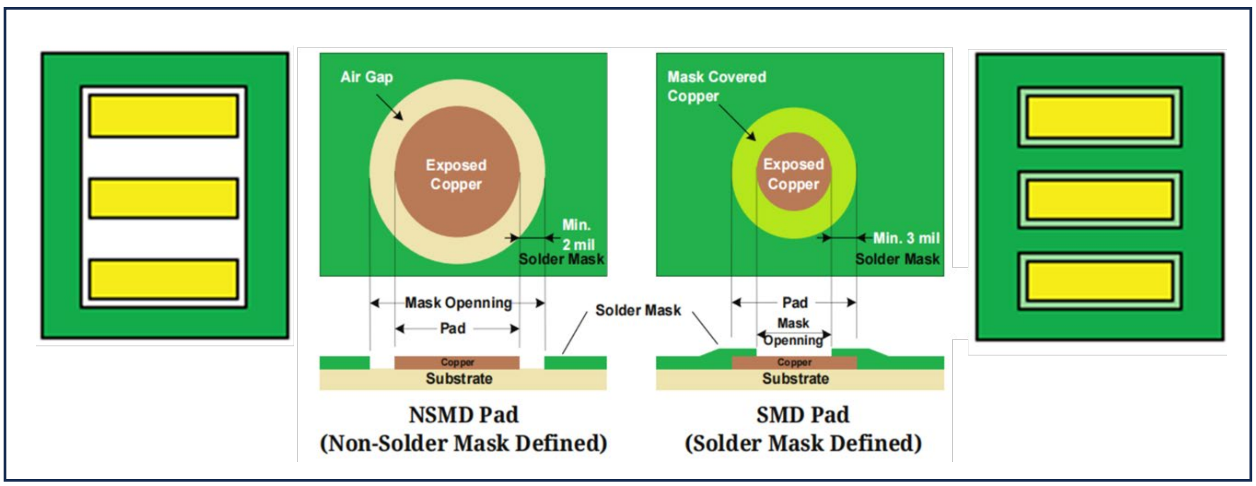


Fig. 3: NSMD vs SMD solder pad

4.3 Solder Thieves and Orientation Through the Wave

The use of "solder thieves" in PCB layout design is a well-established method for improving wave soldering quality, particularly for discrete packages. As illustrated in Fig. 4, this approach incorporates enlarged pads positioned at the end of each row of fine-pitch solder pads, along with proper orientation of the component relative to the solder wave. These enlarged pads, referred to as solder thieves, function to capture excess solder during the wave soldering process.
For optimal results, the component should be oriented such that its leads are perpendicular to the PCB travel direction during wave soldering.

For the Navitas WDPak-4L package, it is recommended to implement two solder-thief pads—one for the power lead and one for the signal lead—while maintaining the perpendicular lead orientation as shown in Fig. 5.

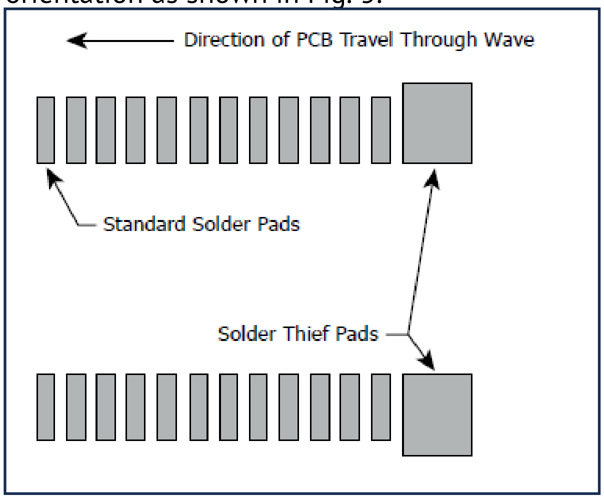


Fig. 4: Thieves and orientation concept (General)

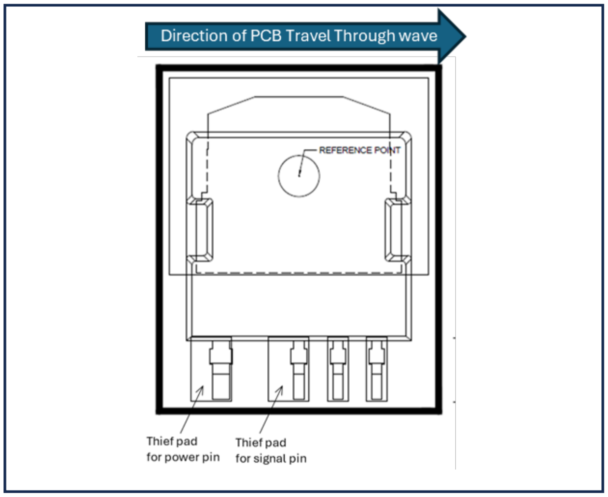


Fig. 5: The design concept for WDPak-4L

4.4 Solder Land Pad Design and Spacing Between Solder Pads

The WDPak-4L package is designed for compatibility with wave soldering processes, featuring a lead pitch of ≥1.14 mm and a narrow lead width of 0.3 mm to ensure sufficient spacing between leads. When used with advanced wave soldering equipment equipped with solder-bridging prevention features, the package can be reliably attached. For legacy or less sophisticated wave soldering systems, specific PCB and footprint layout considerations are recommended, as outlined in this document.

To minimize the risk of solder bridging, the spacing between solder pads should be maximized. At the same time, the pad layout and wave-soldering process must be carefully selected to ensure the formation of high-quality solder fillets on all sides of the lead "foot." The WDPak-4L solder pad can be designed with a minimum width of 0.6 mm, which allows for pad-to-pad spacing of up to 0.54 mm as shown in Fig. 6. Table 1 provides a comparison of package and solder pad layout dimensions.

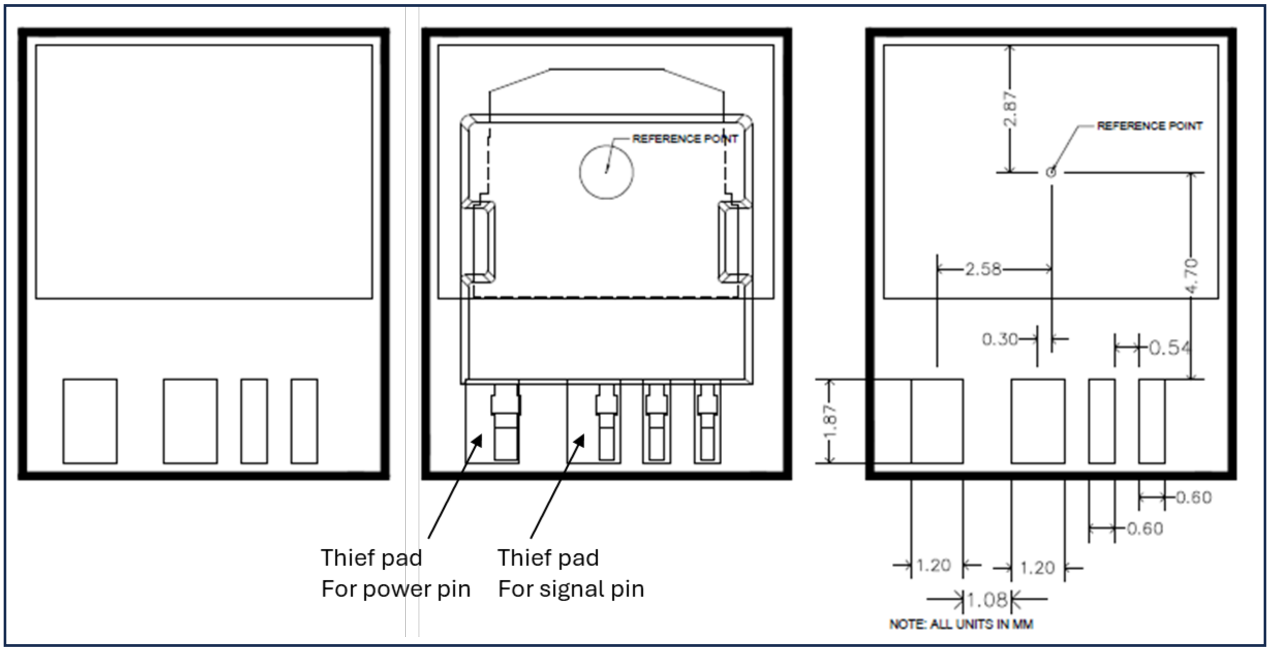


Fig. 6: Recommended wave soldering land pad design

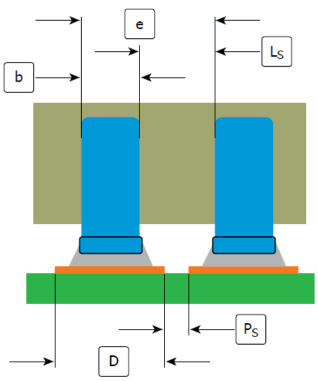


Fig. 7 Solder pad spacing

Layout Dimension(mm)	WDPak-4L	Standard Dpak-4L	Standard SOIC
Lead pitch (e)	1.14	1.14	1.27
Lead width (b)	0.30	0.60	0.40
Lead spacing (Ls)	0.84	0.54	0.87
Recommended Solder Pad Width (D)	0.60	Not Wave -Solderable	0.60
Solder Pad Spacing (Ps)	0.54		0.67

Table 1. Layout dimensions for wave solderable packages

5. Wave Soldering Process

5.1 Adhesive (Glue)

To secure components on the PCB during wave soldering, adhesive dots must be applied to bond the components to the board. The adhesive must meet the following criteria:

- **Tackiness and volume**: The glue must possess sufficient tackiness and volume to prevent component displacement without any overflow or detachment during transport from the pick-and-place machine to the curing equipment.
- **Post-cure adhesion**: After curing, the adhesive must maintain strong adhesion to ensure components remain fixed throughout the entire wave soldering process.

Adhesive can be applied using either printing or dispensing methods. To ensure improved planarity and consistent adhesive volume, Navitas's wave soldering investigations employed stencil printing with a stencil thickness of 0.1 mm (4 mil).

Adhesive must be cured according to the specified conditions of the supplier. Glue should be fully cured before wave soldering.

5.2 Solder Material and Solder flux

General wave soldering, the most common solder alloys used are lead-free alloys like SAC305 (tin-sliver-copper, 3% silver) or SAC0107 (tin-sliver-copper, 0.1% silver) and tin-lead (Sn-Pb) alloys, typically with a 63/37 or 60/40 composition. Lead-free options are favored due to environmental regulations, while tin-lead alloys offer excellent wettability and mechanical strength.

Lead-free alloys are preferred due to environmental regulations and compliance requirements. However, tin-lead alloys remain in use for their superior wettability and mechanical strength. When selecting lead-free alloys, the silver (Ag) content should be matched to the application:

- **Low silver content (e.g.,SAC0107)** :

  Recommended when drop shock resistance is critical and cost sensitivity is high.

- **High silver content (e.g., SAC305)** :

  Preferred for applications requiring enhanced thermal fatigue resistance and long-term reliability under temperature cycling.

Fluxing is necessary to promote wetting of both the PCB and the mounted components. It ensures good and even solder joints. After the fluxing process, the solder side of the PCB (including the components) is covered with a thin layer of flux. Flux can be applied to the PCB by spraying or foaming. It’s recommended to use a no-clean flux with low corrosive content, such as Rosin Mildly Activated (RMA) flux.

5.3 Wave Soldering Condition

Recommended wave soldering profile is described in Fig. 8 and Table 2.

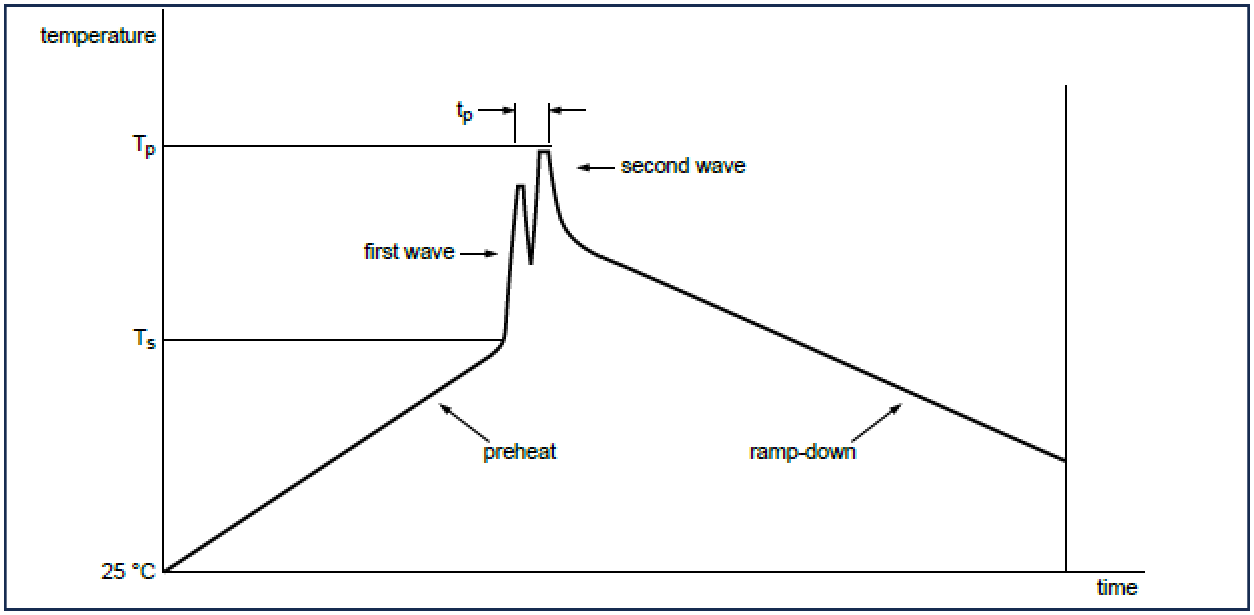


Fig. 8: Wave soldering profile

Profile Feature	SnBb eutectic assembly	Pb-free assembly
Average ramp-up rate	~ 200 °C/s	~ 200 °C/s
Heating rate during preheat	1°C/s to 2 °C/s typical, 4 °C/s maximum	1°C/s to 2 °C/s typical, 4 °C/s maximum
Final preheat temperature T_s	~ 130 °C	~ 130 °C
Peak temperature T_p	235 °C	260 °C
Maximum time within peak temperature t_p	10 s	10 s
Ramp-down rate	5 °C/s maximum	5 °C/s maximum

Table 2. Wave soldering parameters

5.4 Navitas Wave Soldering Trials

Navitas conducted third-party wave soldering trials for the WDPak-4L package using two solder alloys (SAC305 and SAC0107) and two PCB design types (SMD and NSMD). These trials were performed in accordance with the previously described designs, recommendations, and guidelines. The results demonstrated consistently good performance in adhesive printing, component placement, solder bridging prevention, and solder coverage, as summarized in Table 3.

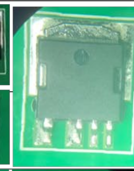
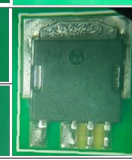
LEG	Wave solder material	PCB design	Wave soldering result		Remark
			Solder bridging and component placement	Solder coverage	
#1	SAC305 (High Ag content)	SMD	 		- No solder bridging or component placement issue were observed. - The total solder void level remained below 5%, with no voids detected in the die area.
#2	SAC0107 (Low Ag content)	SMD			
#3	SAC305 (High Ag content)	NSMD	 		
#4	SAC0107 (Low Ag content)	NSMD			

Table 3. Wave Soldering Trials

Additional Information

DISCLAIMER Navitas Semiconductor (Navitas) reserves the right to modify the products and/or specifications described herein at any time and at Navitas' sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied. This document is presented only as a guide and does not convey any license under intellectual property rights of Navitas or any third parties. Navitas' products are not intended for use in applications involving extreme environmental conditions or in life support systems. Terms and Conditions.

Navitas, GaNFast, GaNSense, GeneSiC, and the Navitas logo are trademarks or registered trademarks of Navitas Semiconductor and subsidiaries. All other brands, product names, and marks are or may be trademarks or registered trademarks used to identify products or services of their respective owners.

Contact: info@navitassemi.com