GaNSafe Application Note

Due to increased need of high efficiency and high-power density in industrial power systems, wide-bandgap semiconductors such as silicon carbide (SiC) MOSFETs and gallium nitride (GaN) based high-electron-mobility transistor (HEMT) have become a necessity. Navitas offers various GaN power ICs for these demanding high-power applications in solar/energy storage and EV markets and for the rapid deployment of artificial intelligence (AI) into global data centers. This application note introduces one of the Navitas GaN ICs, GaNSafe™, and details how to make a reliable design with GaNSafe.

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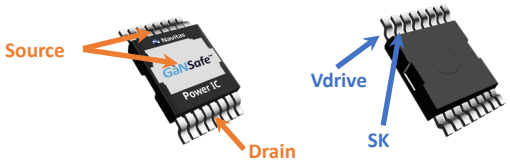
1. GaNSafe package

GaNSafe can switch at significantly faster switching speeds compared with silicon and SiC MOSFETs. Higher switching speeds come with a penalty of higher electromagnetic interference (EMI) and to counter this, GaNSafe ICs come with a range of features to increase noise immunity for the gate driver under high frequency switching conditions and helps avoid false trigger of FET gate. This proves a significantly more optimal solution versus those based on standard discrete GaN FETs.

High power systems require low package parasitic inductance to reduce gate ringing, additionally packages must be able to dissipate heat efficiently. Navitas has therefore released these products in industry-standard TOLL leadless bottom-side cooling and TOLT leaded top-side cooling packages to meet the demanding requirements of high frequency and high power applications.

TOLL	TOLT
	
Dimensions:11.68x9.9x2.3mm	Dimensions: 15x9.9x2.3 mm

2. GaNSafe features and internal operation logic

2.1 GaNSafe notable features

The GaNSafe power IC is the industry's first GaN power device to integrate both driver and critical protection. These features allow for high-speed operation and improve both product reliability and robustness and have been implemented in an industry-standard 4-pin package (drain / source / V_{DRIVE} / SK) – see Figure 1.

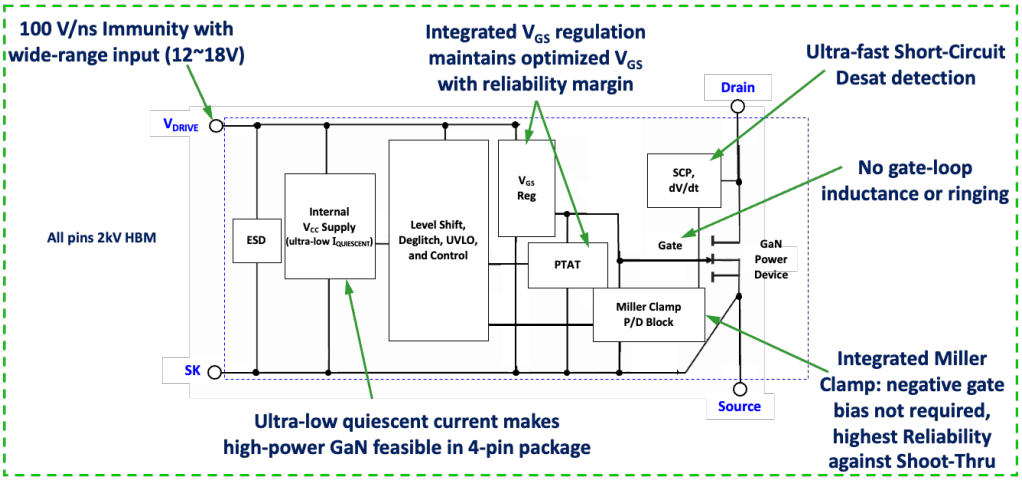


Fig. 1: GaNSafe Block Diagram

Notably, GaNSafe power ICs have an internal bias power V_{GS}, and this furthermore, has a positive temperature coefficient (PTC) to optimize V_{GS} over - 40oC to +150oC junction temperature. This maintains V_{GS} close to the optimal 6.7 V and below 7.0 V for lifetime reliability constraint, which improves GaNSafe's current capability under high temperature.

Due to the GaN's reduced short circuit withstand time (SCWT), it's critical to have integrated short circuit protection. GaNSafe therefore is able to detect the voltage between the drain and source during turn-on, and once the V_{DS} voltage is higher than V_{DSscp} threshold, typically 13.5v, the protection circuit is triggered to safely shut down the device.

2.2 V_{DRIVE} power supply design

To achieve these advanced features within only four terminals, GaNSafe has been designed to harvest energy from the V_{DRIVE} pin while receiving the PWM signal by means of an internal level shifter.

Because GaNSafe are powered from the PWM signal, the external driver must provide a current sourcing capability of ⩾500mA. The V_{DRIVE} pin voltage is rated for 10 V to 18 V, with the GaNSafe V_{GS} regulation circuit able to scale down the drive voltage to the level required without the need for external components. However, a V_{DRIVE} voltage plateau ⩾11V is strongly recommended to guarantee all functions (dv/dt slew rate over temp, SCP, etc.) and full details are available via the datasheet.

For half-bridge configurations that implement a bootstrap circuit to power the high-side switch it's important to note that the amplitude of high side V_{cc} is the sum of low side V_{cc} and the reverse conduction voltage of the low side GaN device.It should not exceed 18V.

GaNSafe ICs come with an integrated driver, but only requires the same pin-out as discrete GaN, which creates its easy-to-use configuration. This can be seen in figure 2, which shows the typical GaNSafe driver circuit. This is almost identical to those used in discrete gate driver circuits, with the only difference being a 47~100 pF recommended decoupling cap between the V_{DRIVE} and SK pins.

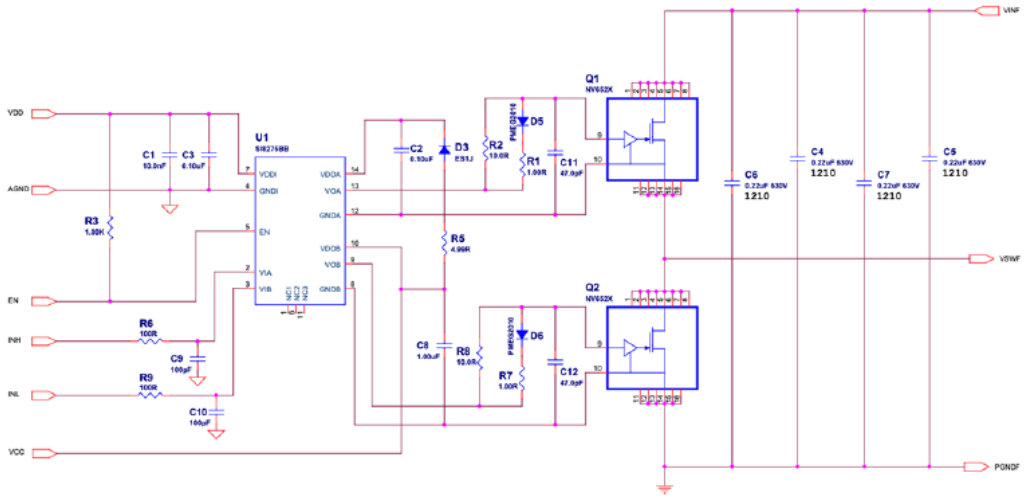


Fig. 2: GaNSafe typical charge pump drive circuit design

A typical V_{DRIVE} pin waveform can be seen in figure 3. This shows the external driver is able to charge the internal GaN gate after a c.30 ns propagation delay with the GaNSafe IC starting to turn on and the V_{DS} starting to decrease at time T1. A subsequent voltage dip on the V_{DRIVE} pin can be observed, caused by the charging current flowing through an external turn-on resistor, and at time T2, the GaNSafe is fully turned on with an internal gate voltage of 6.7 V.

Between times T2 and T3, the charging current decreases, and the V_{DRIVE} voltage returns to the external driver PWM supply level. To maintain normal function for the internal circuit, the V_{DRIVE} voltage should remain above 8.5V throughout the T1 to T3 interval. Consequently, based on the internal operation algorithm, the minimum V_{DRIVE} on-time pulse duration is specified as 75 ns.

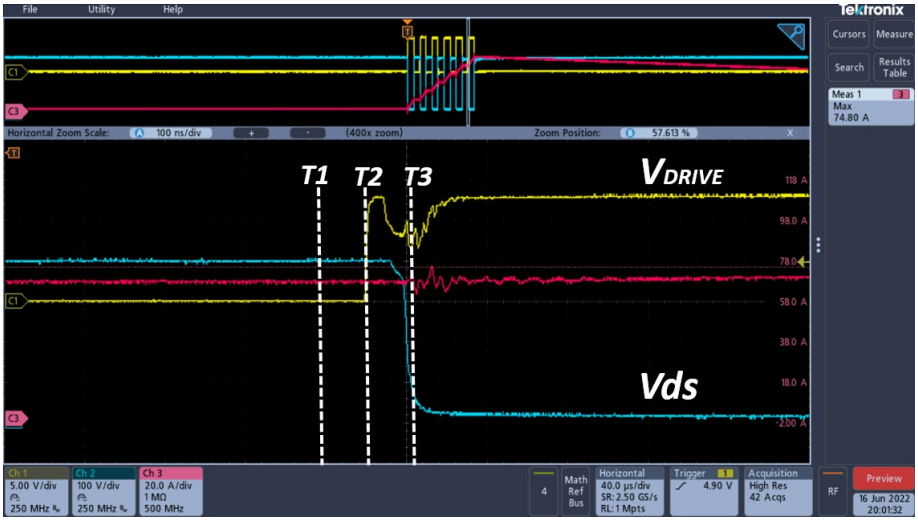


Fig. 3: V_{DRIVE} typical waveform

The IC's internal Miller clamp and pull-down circuit prevents voltage bounce on the internal GaN gate to avoid a mis-trigger under high dv/dt conditions during turn-off. As a result, the negative drive voltage is not required, which further improves the robustness, long-term reliability and system efficiency.

3. GaNSafe layout design guideline

GaN HEMTs have significantly improved figures of merit versus traditional silicon power transistors and are able to switch far faster as a result. However, the higher switching speed results in an extremely high dv/dt and di/dt, which makes PCB layout design more challenging. This is especially true under the hard-switching conditions and to achieve both optimal switching performance and high reliability, proper routing of the power loop and gate drive loop are critical, as is the use of interlayer shielding.

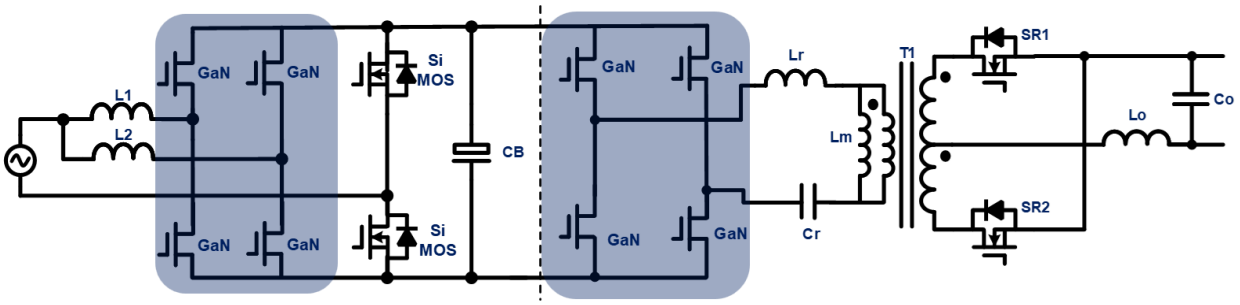


Fig. 4: 3.2kw CRPS185 80 PLUS Titanium PSU topology diagram

Figure 4 shows a 3.2 kW CRPS185 PSU design with the GaNSafe ICs used as part of the interleaved totem pole PFC and full bridge LLC. This delivers a power density of 98 W/in^3 and 80 PLUS Titanium-class efficiency.

The switching frequency of the totem pole PFC is 65 kHz, and the resonant frequency of full bridge LLC is 300 kHz, with the PCB layout guidelines given based on the 3.2kw CPRS185 PSU daughter card design.

As a direct result of the GaNSafe power ICs' unique internal structure, it is no longer essential for these to be positioned in close proximity to the external driver IC. All the GaNSafe components can therefore be placed on the daughter card, rather than the main board, which offers more layout flexibility. The circuit layout is shown in figure 5 with the critical components highlighted in the diagram.

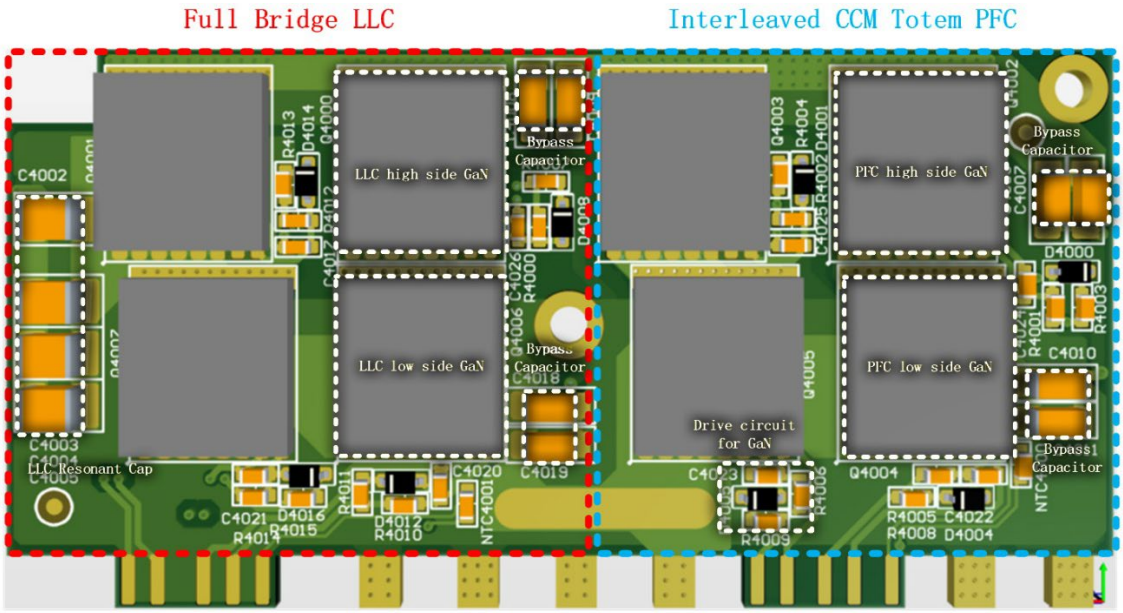


Fig. 5: 3.2kw CRPS185 daughter card

3.1 Component placement and routing

Parasitic inductance in power switching circuits can lead to high voltage overshoot, oscillation, and severe EMI, which would subject the GaN devices to excessive electrical stress.

Countering this uses the same methodology as would be used in traditional silicon power transistors. The scale of the parasitic inductance depends on the length of the high frequency current loop, and therefore the high-side and low-side GaN FETs as well as the multi-layer ceramic bypass capacitors should be placed together to make the high frequency loop as small as possible. This is shown in figure 6, with the yellow line showing the smallest high frequency current loop.

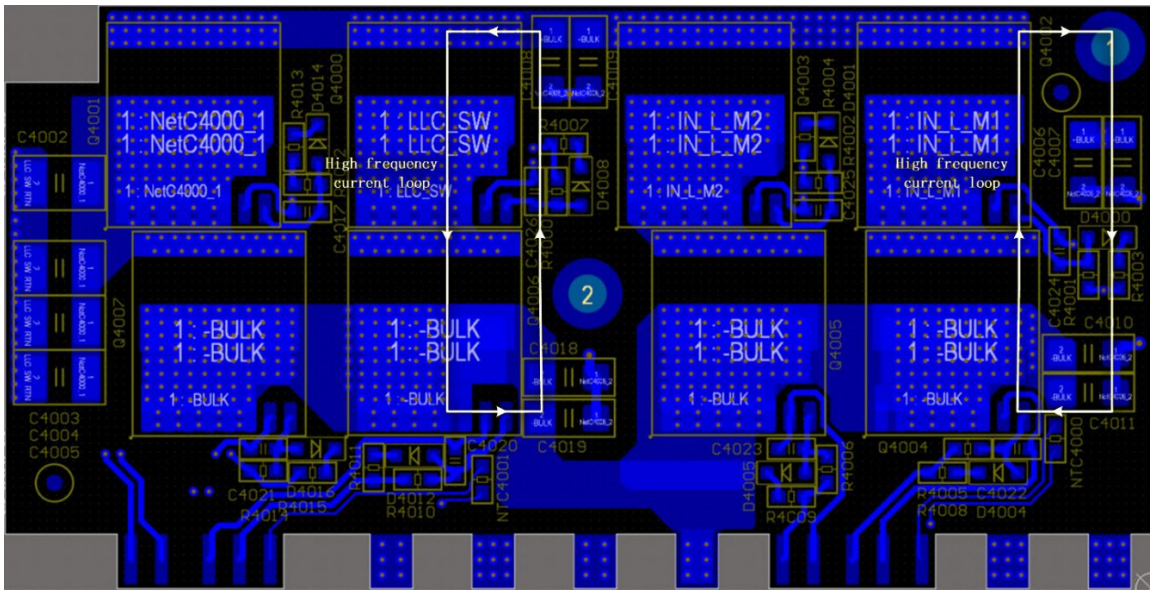


Fig. 6: PCB layout of 3.2kw CRPS185 daughter card

3.2 Gate drive placement and shielding

Parasitic loop inductance in the gate driver circuit can lead to gate oscillations, which can in turn cause voltage overshoot and mis-trigger the FETs. As a result, when using discrete GaN, it is essential to locate the driver circuits, including the driver IC as close to the FET as possible. This is not the case for Navitas GaNSafe.

Because GaNSafe integrates both the gate driver and the gate protection circuitry, the internal gate-source loop inductance is almost zero. This provides a significant degree of flexibility to the placement of the external PWM driver. In the above example, this allowed the driver IC to be positioned on the main board, away from the GaNSafe daughter card, to provide a greater heat dissipation area and improve thermal performance.

The final design challenge is switching noise, caused by high dv/dt or di/dt. This affects the driver and sampling signals through parasitic capacitance and to reduce its negative effects, a shielding layer between the drive circuits (turn-on and turn-off resistors) and the switch node is essential. For GaNSafe, it is recommended to both use the Kelvin source pin to create a shielding plane on the layer directly beneath the device, as illustrated in Figure 7, and to avoid any overlap or interaction between the shielding plane and the high-side or low-side GaN device power source plane.

Additionally, in order to increase V_{DRIVE} pin noise immunity in GaNSafe devices, it is recommended to place a 47~100 pF 0402 MLCC between and directly adjacent to the SK and V_{DRIVE} pins.

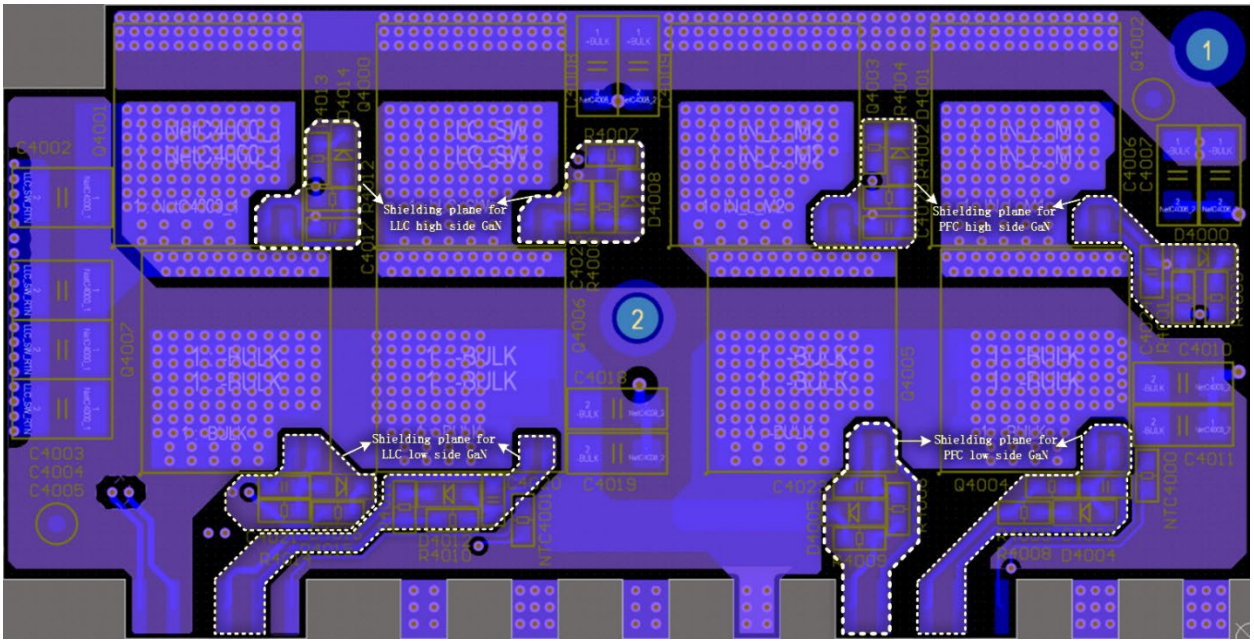


Fig. 7: GaNSafe shielding plane design

Additional Information

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