PCIM ASIA

Navitas *Energy, Driven*

DRIVING FOR ZERO SWITCHING LOSS POWER SOLUTIONS

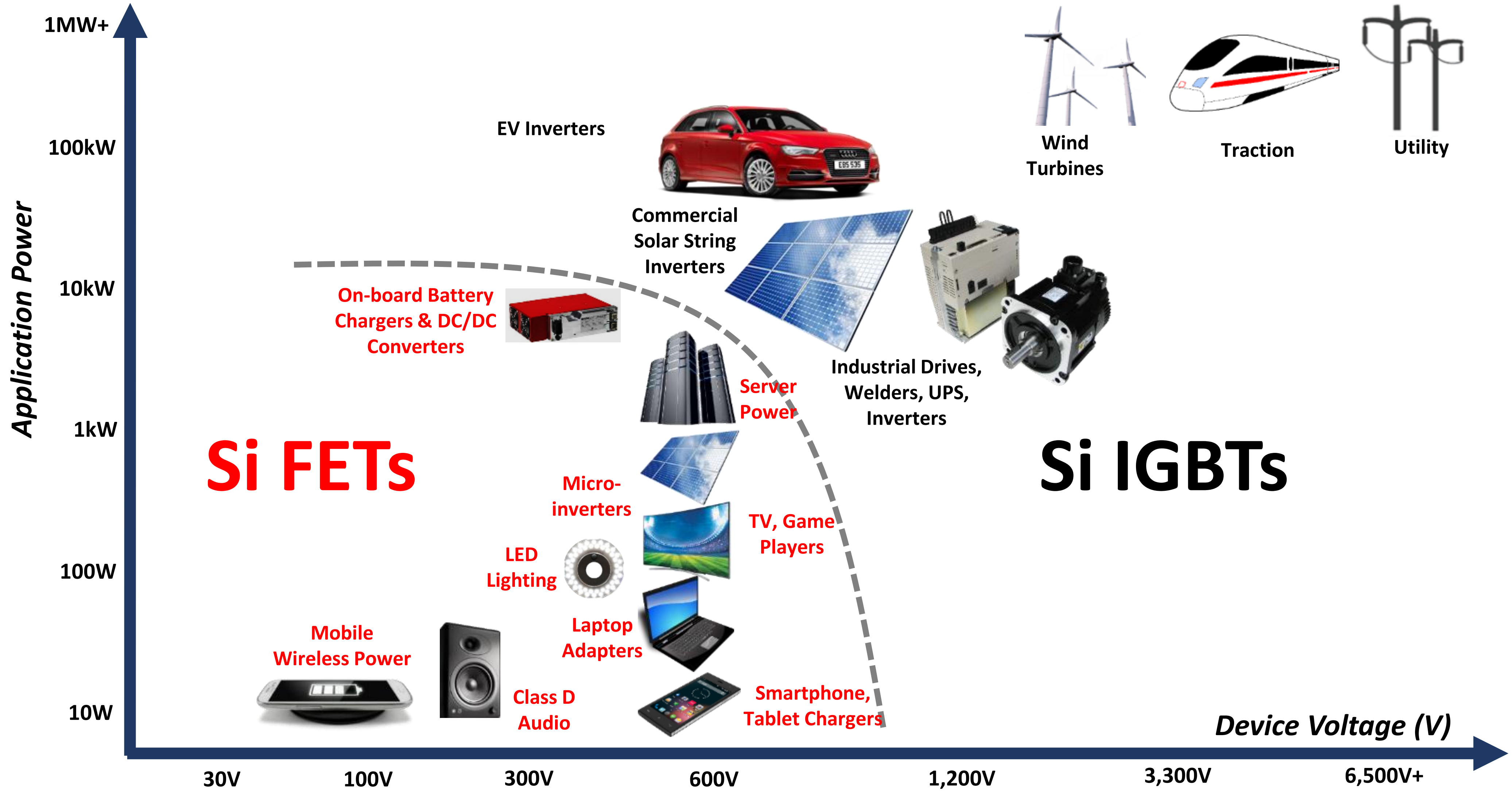
Dan Kinzer, CTO

June 28th 2016

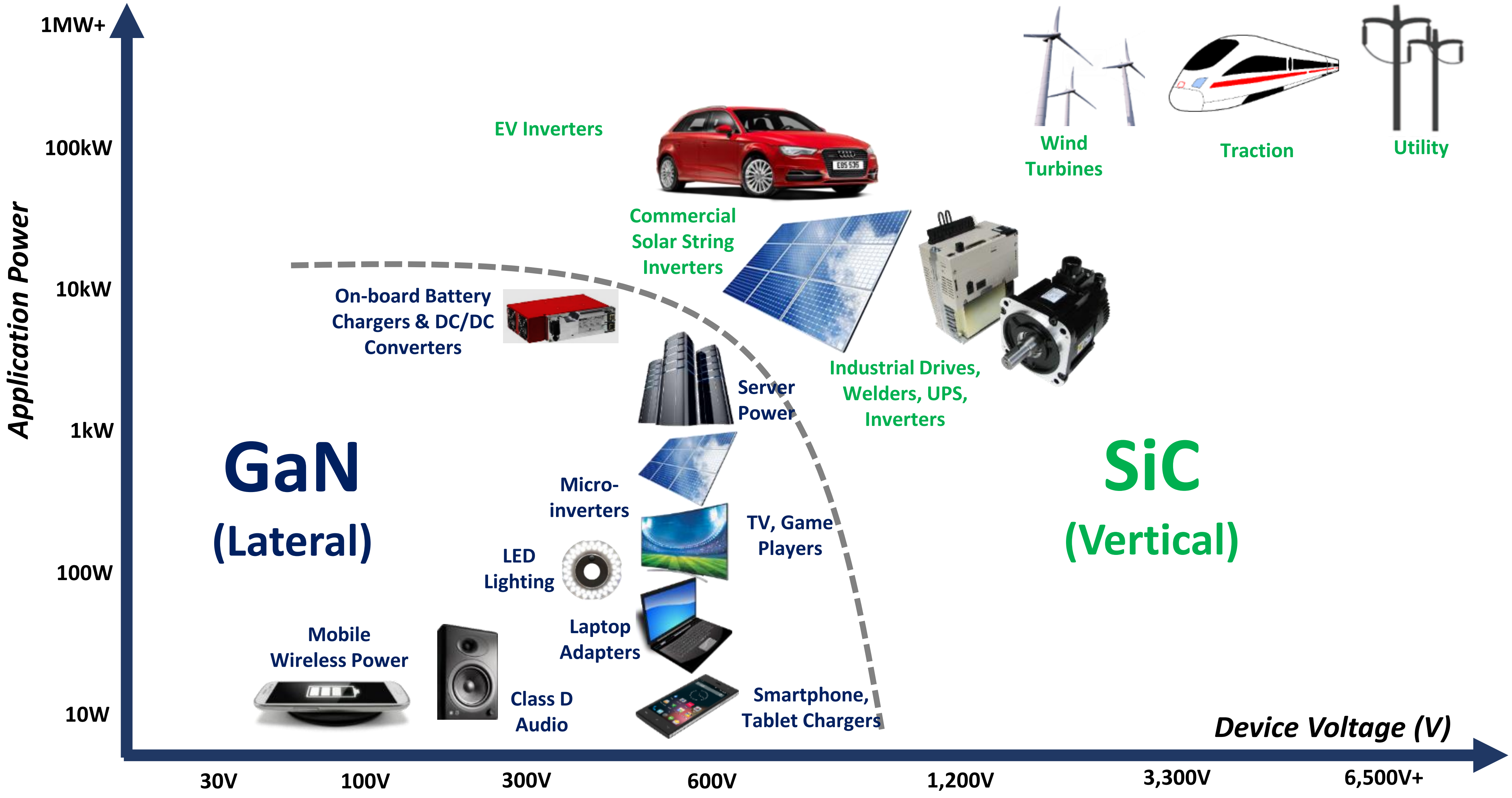
上海国际赛车场

Shanghai International Circuit

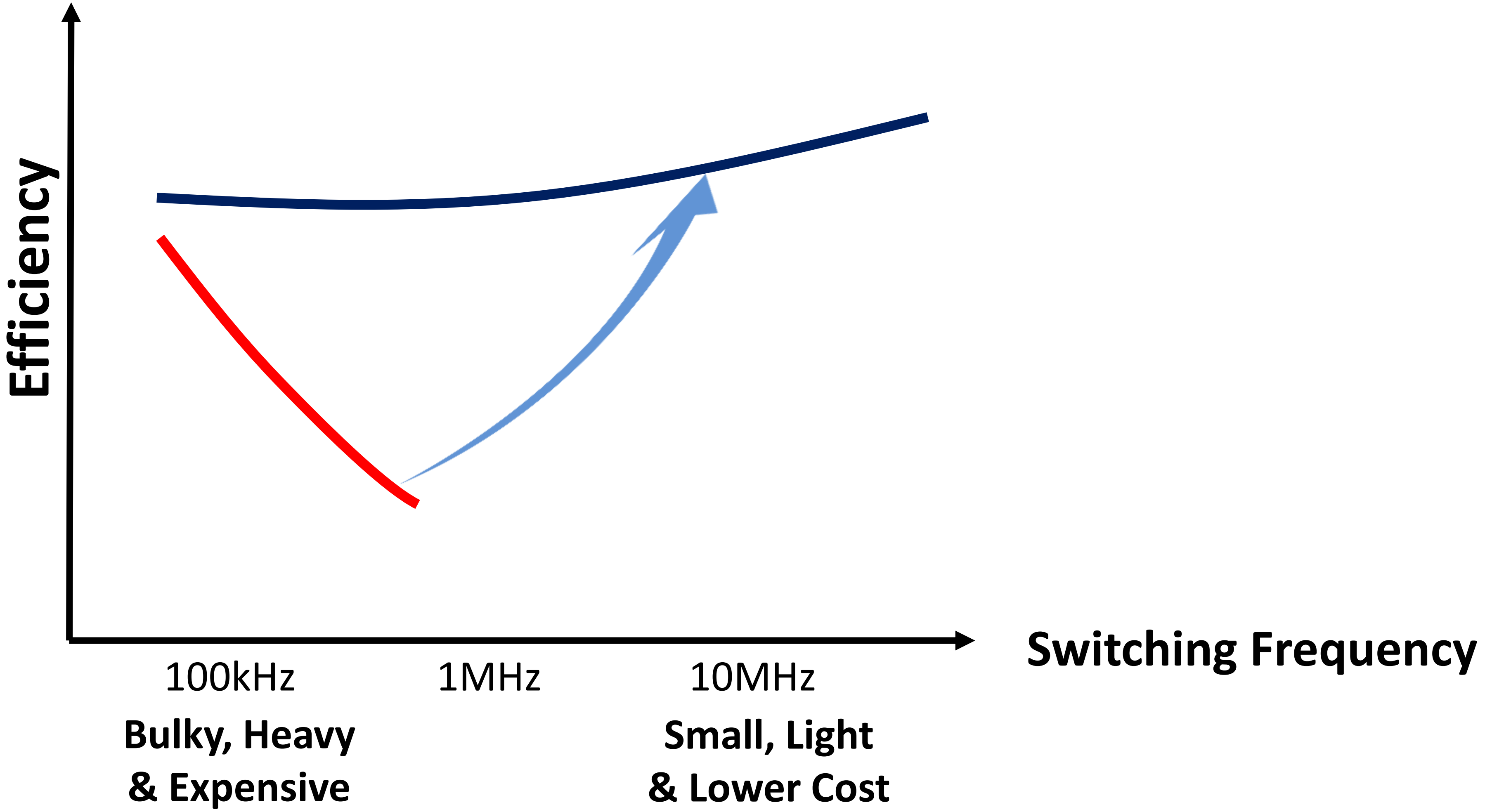
The Si Landscape



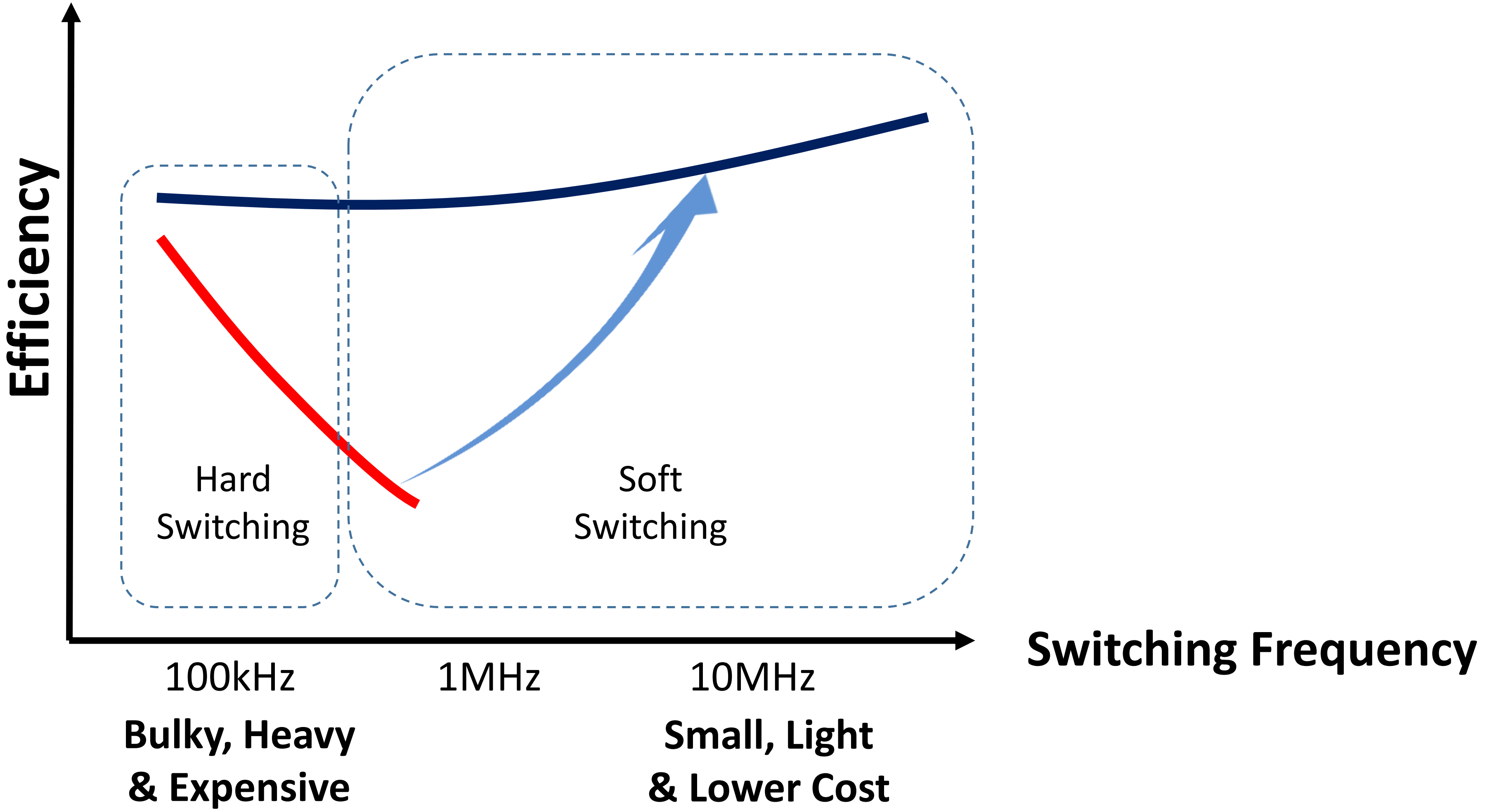
The WBG Landscape



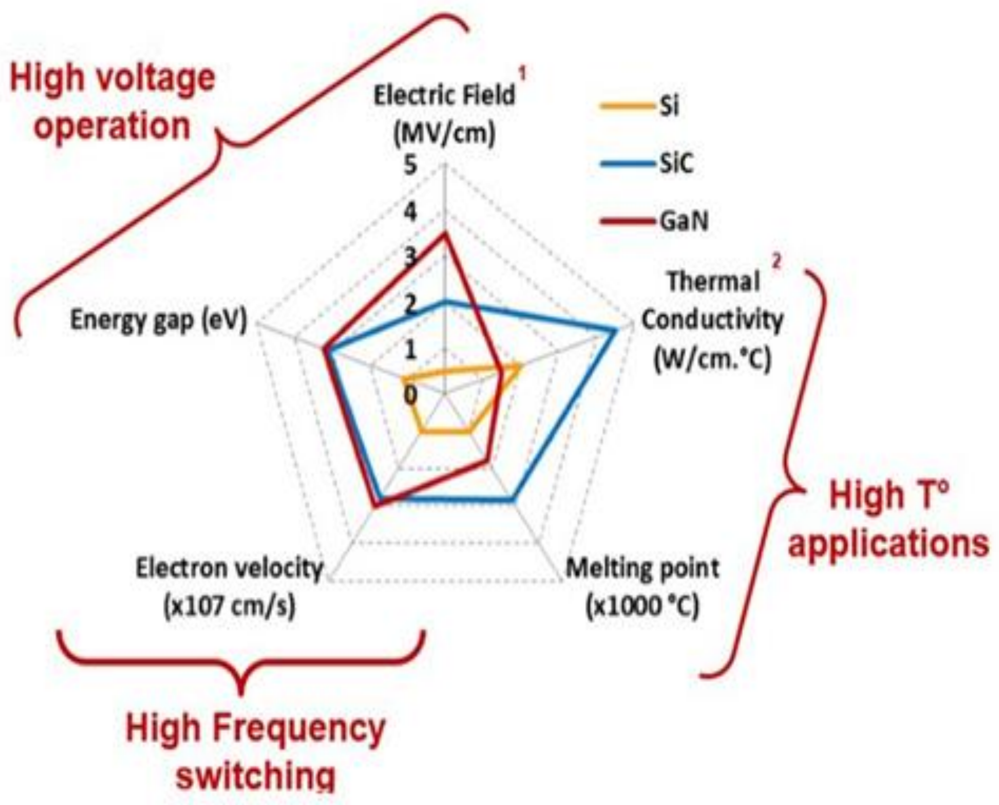
Driving to Higher Speeds



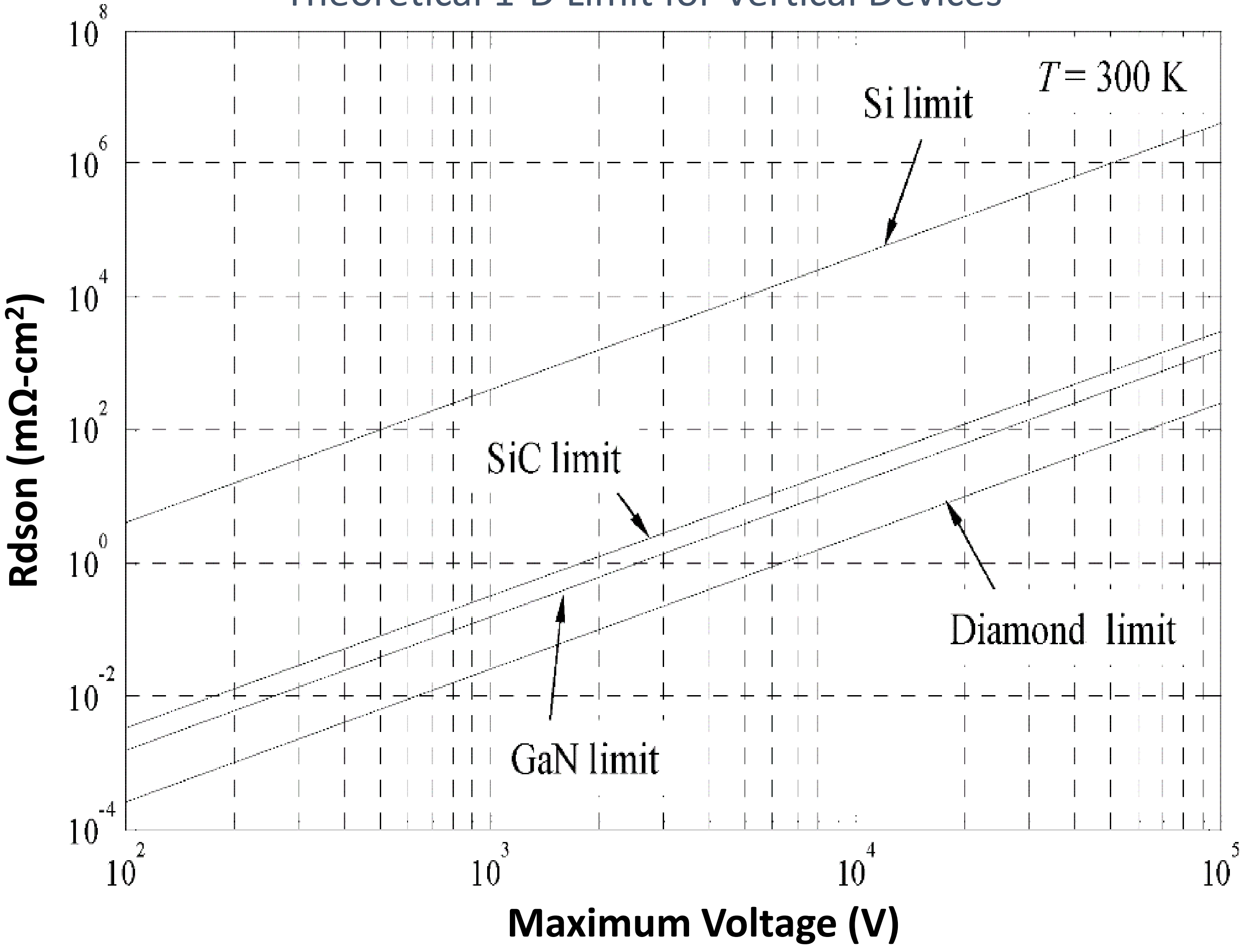
Driving Styles



Performance Limits of WBG Vertical Devices

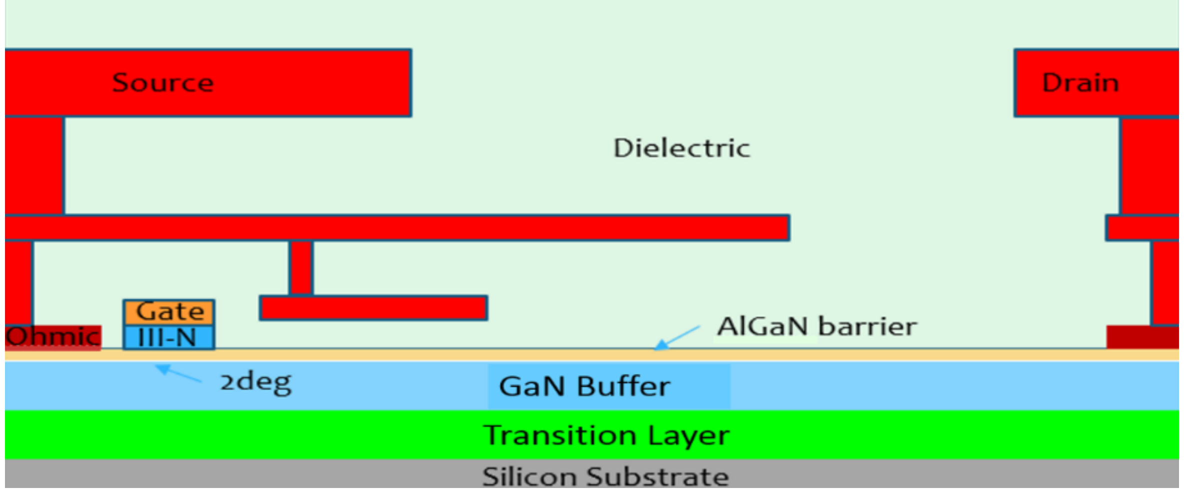


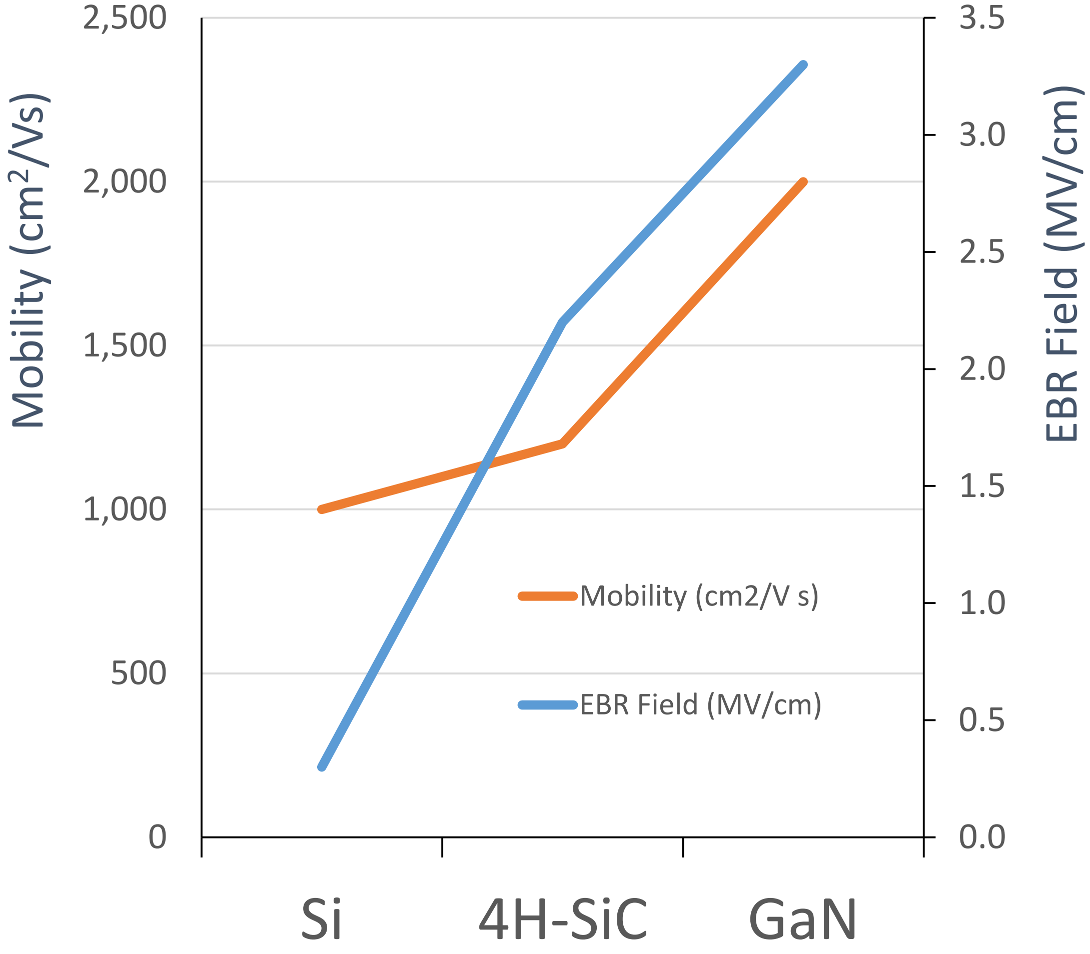
Theoretical 1-D Limit for Vertical Devices



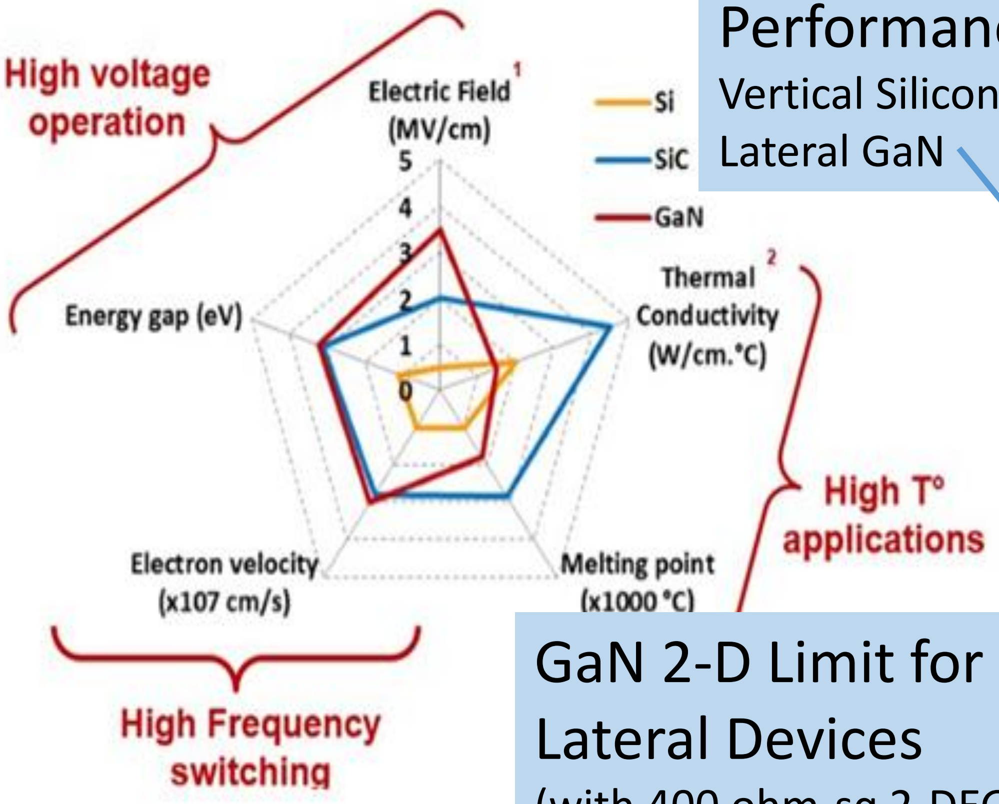
Lateral GaN Advantage for Off-line Applications

- WBG GaN material allows high electric fields so high carrier density can be achieved
- Two-dimensional electron gas with AlGaN/GaN heteroepitaxy structure gives very high mobility in the channel and drain drift region
- Lateral device structure achieves extremely low Q_g and Q_{OSS} and allows integration
- Integration on silicon substrates means mature low cost wafer fabrication is available

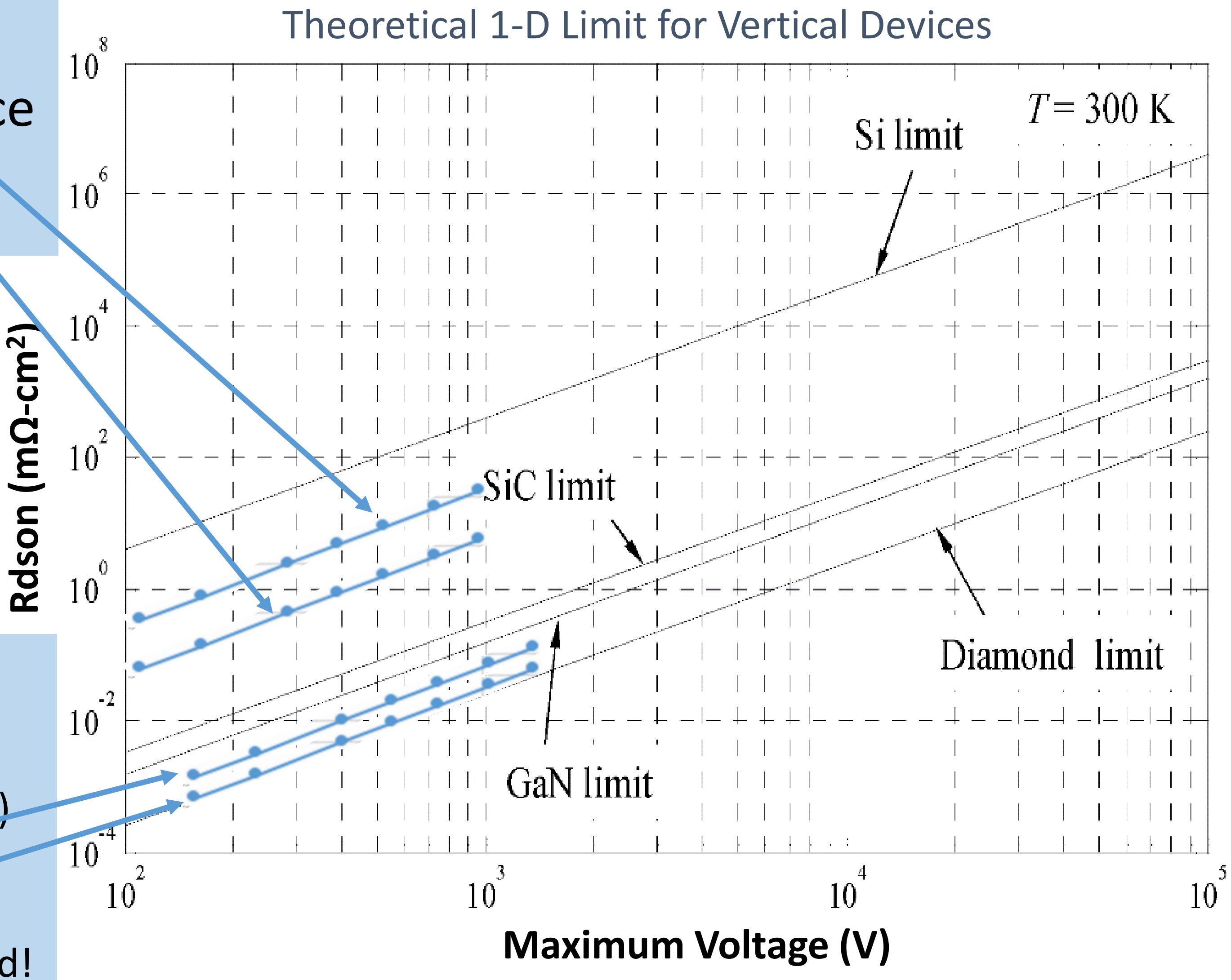




Performance Limits of WBG Materials



Current Performance
Vertical Silicon
Lateral GaN

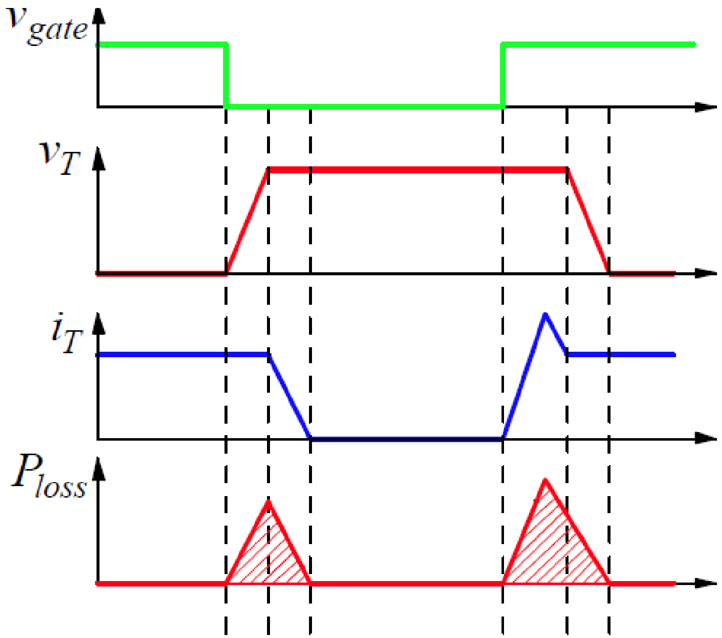


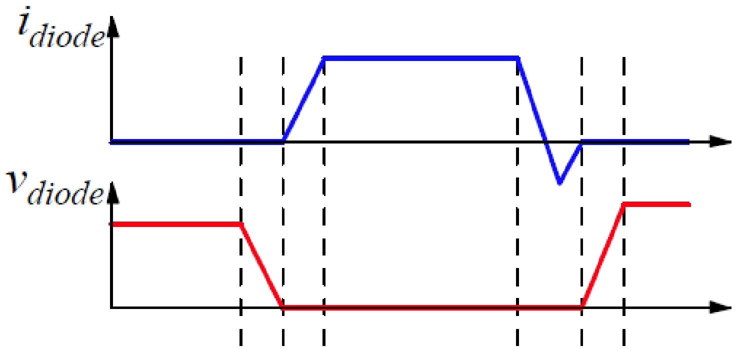
GaN 2-D Limit for Lateral Devices
(with 400 ohm-sq 2-DEG)
2.5MV/cm
3.5MV/cm
Almost matches Diamond!

Hard-Switching

Primary Switch Power Loss:

$$P_{FET} = P_{COND} \quad + P_{DIODE} + P_{T\text{-}ON} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$





$$\boxed{P_{sw} \propto f_s\left[t_{c(on)} + t_{c(off)}\right]}$$

Circuit diagram: "Soft-Switching in DC-DC Converters: Principles, Practical Topologies, Design Techniques, Latest Developments", Mohan, Ayyanar, Persson, APEC 2002

Si: High C_{OSS} = Long ZVS Transition = Trapped Energy

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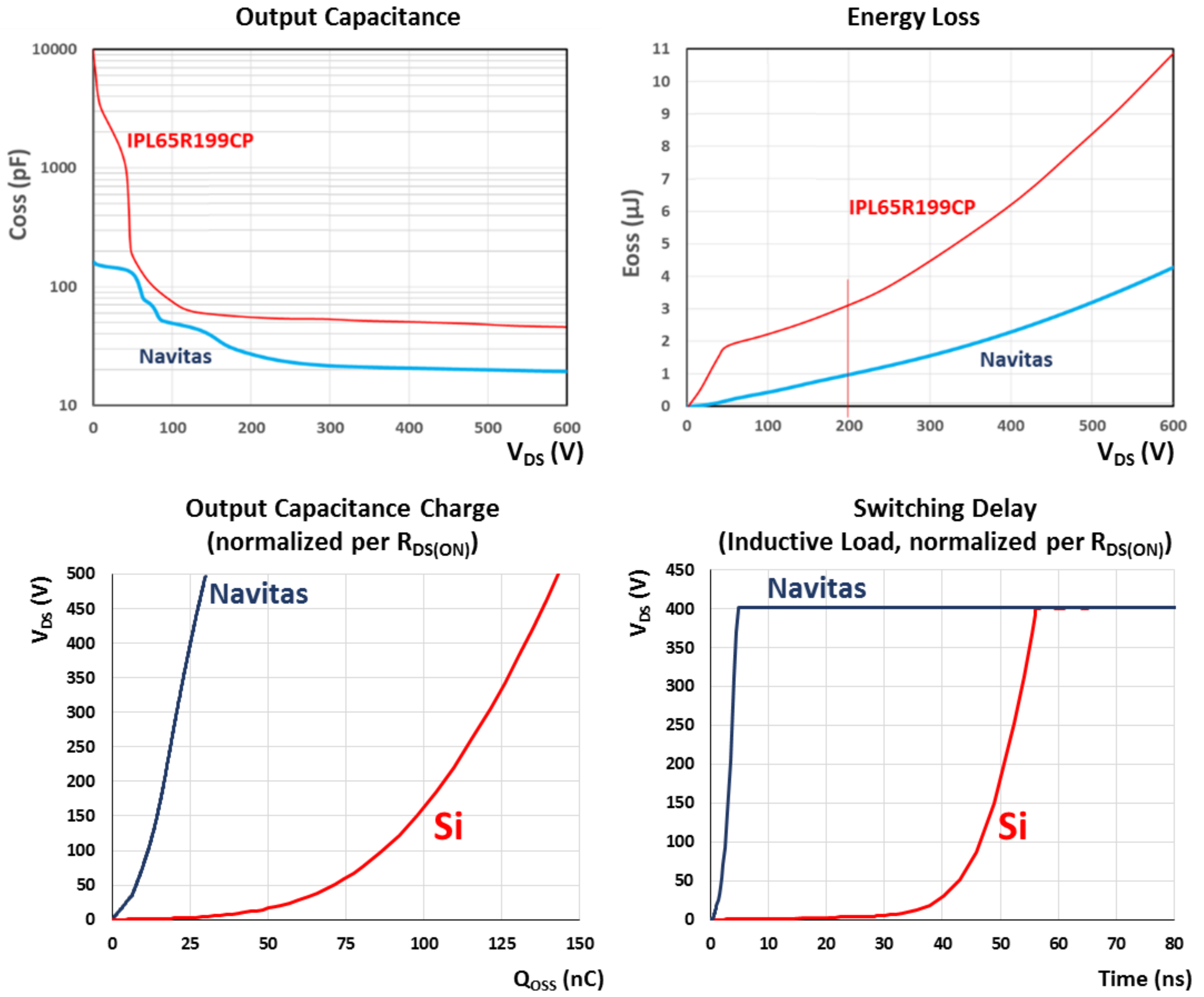
- Hard Switching loss:
  $P_{LOSS} = E_{OSS} * F_{SW}$
- High C_{OSS} → Delay (limits F_{SW})
- Too slow → partial ZVS → **E_{OSS} loss**

- Si Superjunction C_{OSS} is 50x-100x higher than GaN at V_{DS} < 30V
- Si SJ Eoss is 3x higher than GaN at 200V (partial ZVS)
- Si SJ also has a high effective series resistance (ESR) and a lossy, hysteretic output capacitance, so even soft switching won't save it at high frequency



Soft Switching with Si

Primary Switch Power Loss:

$$P_{FET} = P_{COND} * k + P_{DIODE} + \cancel{P_{T\text{-}ON}} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

- k-factor 2 (or more) due to increased circulating current, duty cycle loss, high C_{OSS}
- $P_{T\text{-}On}$ = 0 (soft, zero voltage switching)
- P_{Qoss} ↓ 2-3X (most energy stored in output capacitance is recovered)

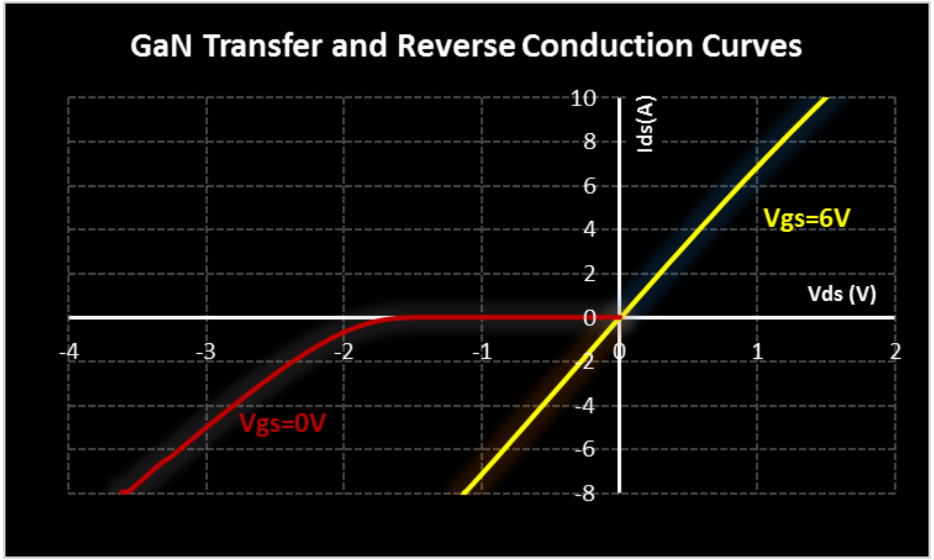
ZVS LLC – Critical Parameters

	Si	Cascode GaN	eMode GaN
Partnumber	IPL60R199CP	TPH3206LD	Navitas
Voltage (V)	600	600	650
$R_{DS(ON)}$ (typ, mOhm)	180	150	160
Q_G (typ, nC)	32	6.2	2.5
C_{OSS}(er) (typ, pF)	69	64	30
C_{OSS}(tr) (typ, pF)	180	105	50
t_{rr} (typ, ns)	340	17	**0**
Q_{rr} (typ, nC)	5,500	54	**0**
$R_{DS(ON)}$ x C_{OSS}(er) (mOhm.pF)	12,420	9,600	**4,800**
$R_{DS(ON)}$ x C_{OSS}(er) (mOhm.pF)	32,400	15,750	**8,000**

- Dead-time (t_d) and magnetizing current (I_m) discharge C_{OSS} to achieve ZVS* $\left(C_{OSS} \approx \frac{I_m td}{2VIN}\right)$
- eMode GaN has 2x-4x smaller C_{OSS}-related metrics than Si, cascode GaN
- Higher efficiency, higher frequency operation
- At 1MHz, GaN Q_G is so low, ***gate drive loss ~zero***

* "Evaluation and Application of 600 V GaN HEMT in Cascode Structure", X. Huang, et al, VPT, IEEE Transactions on Power Electronics, Vol. 29, No. 5, May 2014

GaN Q_G and Reverse Conduction



- Reverse Conduction
  - LLC converters need low stored energy in output capacitance to sustain resonant transitions at light load
  - Need low Q_{rr} and fast, robust body diode characteristics to avoid shoot-through current, peak drain-source voltage, and reverse recovery dv/dt*
  - eMode GaN has no PN junction, so no minority carriers are injected and stored charge
  - ***Q_{rr}, t_{rr}, i_{rr} ~zero***

* "New power MOSFET technologies optimized for efficient and reliable telecommunication power system", W. Choi et al, Fairchild, APEC 2012

Soft-Switching with eMode GaN

Navitas

Primary Switch Power Loss:

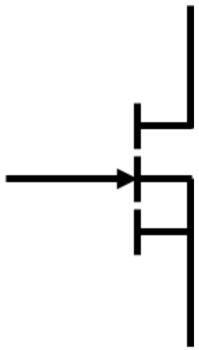
Minimized Reduced

$$P_{FET} = P_{COND} * k + P_{DIODE} + \cancel{P_{T\text{-}ON}} + P_{T\text{-}OFF} + \cancel{P_{DR}} + \cancel{P_{QRR}} + \cancel{P_{QOSS}}$$

- k-factor >1 (less than Si) due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓10X ~~2-3X~~ (GaN C_{OSS} charging/discharging loss negligible up to 2MHz)
- P_{DRIVER} ↓10X (GaN P_{DR} negligible up to 2MHz)
- P_{QRR} = 0
- P_{DIODE} ↓2X (reverse conduction loss reduced by synchronous rectification)
- $P_{T\text{-}OFF}$ = Reduced (limited by I-V crossover loss due to drive loop impedance)

Creating the World's First AllGaN™ Power ICs

Fastest, most efficient GaN Power FETs



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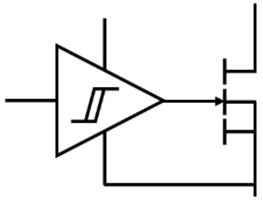
First & Fastest Integrated GaN Gate Driver



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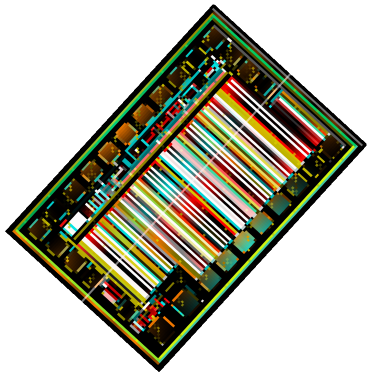
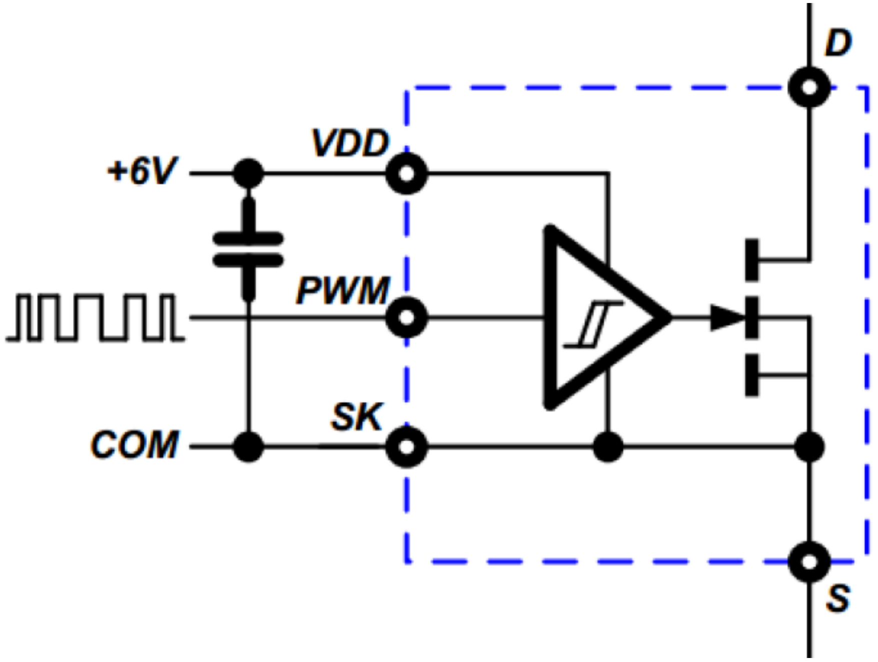
World's First AllGaN™ Power IC

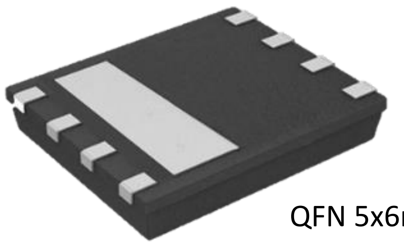


Up to 40MHz switching, 4x higher density & 20% lower system cost

GaN Power IC with Integrated Driver

- **<u>Monolithic</u>** integration
- 20x lower drive loss than silicon
- Driver impedance matched to power device
- Shorter prop delay than silicon (10ns)
- Zero inductance turn-off loop
- High dV/dt immunity (200V/ns)
- Digital input (hysteretic)
- Rail-rail drive output
- Layout insensitive

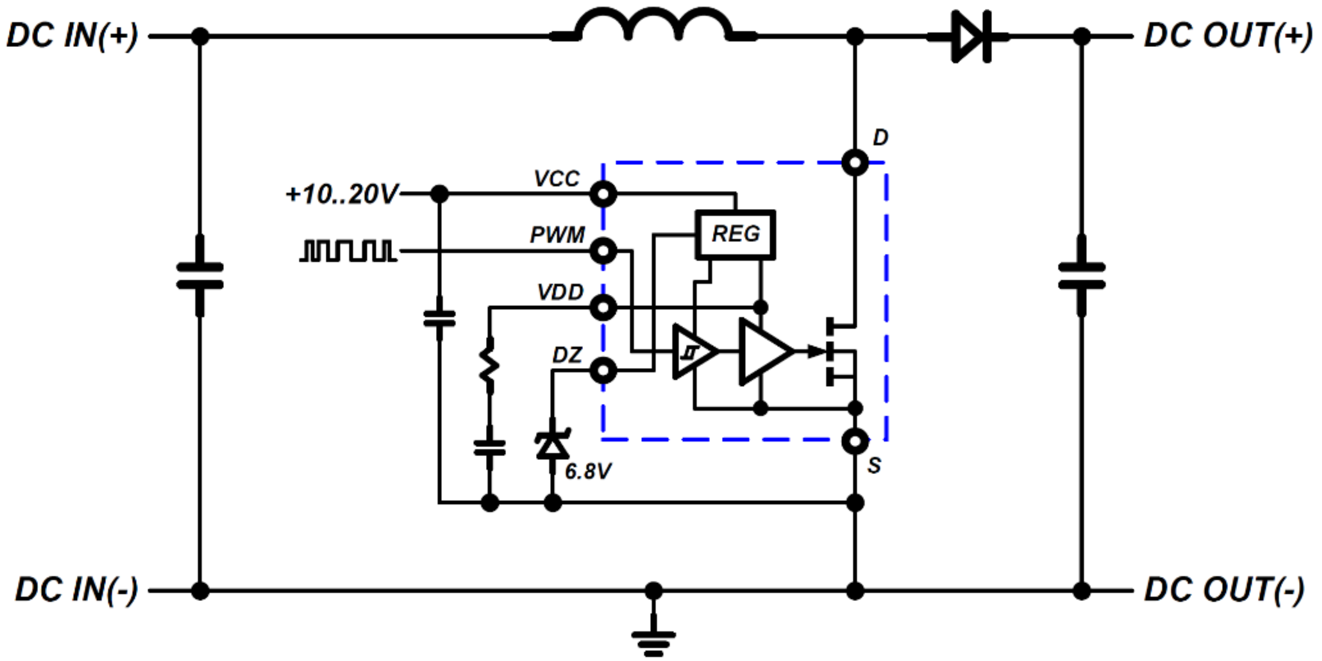


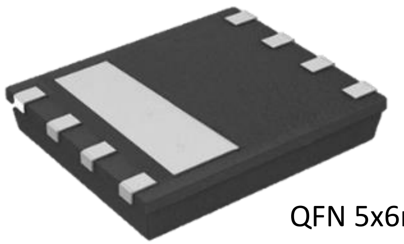


QFN 5x6mm

GaN Power IC – Next Step in Integration

- Extended PWM input range
  - 3.3V, 5V, 15V, 20V input
- Wide V_{CC} range (10V-20V)
- On-board (monolithic) regulator
  - Zener-selectable gate drive voltage
  - Safe start up, power down
  - Internal UVLO
- Resistor programmable turn-on dv/dt
- Standard QFN, simple layout

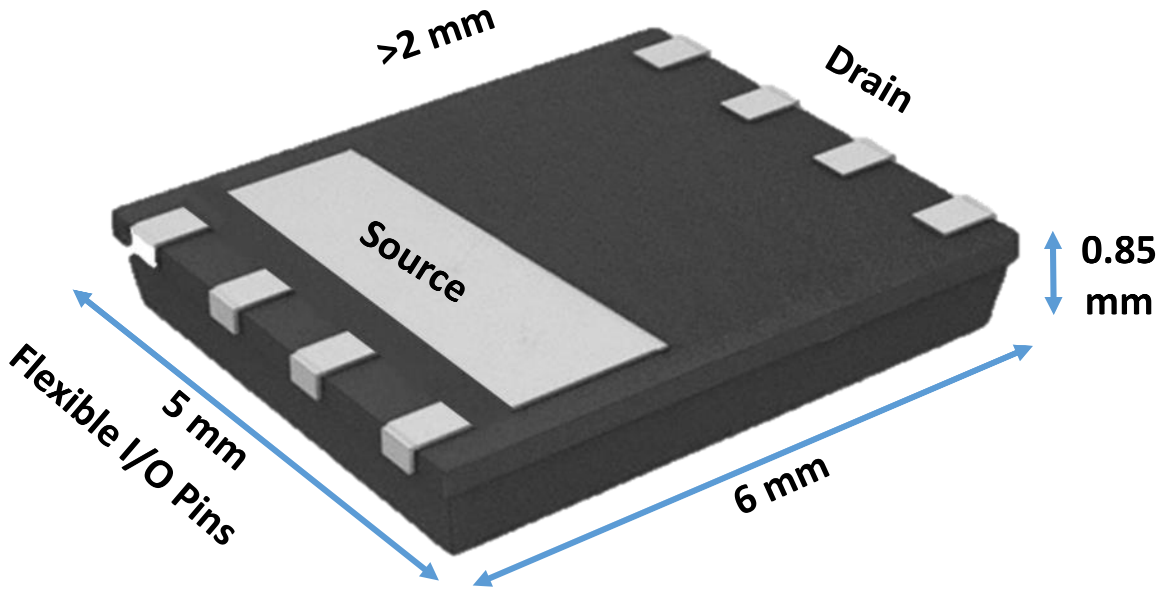




QFN 5x6mm

Fast, Low Cost, Industry-Standard QFN

- Leadframe-based 5X6mm power package outline
- Low profile, small footprint with HV clearance
- Kelvin source connection for gate drive return
- Low inductance power connections (~0.2nH)
- Low thermal resistance (<2^{o}C/W)
- I/O pins enough for drive functions
- High volume
- Reliable
- Low cost



Soft-Switching with GaN Power IC

Primary Switch Power Loss:

Minimized Minimized

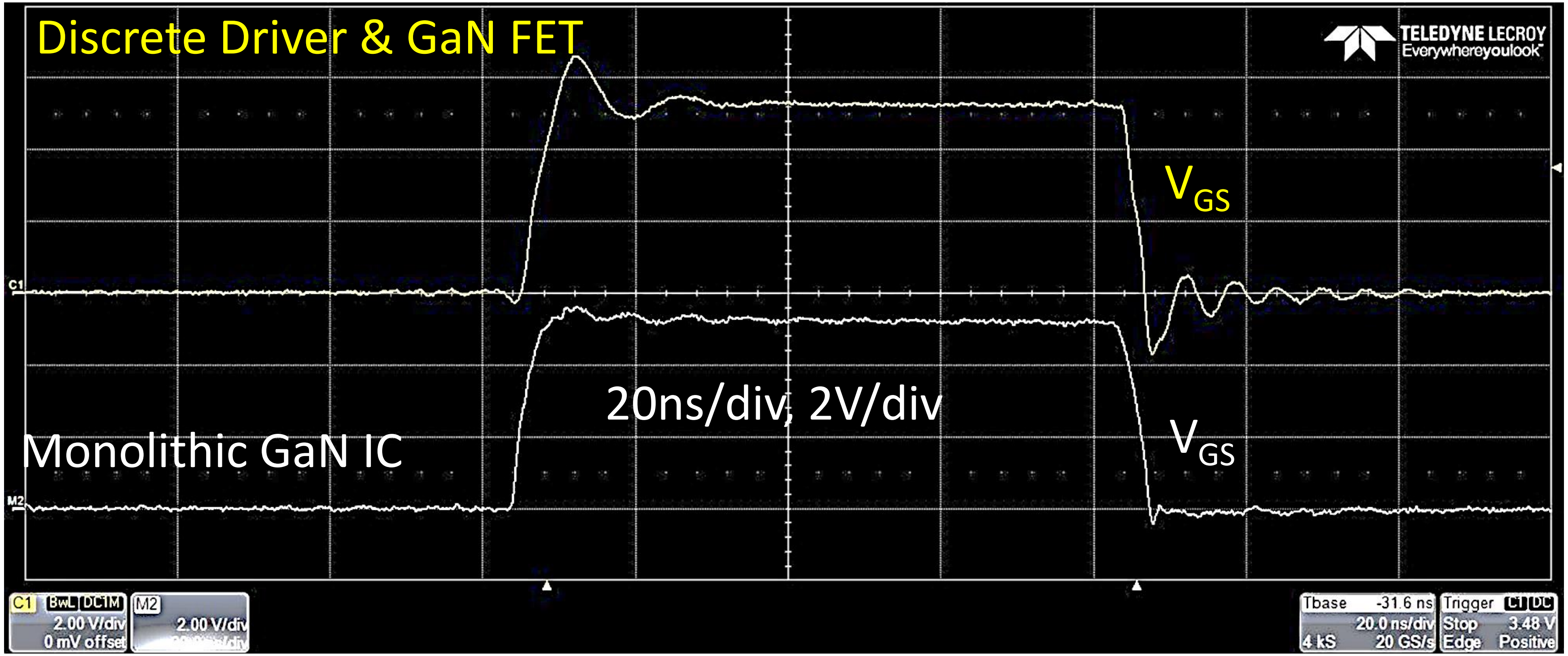
$$P_{FET} = P_{COND} * k + P_{DIODE} + \cancel{P_{T\text{-}ON}} + \cancel{P_{T\text{-}OFF}} + \cancel{P_{DR}} + \cancel{P_{QRR}} + \cancel{P_{QOSS}}$$

- k-factor >1 due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓10X ~~2-3X~~ (GaN C_{OSS} charging/discharging loss negligible up to 2MHz)
- P_{DRIVER} ↓10X (GaN P_{DR} negligible up to 2MHz)
- P_{QRR} = 0
- P_{DIODE} ↓3X ~~2X~~ (synchronous rectification with improved deadtime control)
- $P_{T\text{-}OFF}$ = 0 ~~Reduced~~ (near-zero drive loop impedance with integration)

>10x frequency increase possible with higher efficiencies

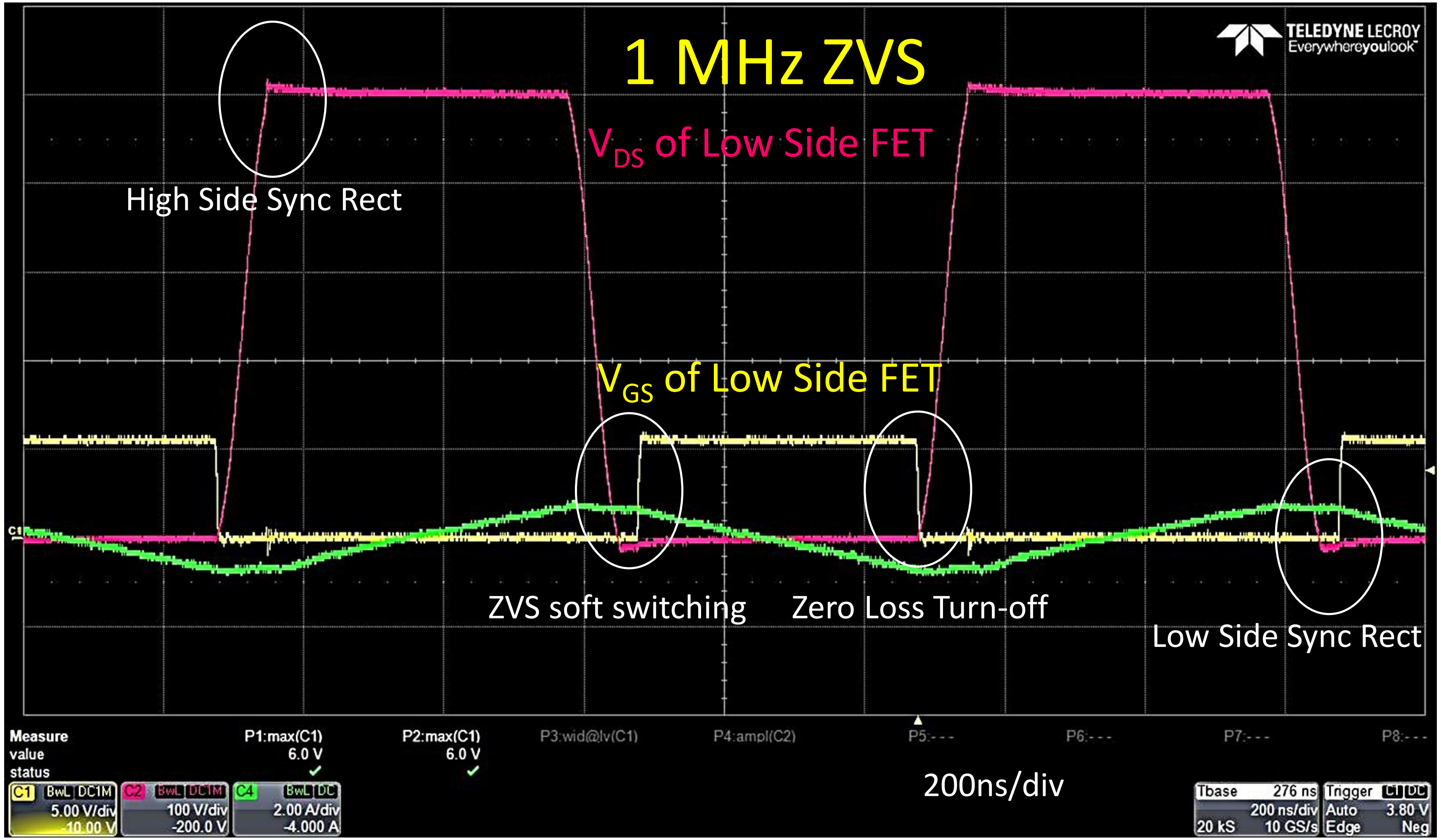
Crisp & Efficient Gate Control

- Eliminates gate overshoot and undershoot
- Zero inductance on chip insures no turn-off loss



GaN Power IC - Zero Loss Switching

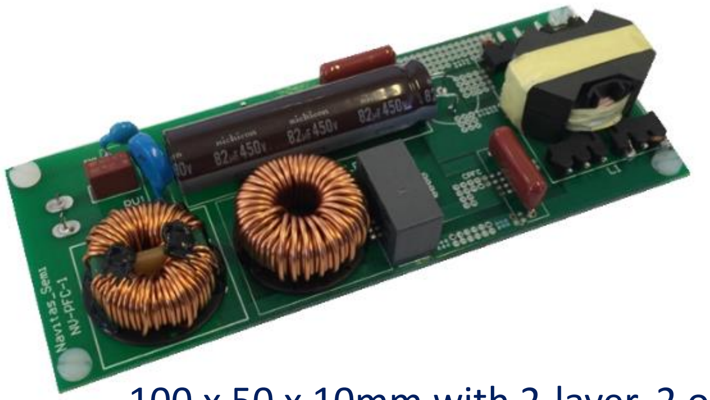
- 500V Switching
- No overshoot / spike
- No oscillations
- ‘S-curve’ transitions
- ZVS Turn-on
- Zero Loss Turn-off
- Sync Rectification
- High frequency
- Small, low cost filter



GaN vs Silicon in 500kHz CrCM PFC

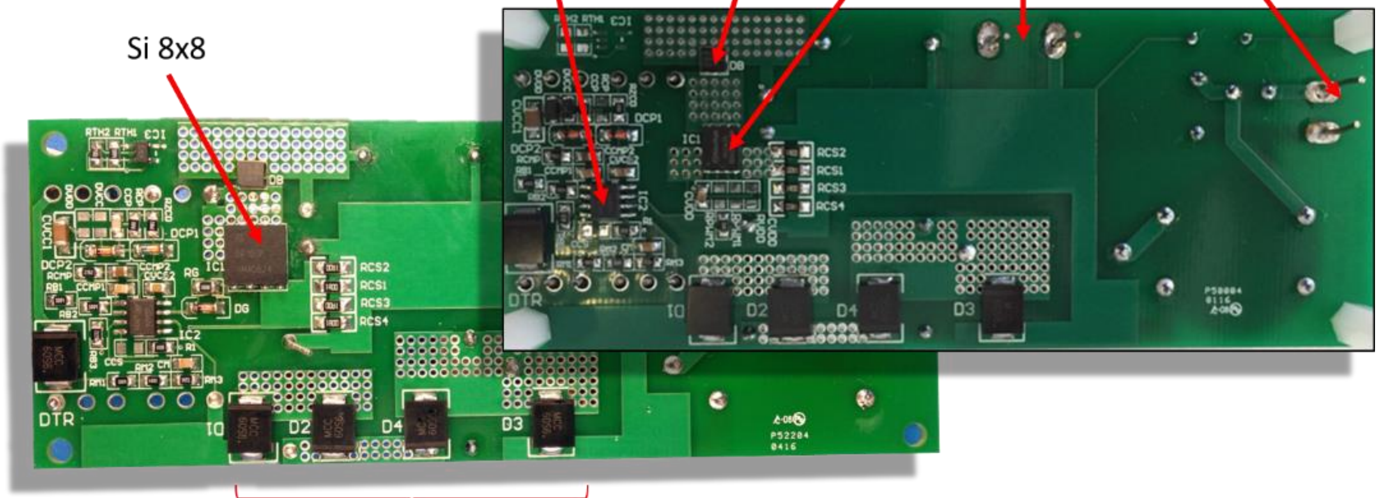
- Critical Conduction Mode (CrCM)
- $120V_{AC}$ = 167-230kHz
- $220V_{AC}$ = 230-500kHz
- 265V peaks at 1MHz *PFC IC (L6562) F_{SW} max*

	Pack	$R_{DS(ON)}$ mΩ	Q_G nC	$C_{OSS}(er)$ pF	$C_{OSS}(tr)$ pF	$R*Q_G$ mΩ.nC	$R*C_{OSS}(tr)$ mΩ.pF	$R*C_{OSS}(er)$ mΩ.pF
Navitas	5x6	160	2.5	30	50	400	8,000	4,800
Si CP Series	8x8	180	32	69	180	5,760	32,400	12,400
Si C7 Series	8x8	115	35	53	579	4,025	66,600	6,100
GaN Benefits	**>50%**	**n/a**	**>10x**	**>2x**	**>10x**	**>10x**	**>7x**	**>2.5x**

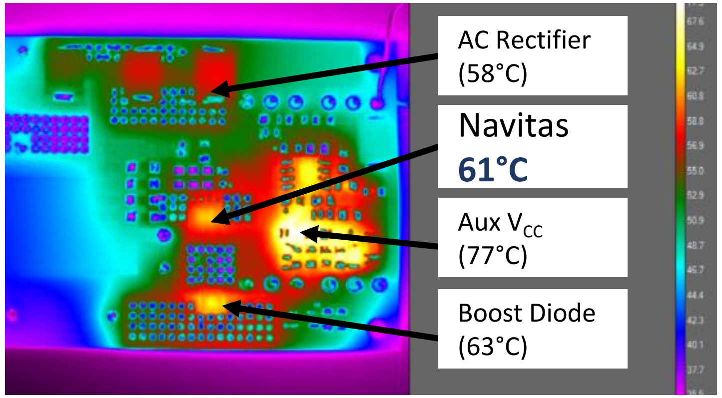


100 x 50 x 10mm with 2-layer, 2 oz Cu

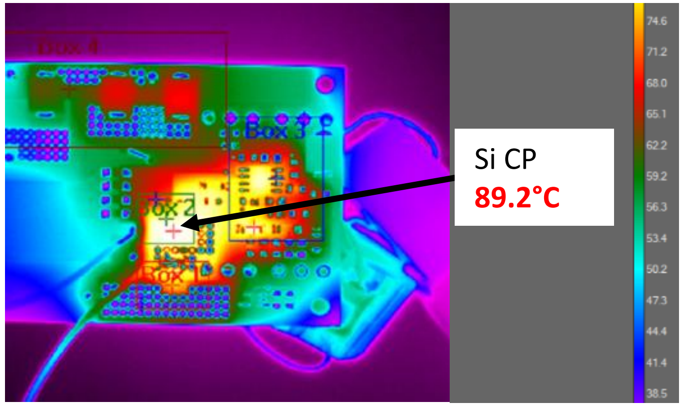
No heatsinks, no forced air,
no glue, potting or heat spreaders



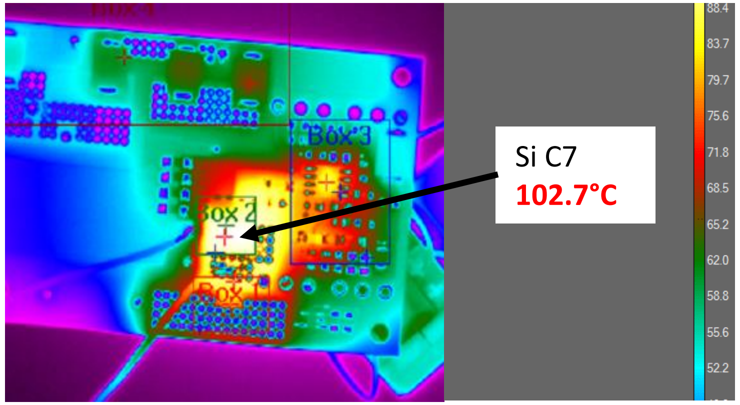
Cool GaN, not Cool Silicon: High Line, Full Load



$220V_{AC}$, 150W



$220V_{AC}$, 150W

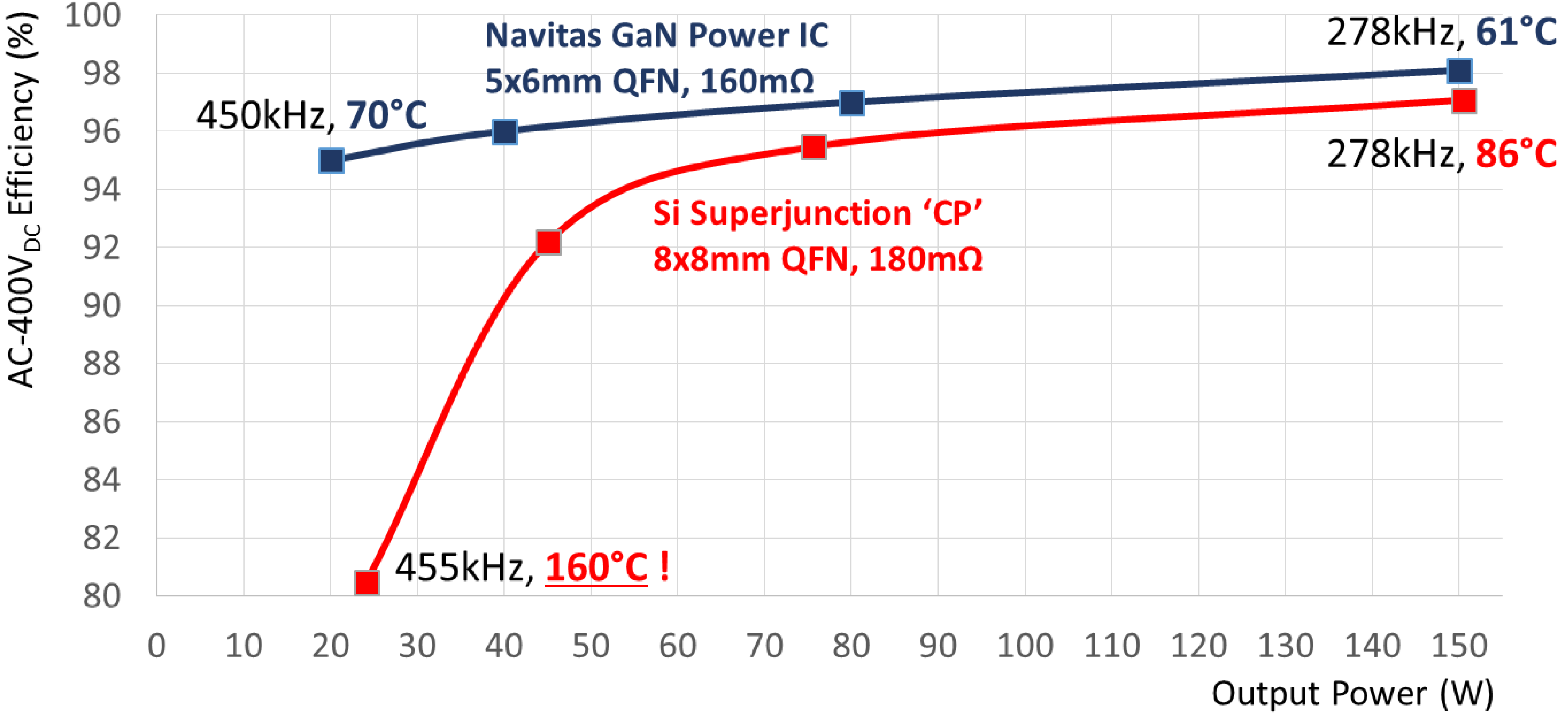


<u>180V</u>$_{AC}$, 150W

- GaN runs cool (61°C)

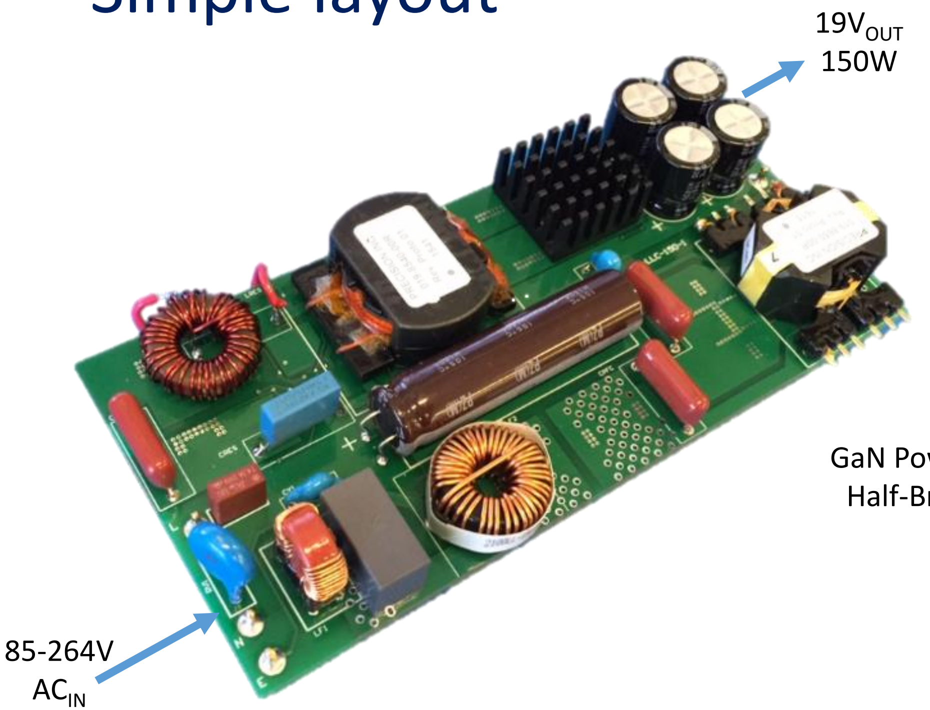
- CP Si running >90°C
- C7 Si too hot to run at $220V_{AC}$

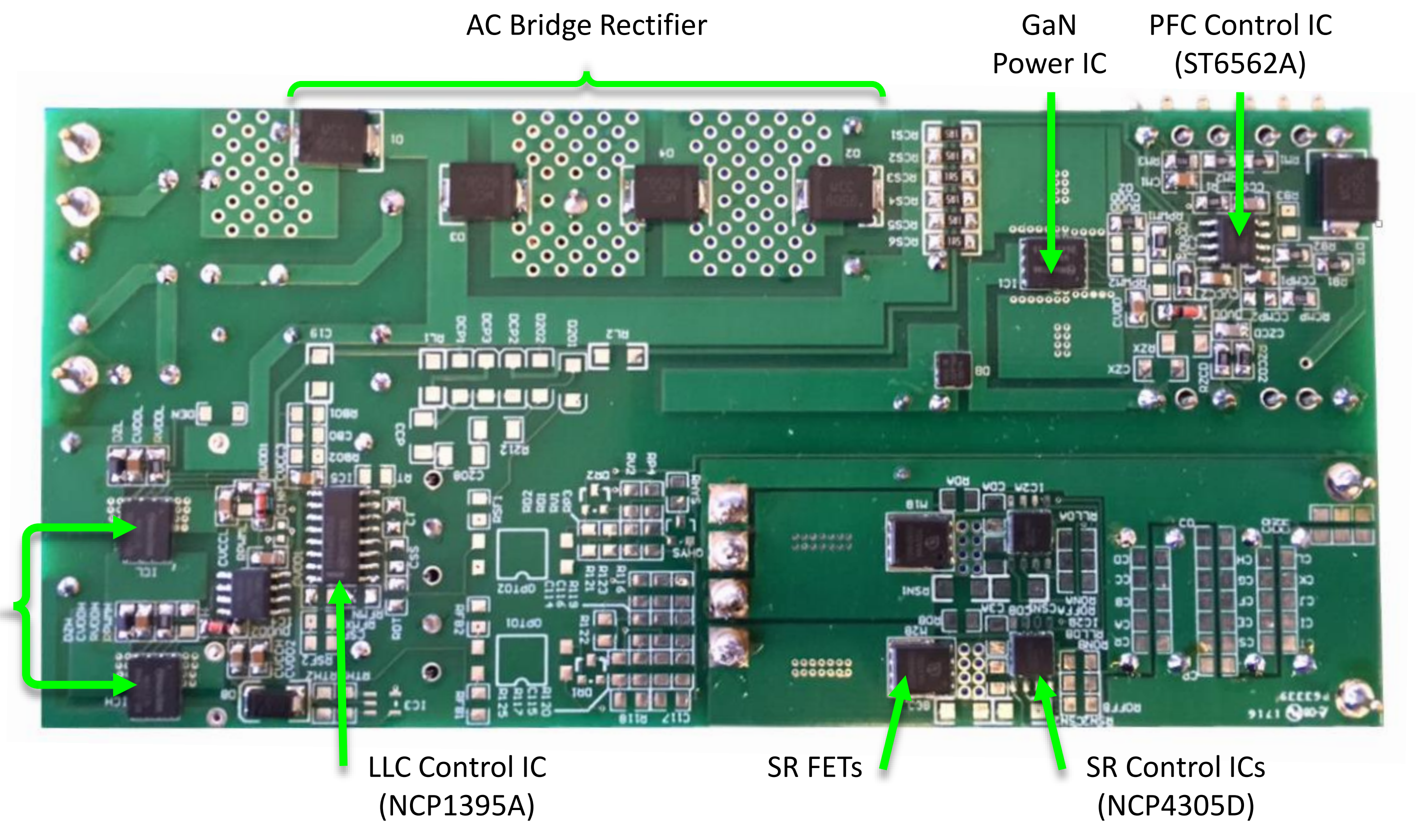
Cool GaN, not Cool Silicon: Driving Frequency



AC-19V: GaN Power ICs in PFC, LLC

- Simple schematic
- Simple layout

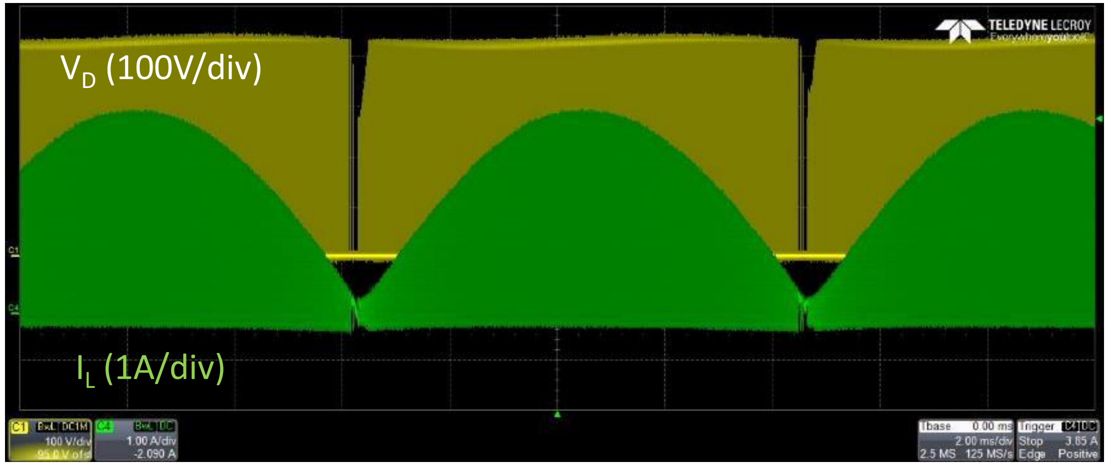




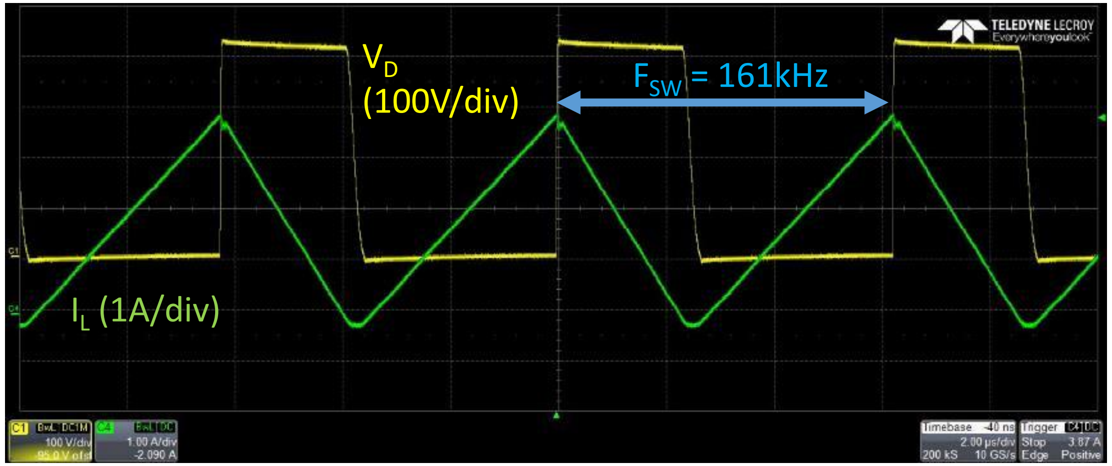
Prototype shown, under optimization

CrCM PFC: High-Frequency, High Performance

$120V_{AC}$, 150W

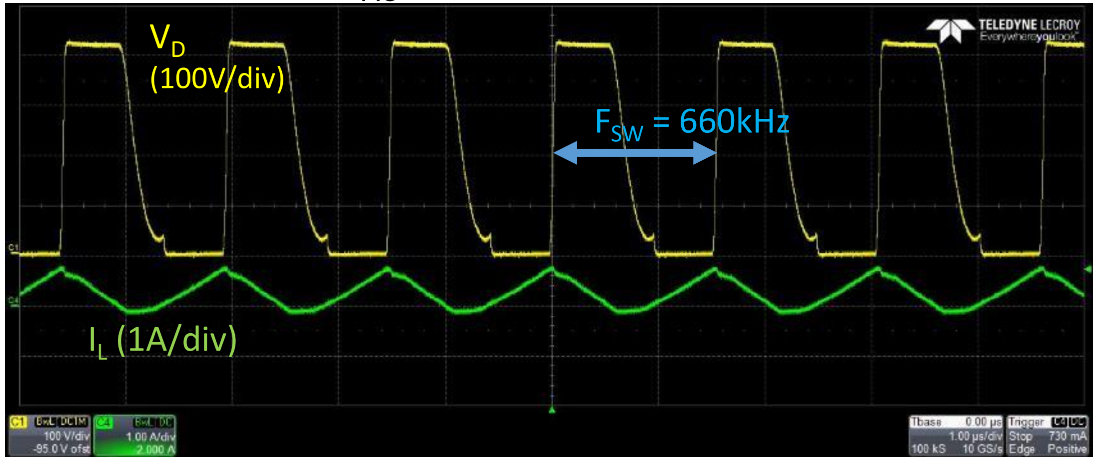


$120V_{AC}$, 150W, @peak AC line)

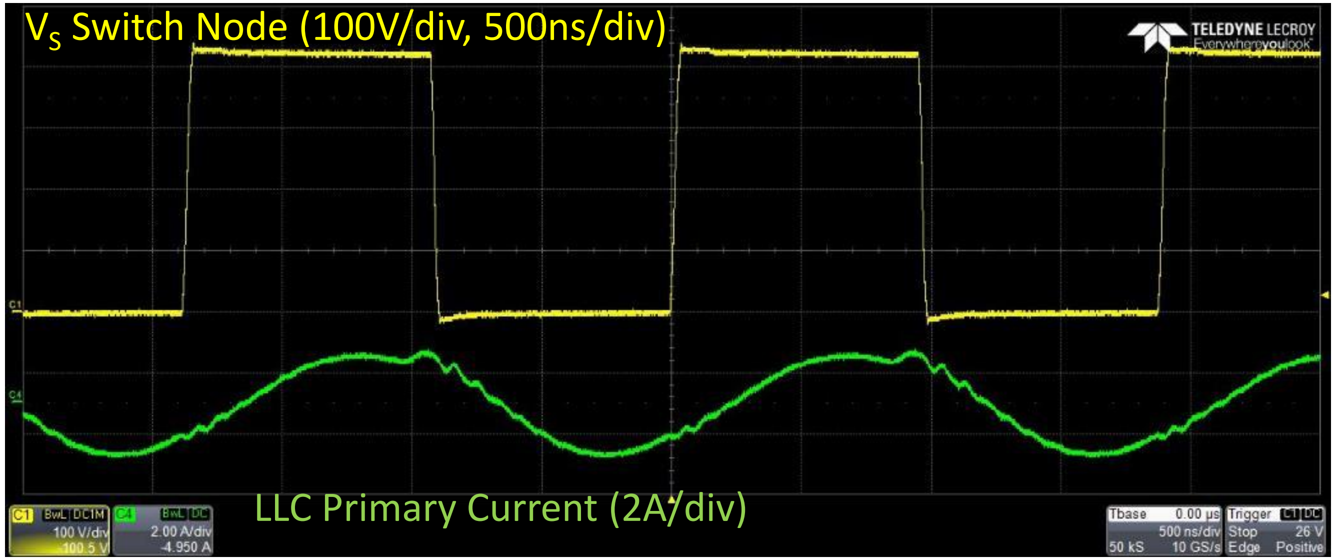


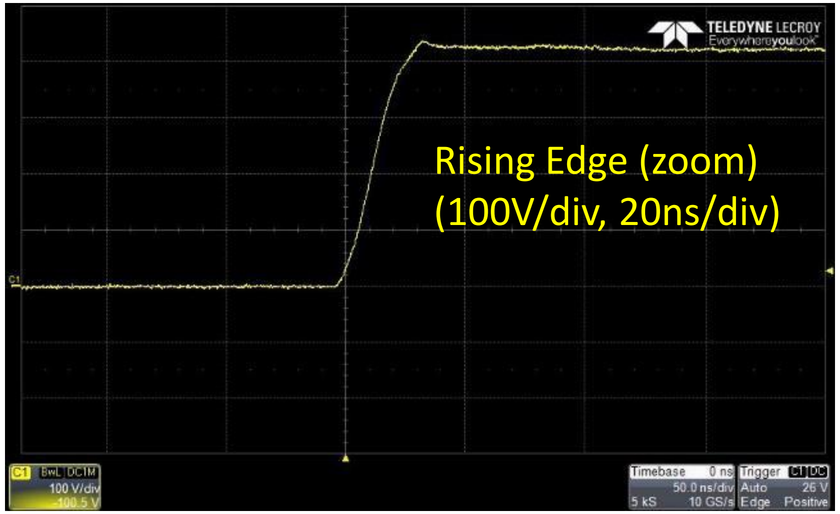
- Excellent Power Factor - PF >99.5%
- High frequency operation
- Easy to achieve ZVS soft-switching
- Negligible switching loss during partial ZVS at high line with GaN

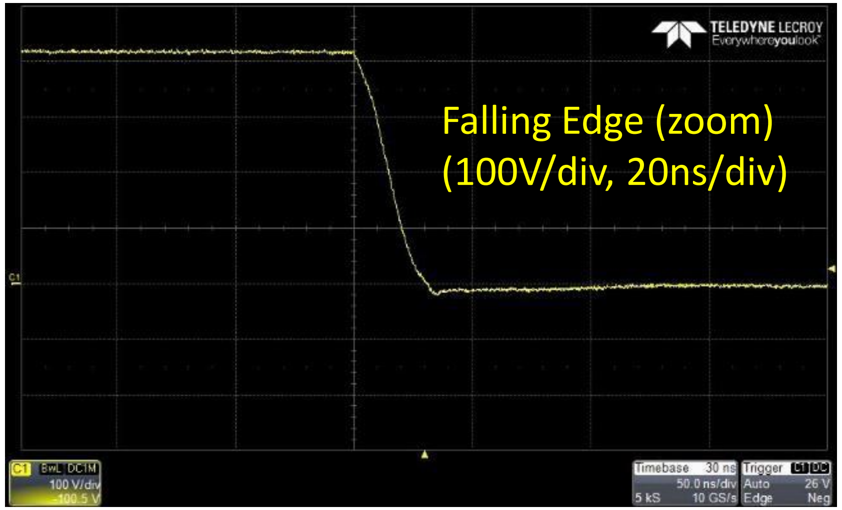
$220V_{AC}$, 85W, @peak AC line)



LLC: Smooth, Fast, Quiet



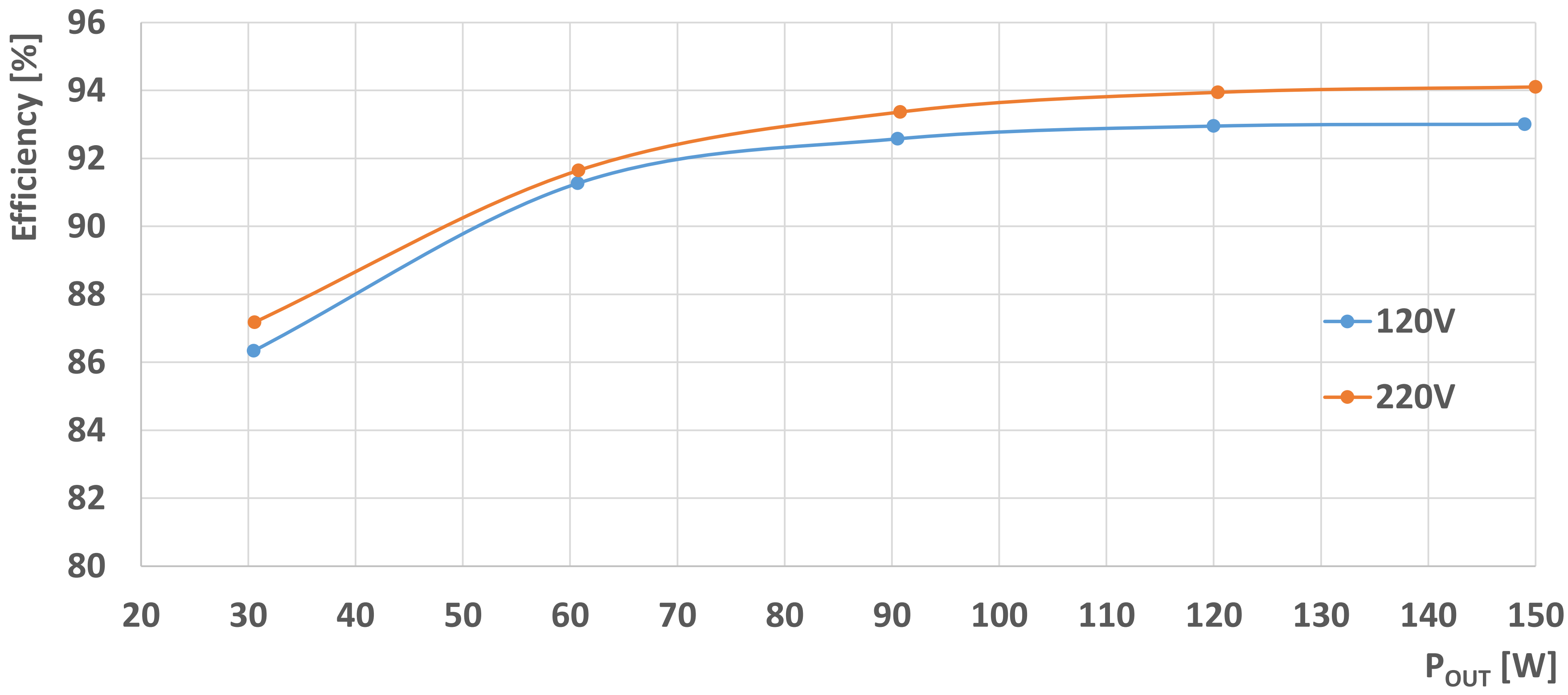




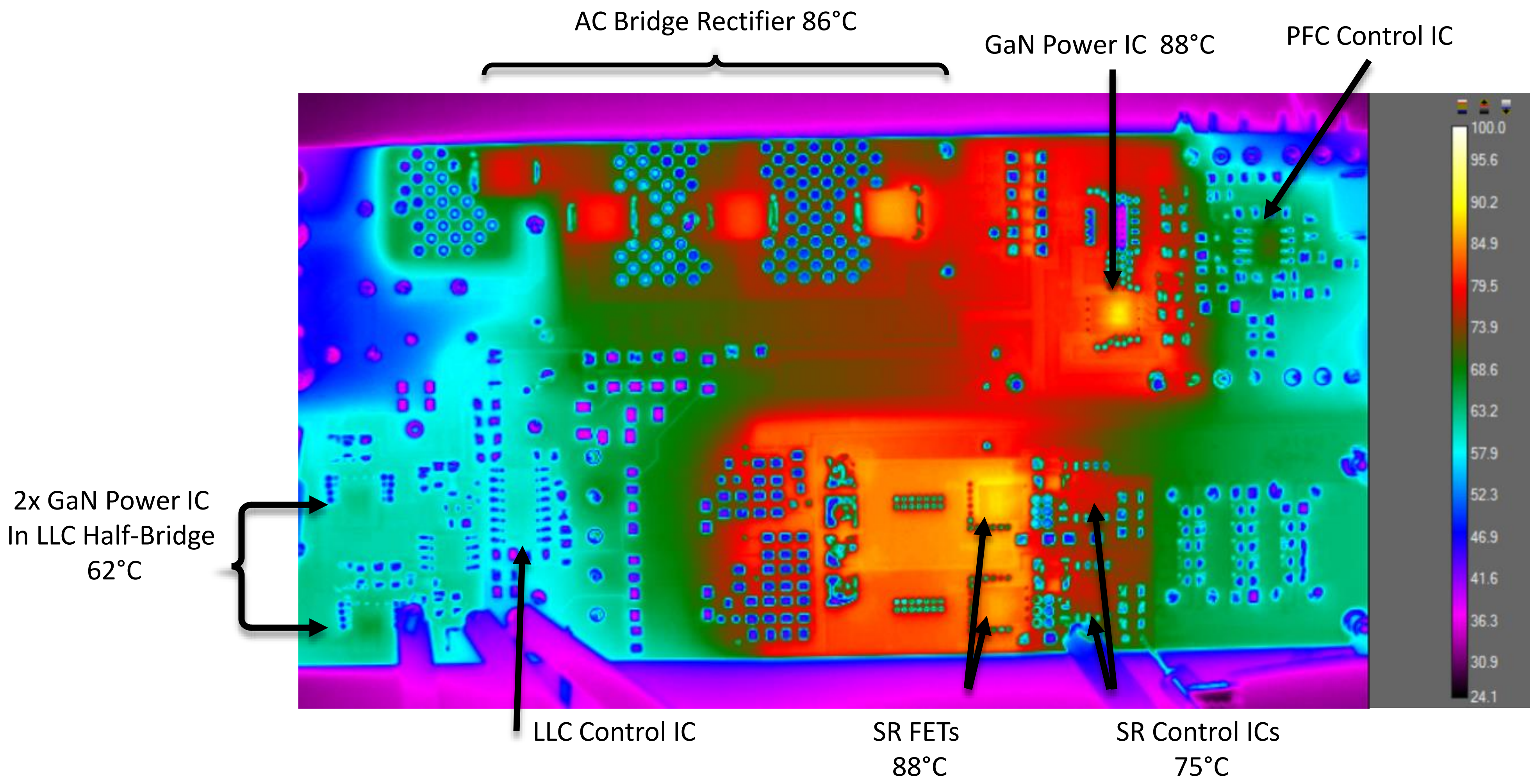
- No spikes, overshoot
- Smooth 'S-curves' with fast ~40V/ns slope
- Low EMI signature

High Efficiency at High Frequency

- AC-19V, 150W, 25°C, no airflow
- $110V_{AC} = 93\%$, $220V_{AC} = 94.1\%$



150W, $90V_{AC}$, 500kHz (no airflow, 25°C)



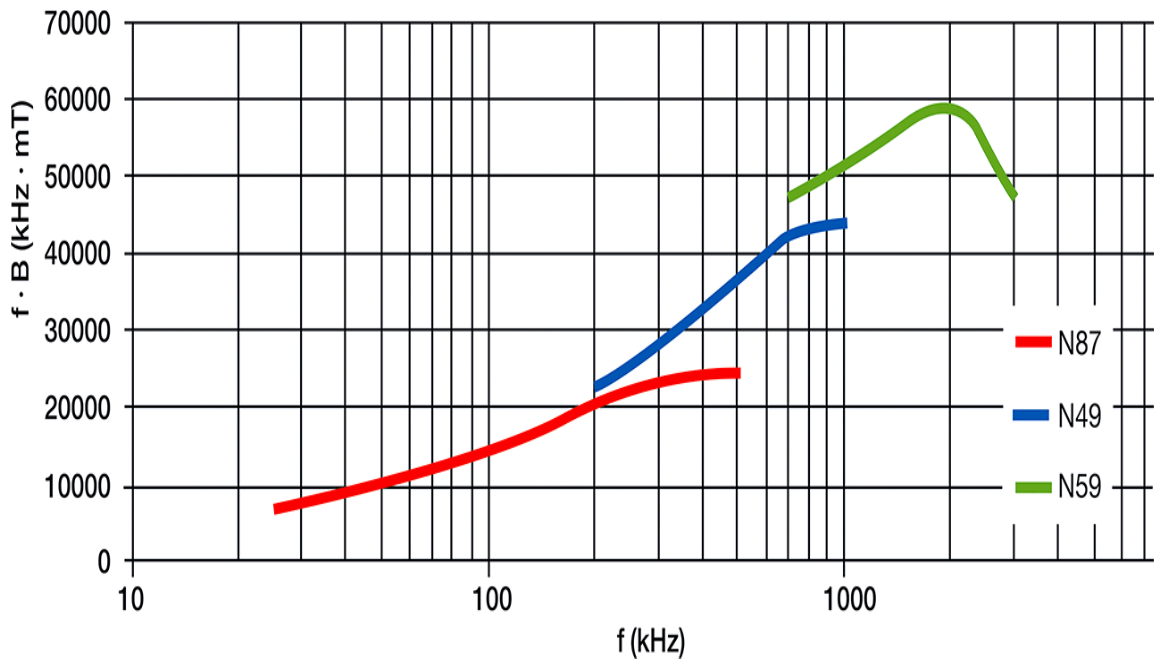
The MHz Eco-System

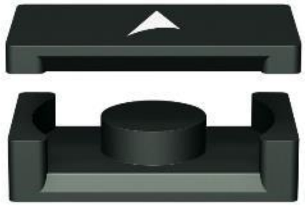
- Navitas GaN Power ICs plus…
  - High-frequency controllers (PFC, PWM, DSP, LLC, SR)
  - High-frequency magnetics
  - High-frequency SR FETs

High Frequency Magnetics ‘GaN Optimized’

Navitas

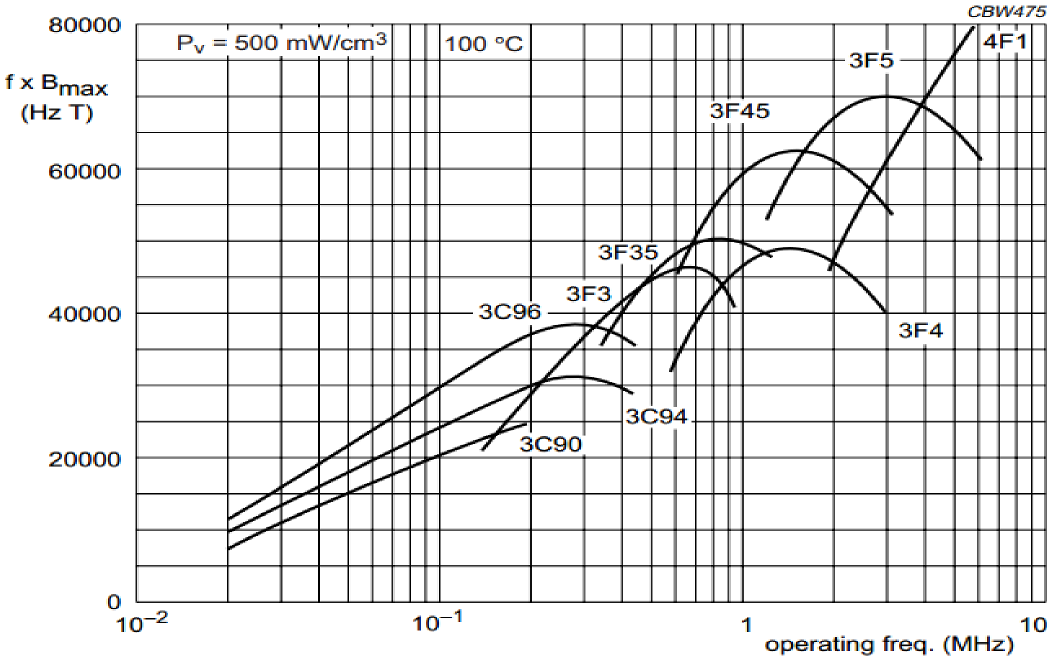
N59 optimized for 2MHz

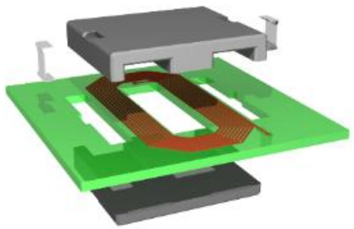




TDK

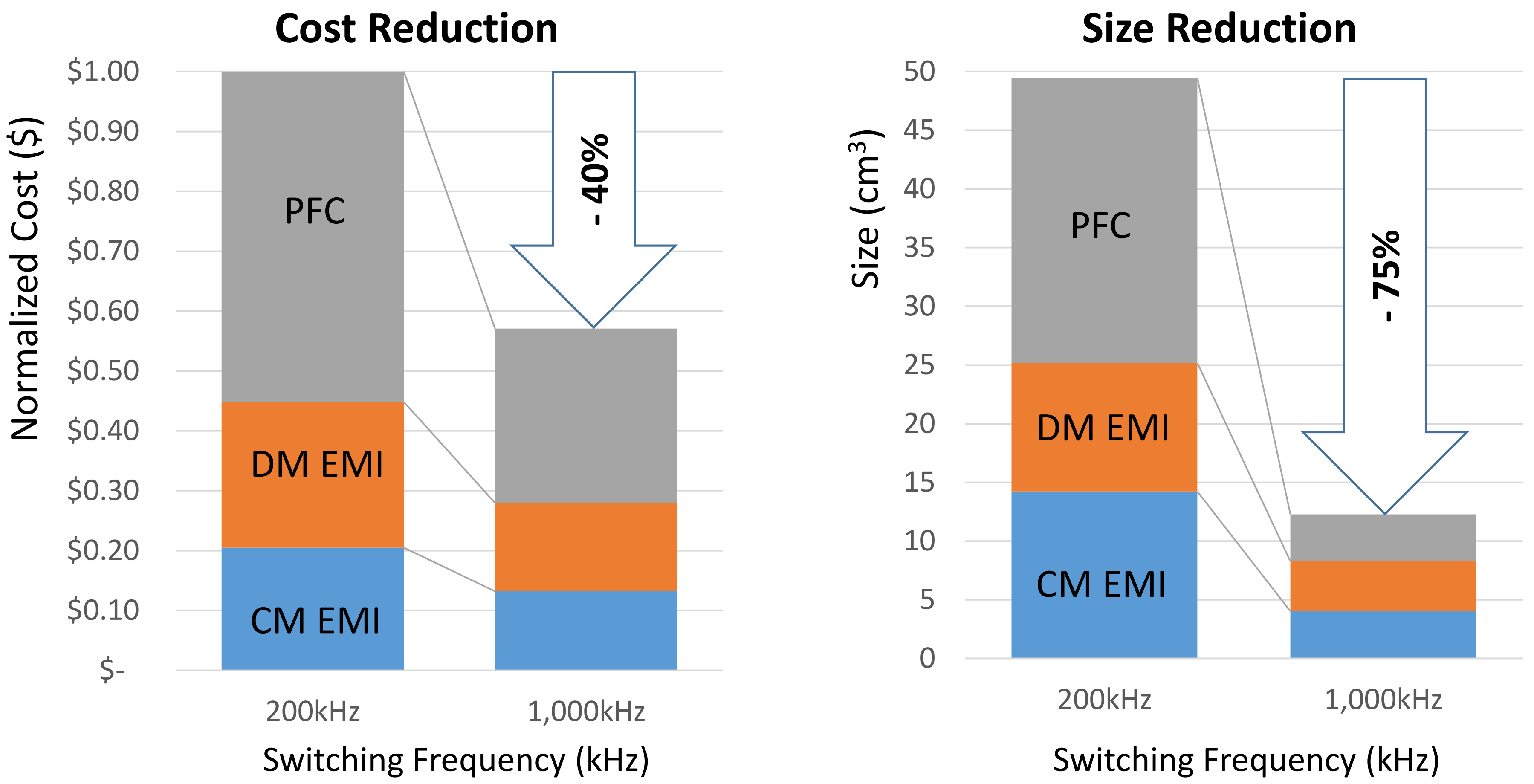
3F & 4F up to 10MHz





PRECISION INCORPORATED

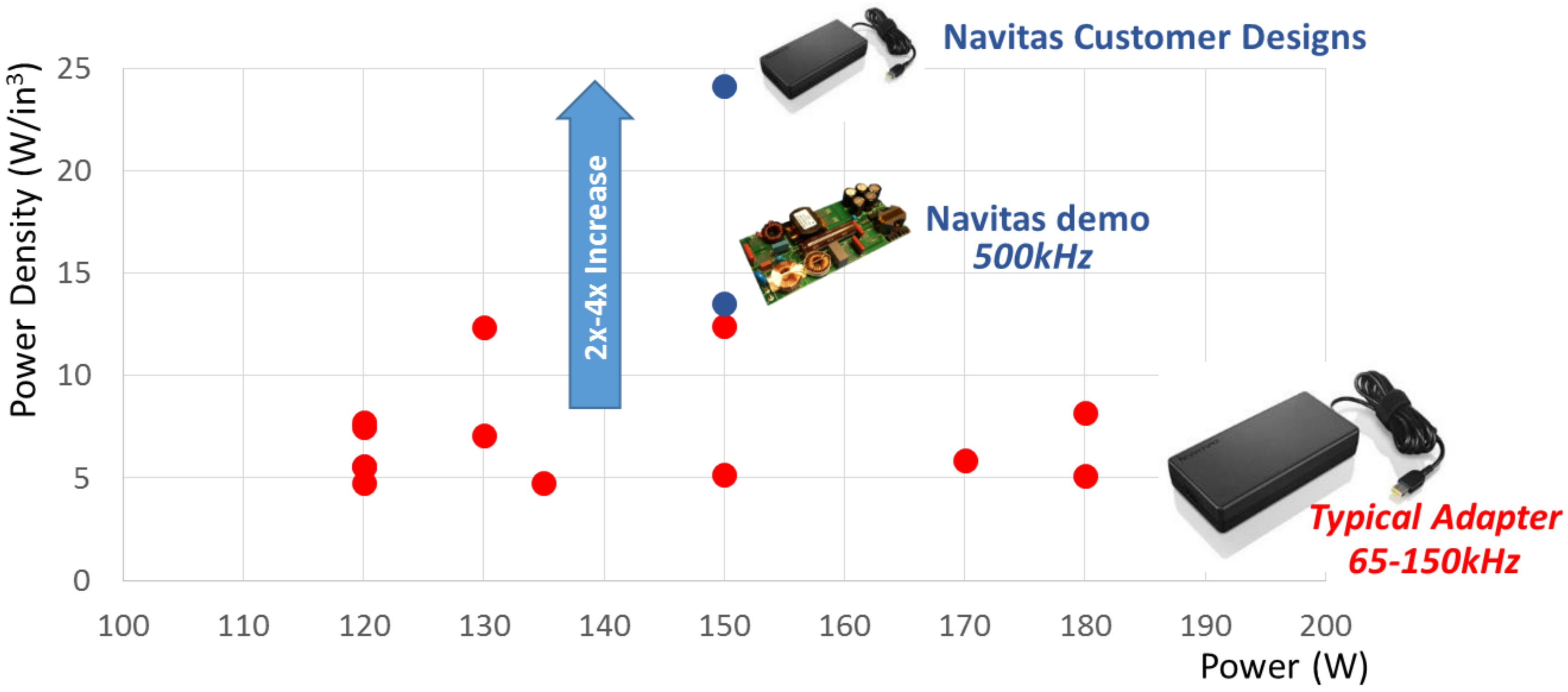
Higher Frequency = Smaller, Cheaper



Magnetics & EMI Filters

Frequency drives 2x-4x Power Density

- Typical adapters (65-150kHz) = 5-12W/in³
- Navitas demo (500kHz) = 13.5W/in³
- Navitas customer estimate = 20-25W/in³

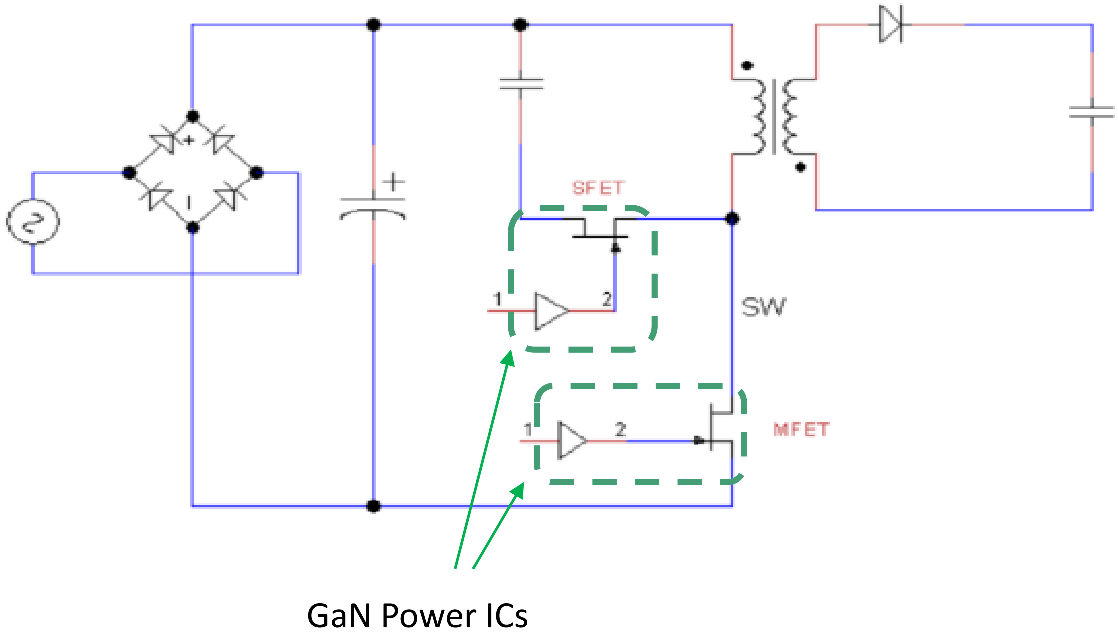


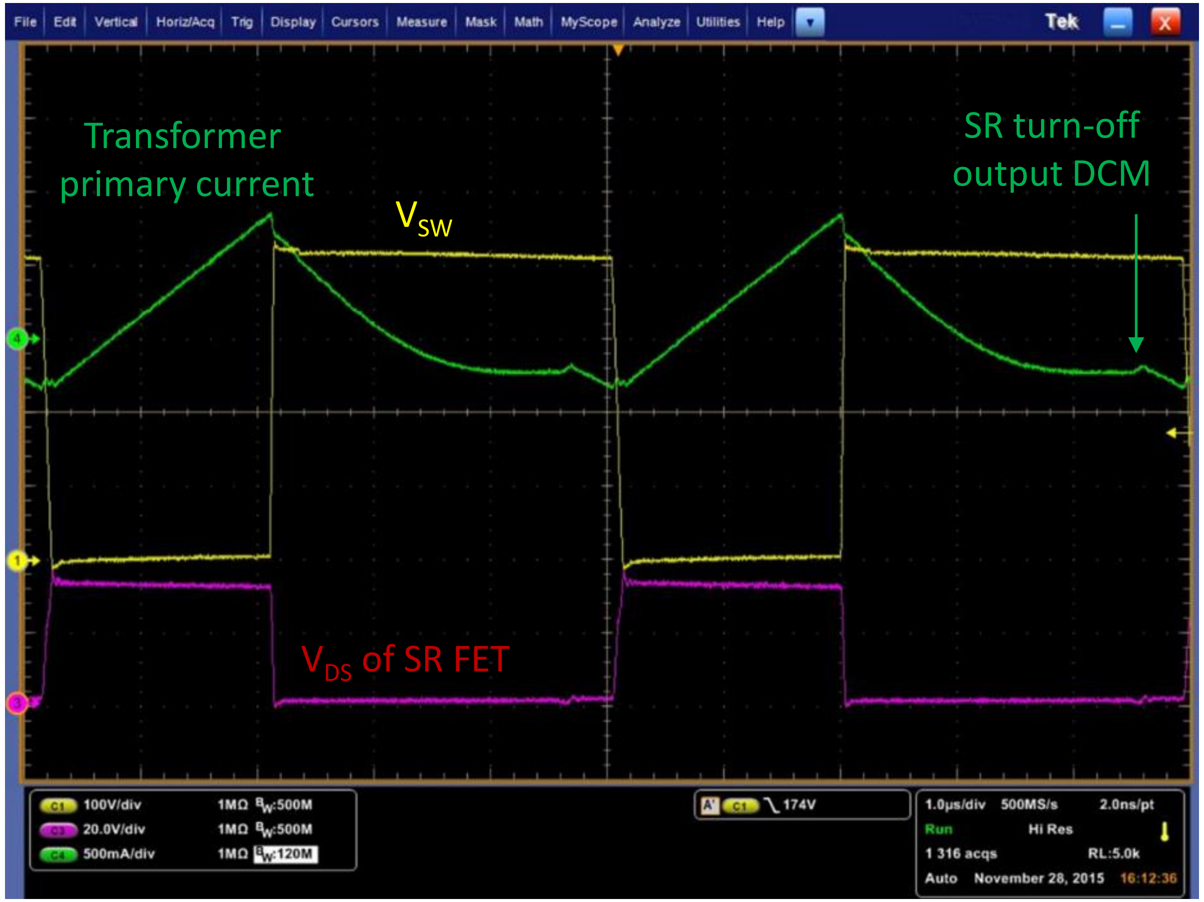
Gamer Laptops (100-150W)

All-in-One PCs (150-200W)

38”-52” TVs (100-200W)

Soft-Switching: Active Clamp Flyback (ACF)

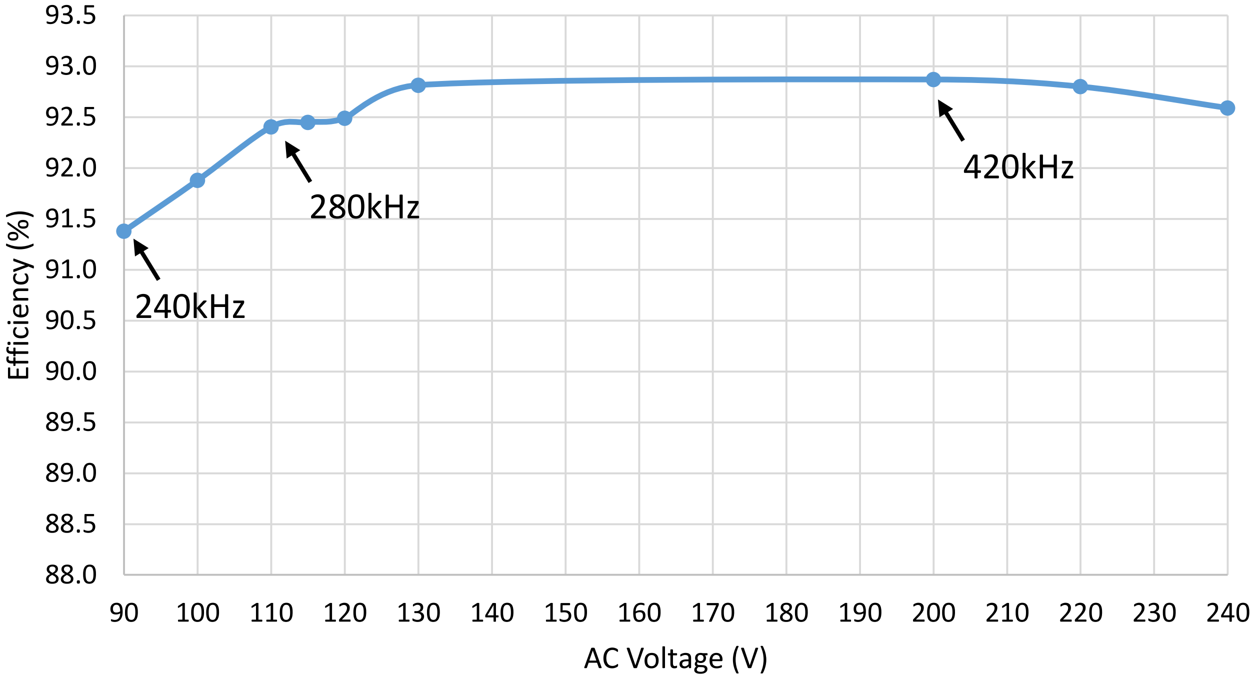


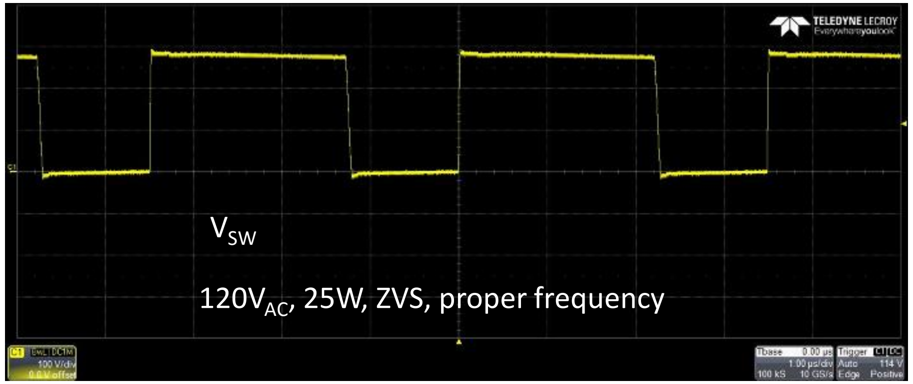


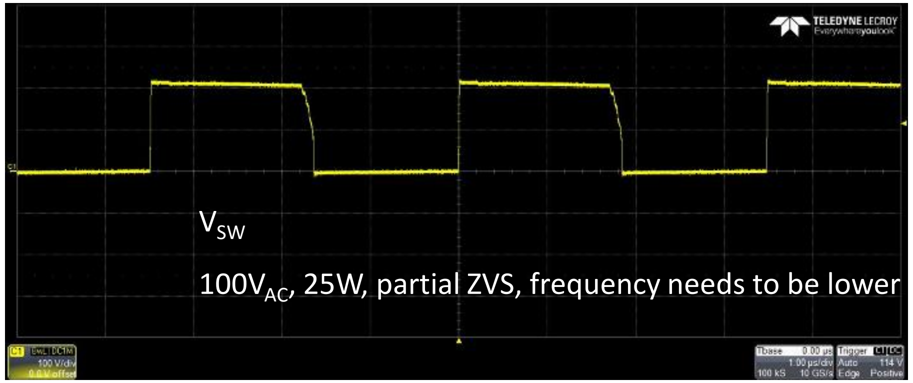
- ACF* gives highest efficiency, highest power density for adapters 20W-75W
- No snubber loss
- Reduced voltage across primary FETs

* "Utilization of an Active-Clamp Circuit to Achieve Soft-Switching in Flyback Converters", Watson, et al, VPT, IEEE Transactions on Power Electronics Vol. 11, No.1, January 1996

Navitas 25W ACF: Frequency, Efficiency





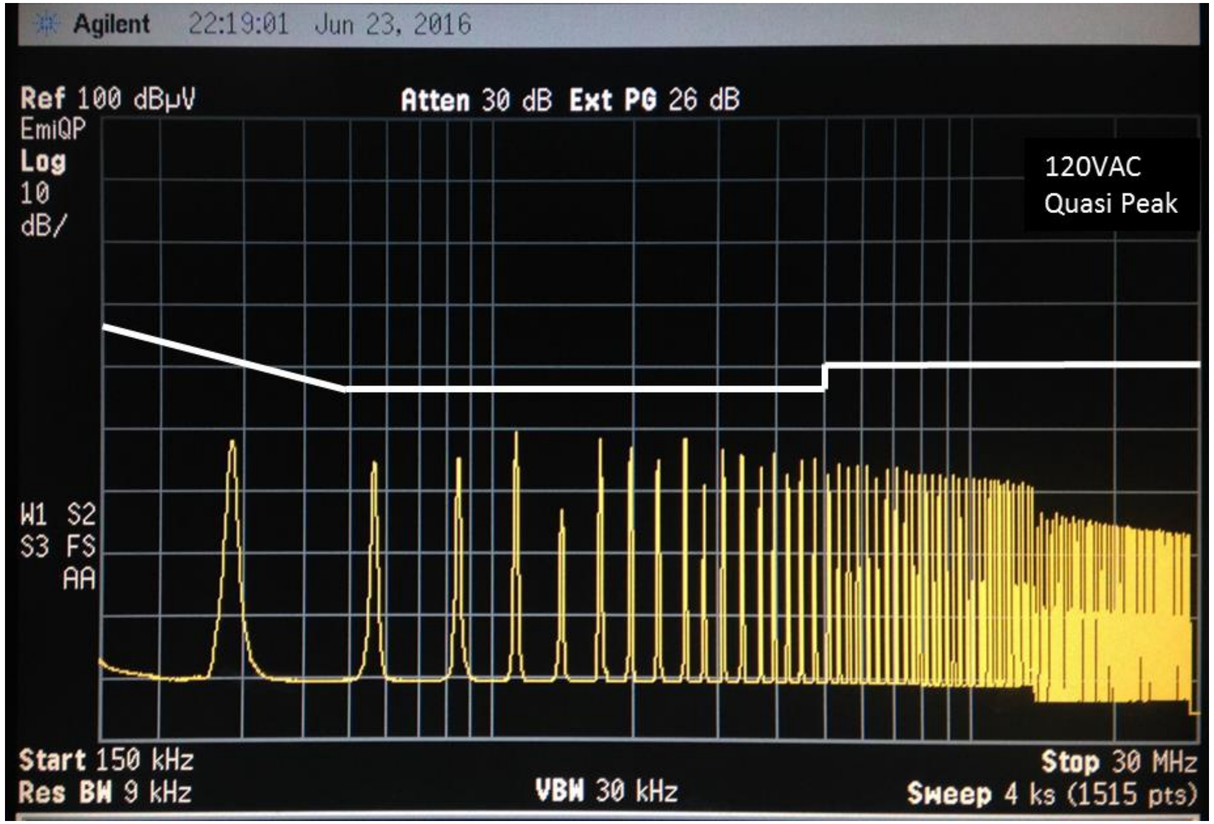


- Existing ACF control IC
    - Uses variable frequency control to maintain critical DCM
    - Too high frequency loses soft switching
    - Too low frequency generates excessive negative current
    - Limited frequency
- New, higher frequency ACF controllers – expect +0.5%

Efficiency measured at PCB

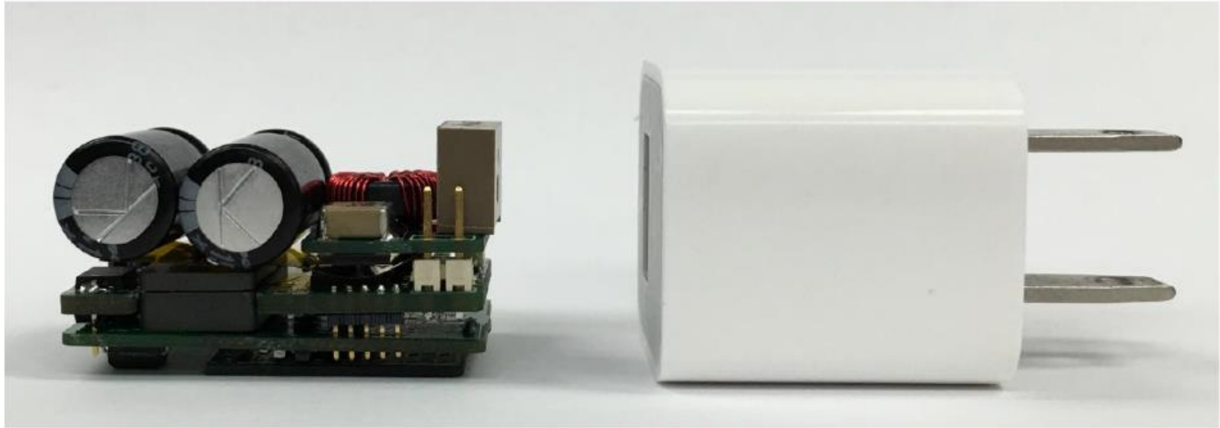
Quiet EMI

- Conducted EMI (CISPR Class B)*
- Quasi-peak, 120V_{AC}, 285kHz
- Quiet performance
  - Controlled switching
  - No spikes, no overshoot
  - 'S'-curve transitions
- Simple EMI filter design**



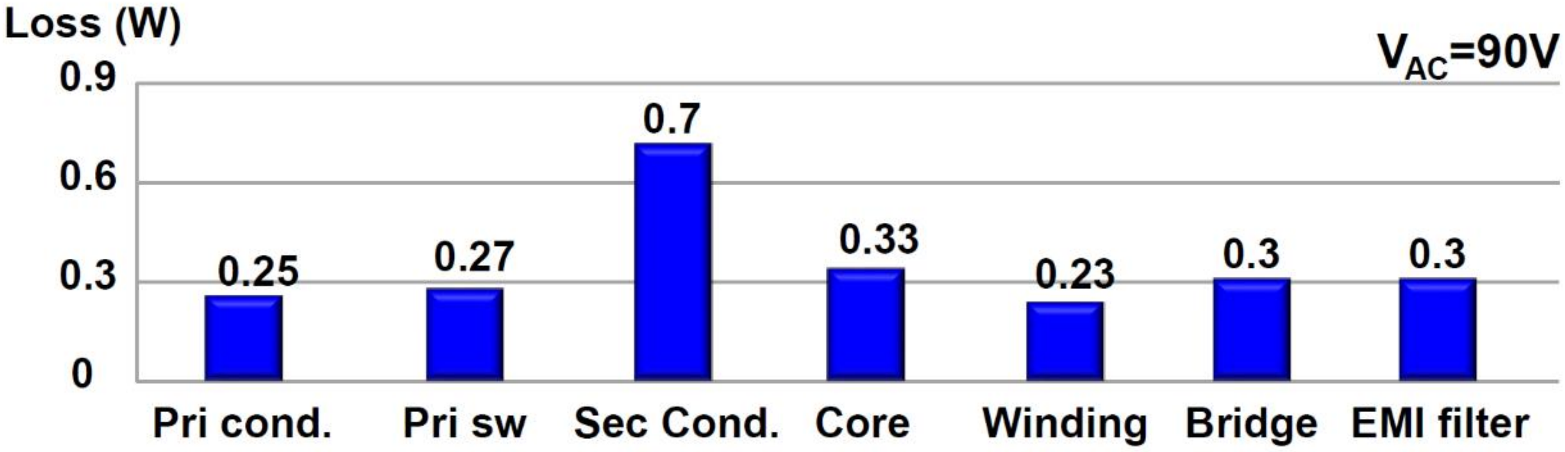
***Refer also to:* "Design Considerations of MHz Active Clamp Flyback Converter with GaN Devices for Low Power Adapter Application", Huang, et al, VPT, APEC 2016
"Conducted EMI Analysis and Filter Design for MHz Active Clamp Flyback Front-End Converter", Huang, et al, VPT, APEC 2016
* *In-house EMI equipment*

ACF at 1MHz, 25W



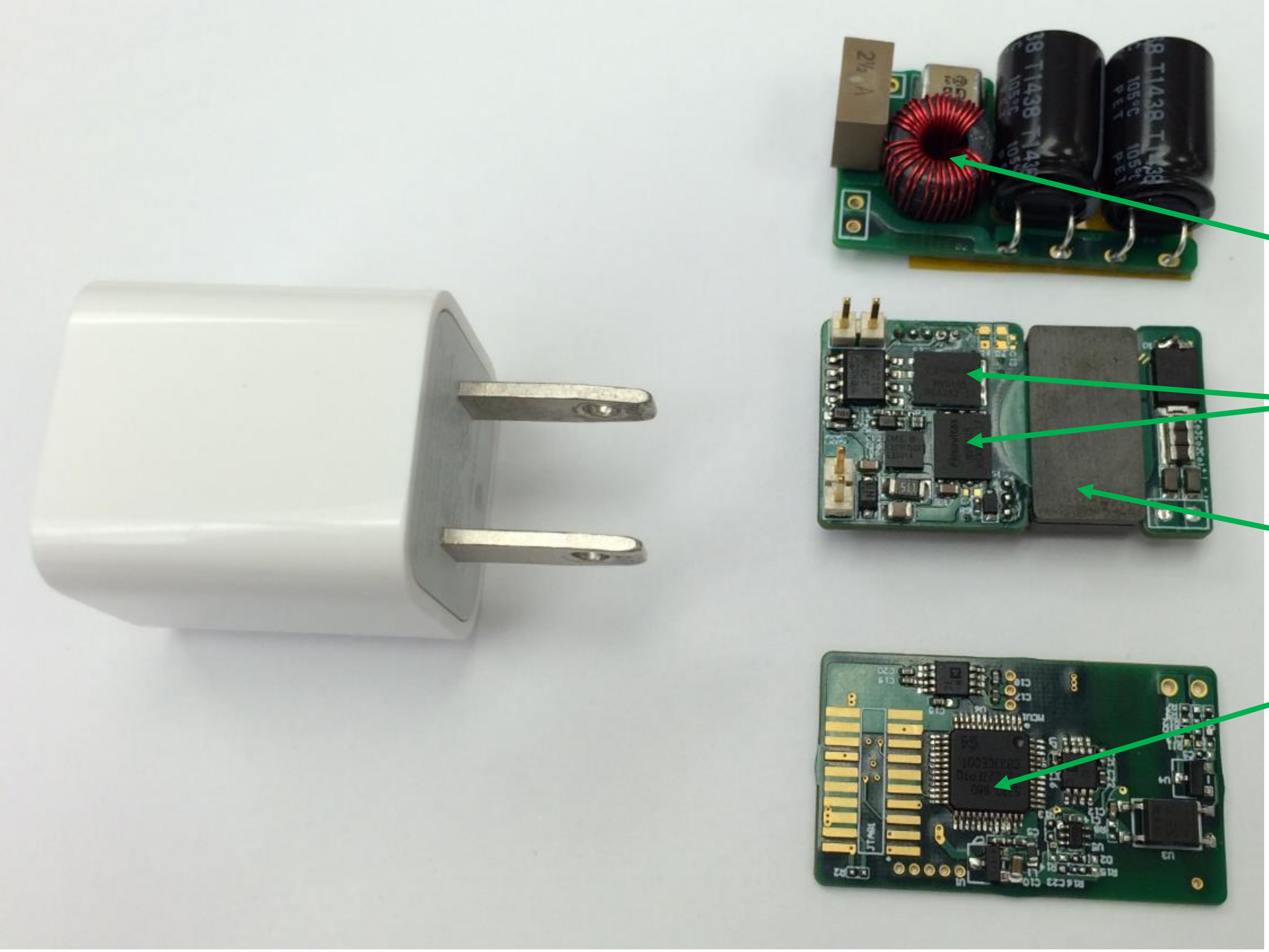
CPES Prototype
25W

iPhone charger
5W



Eff ≈ 91.3% @ P_O=25W

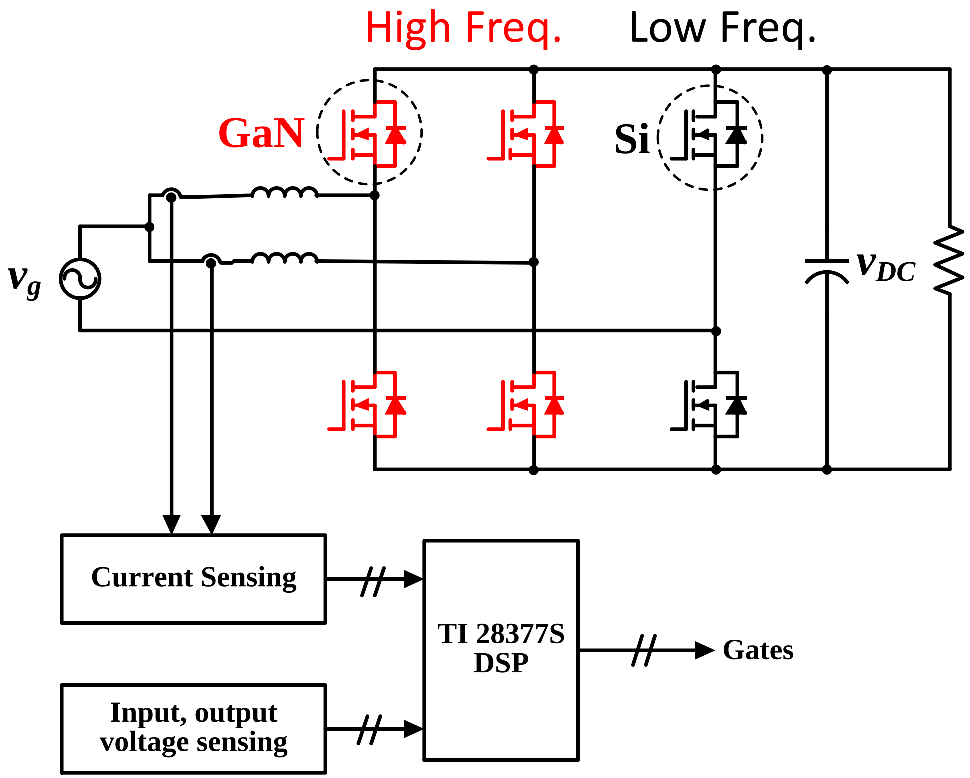
1MHz, 25W ACF



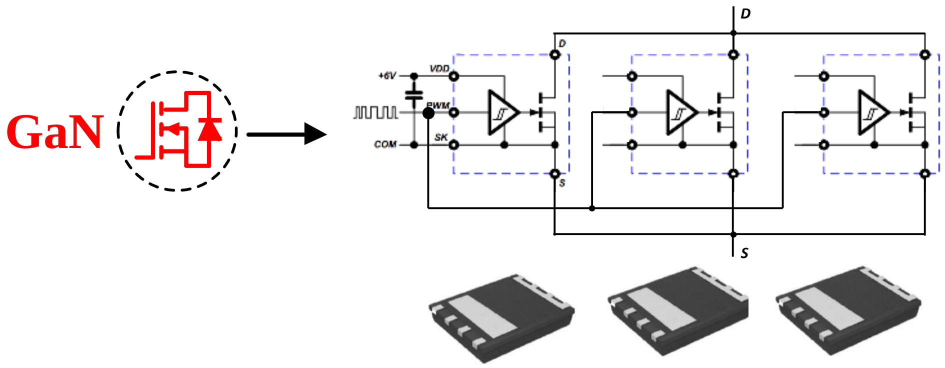
- Single-stage EMI
- Navitas GaN Power ICs
- Planar transformer
- DSP (for prototype)

1MHz 3kW PFC: 99%

- 2-phase Totem-Pole CrCM
- Input : $220V_{AC}$ (47-63Hz)
- Output : 400V, 3,000W



- Frequency* : 1MHz each phase
  - *Dual phase variable frequency interleaving (500kHz – 1.5MHz range)
- Efficiency : >99% @ 800kHz, 200-1,200W/phase (1)
  >98.8% @ 500kHz, 1,800W /phase (1)
- Power Factor : >0.995 (1)



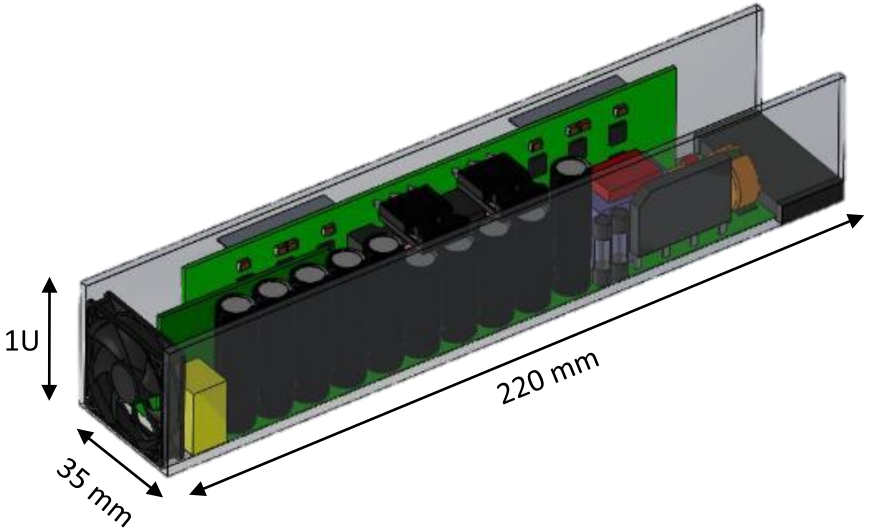
3x 160mΩ GaN Power ICs, in 5x6 mm QFN

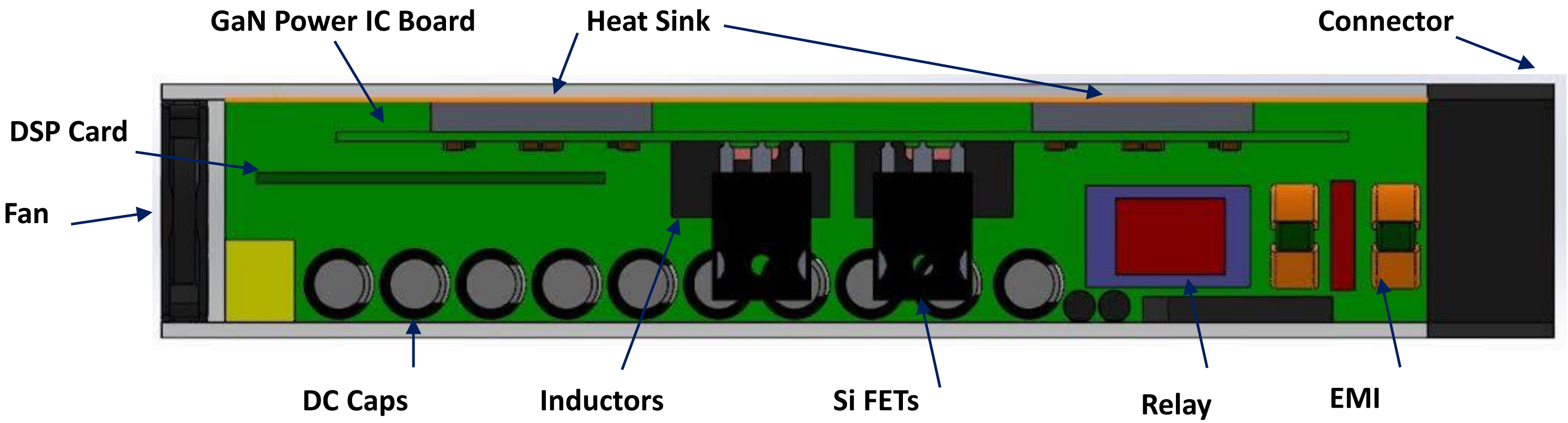
(1) Achieved on Alpha prototype

1MHz 3kW PFC: 135W/in^3

- 2-phase Totem-Pole CrCM
- Input : 220V_{AC} (47-63Hz)
- Output : 400V, 3,000W

- Frequency* : 1MHz each phase
  - *Dual phase variable frequency interleaving (500kHz – 1.5MHz range)
- Efficiency : >99% @ 800kHz, 200-1,200W/phase (1)
  >98.8% @ 500kHz, 1,800W /phase (1)
- Power Factor : >0.995 (1)
- Power Density : 135W/in^3



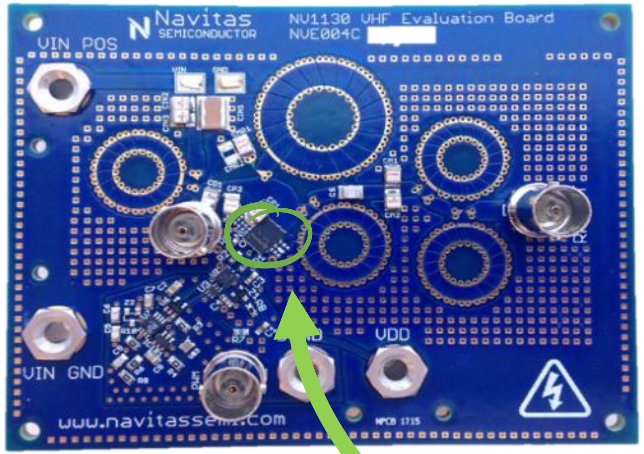


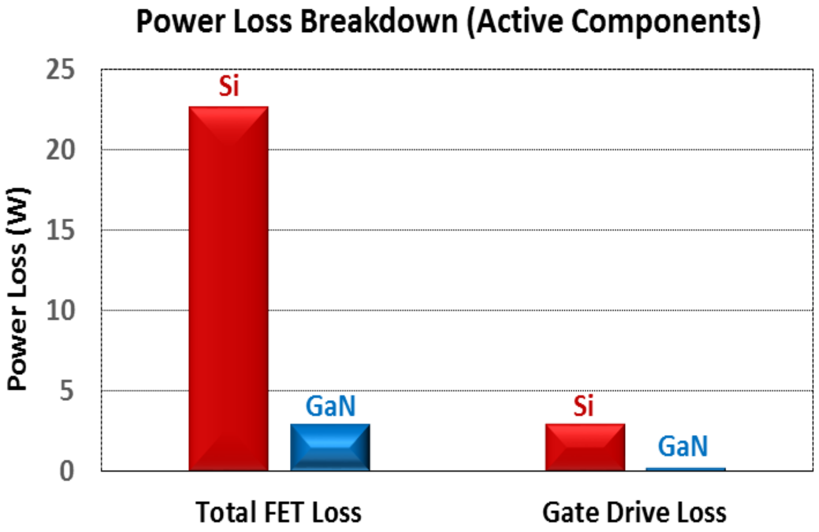
(1) Achieved on Alpha prototype, (2) Target for Beta prototype

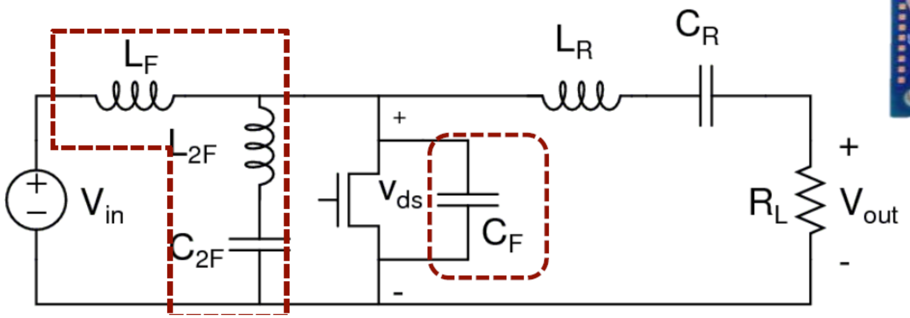
eMode GaN at 27MHz & 40MHz

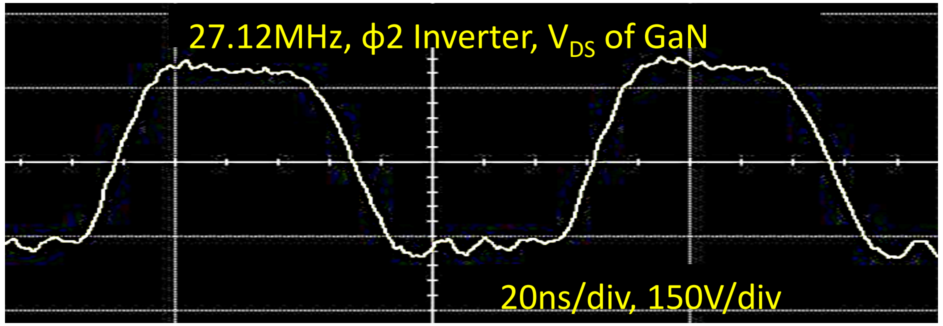
Class Phi-2 DC/AC converter: Stanford / Navitas demo

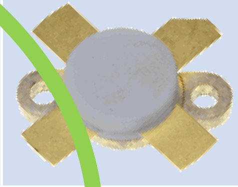
- 50% less loss than RF Si
- 16x smaller package
- Air-core inductors
- Minimal FET loss
- Negligible gate drive loss





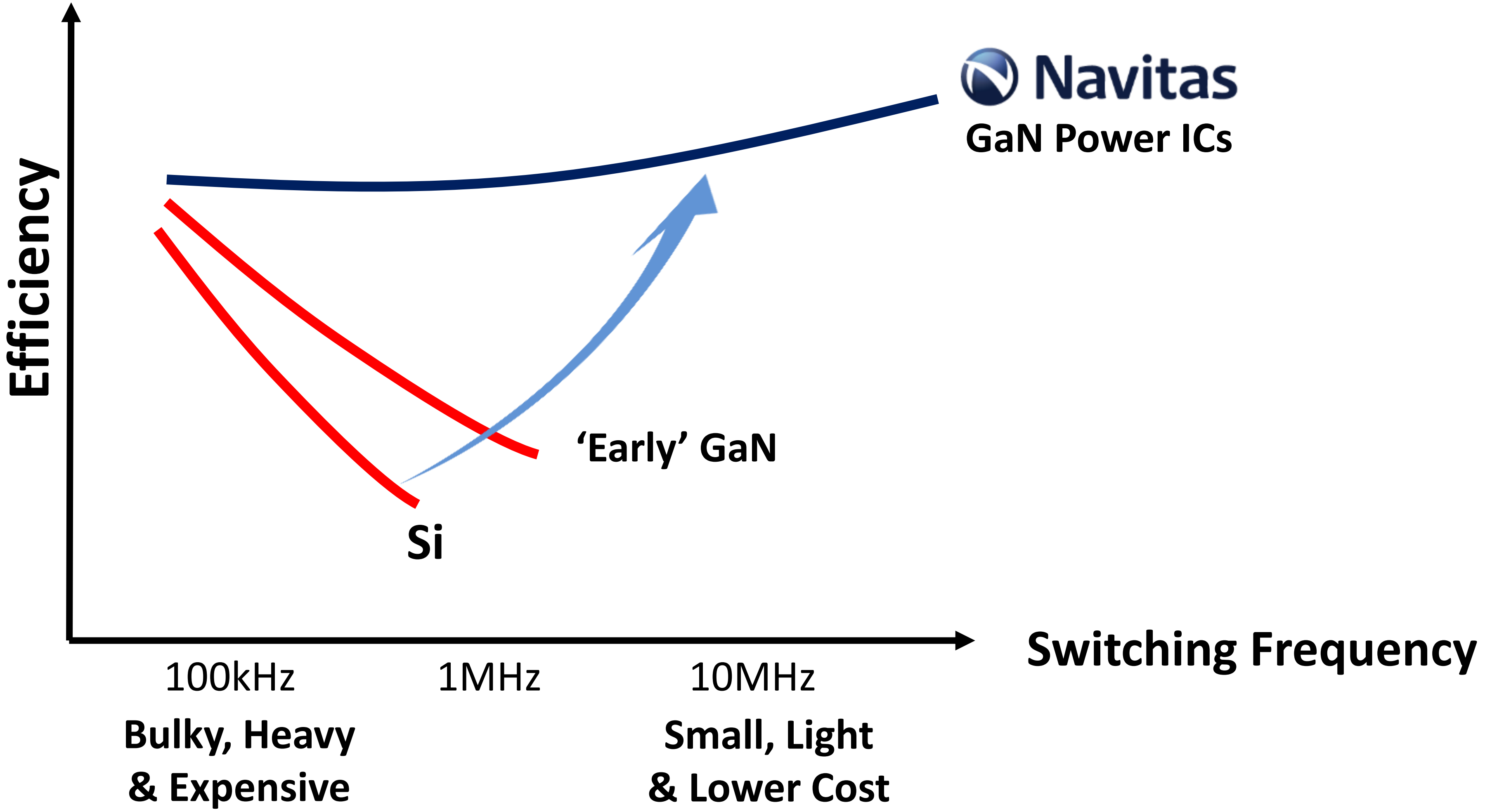




Technology	V	Pack (mm)		F_{SW} (MHz)	Eff. (%)	Power (W)
RF Si (ARF521) Microsemi POWER PRODUCTS GROUP	500	M174 22x22		27.12	91%	150
eMode GaN Navitas	650	QFN 5x6		27.12	96%	150
				40.00	93%	115

“A High-Frequency Resonant Inverter Topology With Low-Voltage Stress” (Phi-2) , Rivas, et al, MIT, IEEE Transactions on Power Electronics, Vol. 23, No. 4, July 2008 http://hdl.handle.net/1721.1/86922

GaN Power ICs Enable High Frequency & Efficiency




PCIM
ASIA
Navitas
DRIVING FOR ZERO SWITCHING LOSS
POWER SOLUTIONS
Zero Loss!
WIN, WIN, WIN
上海国际赛车场
Shanghai International Circuit