



2022中国电力电子与能量转换大会
暨中国电源学会第二十五届学术年会及展览会
2022 China Power Electronics and Energy Conversion Congress
& The 25th China Power Supply Society Conference and Exhibition

“GaN Integration Drives Next-Generation Power Systems”

Tony Liu



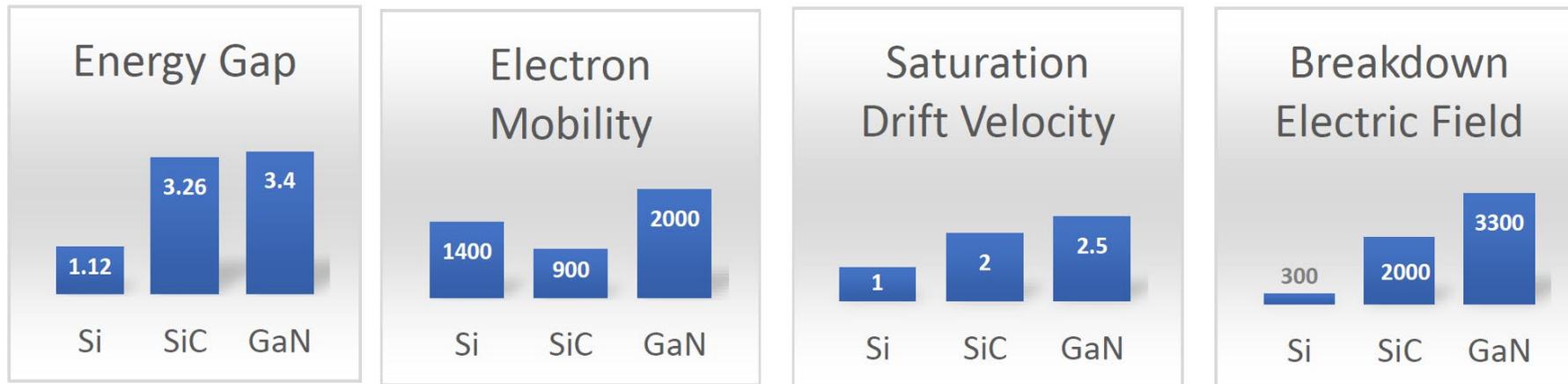
Navitas

Energy • Efficiency • Sustainability



- Introduction GaN Power
- Discrete VS Integrated GaN
- Navitas Integrated GaN IC
- Summary

Technology Comparison



**Stable/robust/
low leakage**

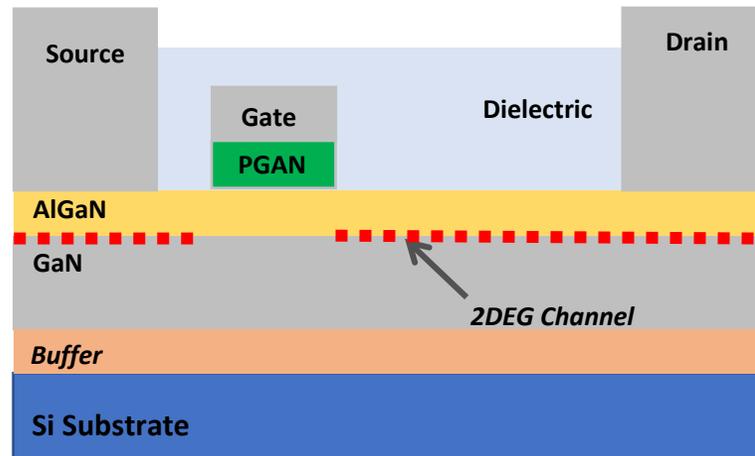
Fastest switching

Smaller die

Excluding the three semiconductors (Ga_2O_3 , Diamond, AlN) for which commercial devices are not available, GaN is the semiconductor with

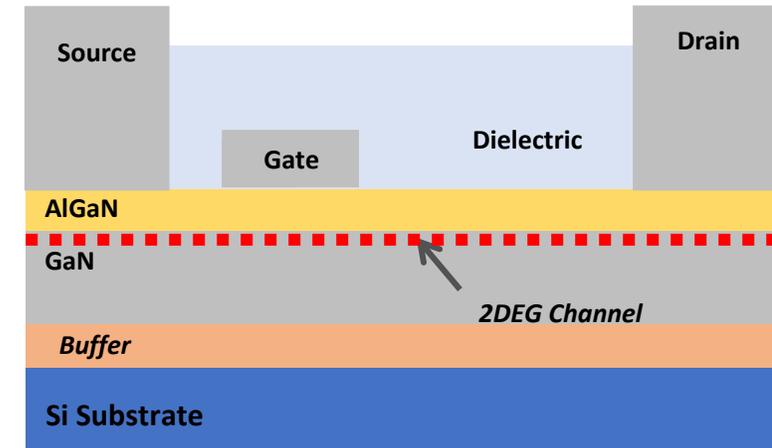
- The largest energy gap
- The largest critical field
- The highest saturation velocity

Emode



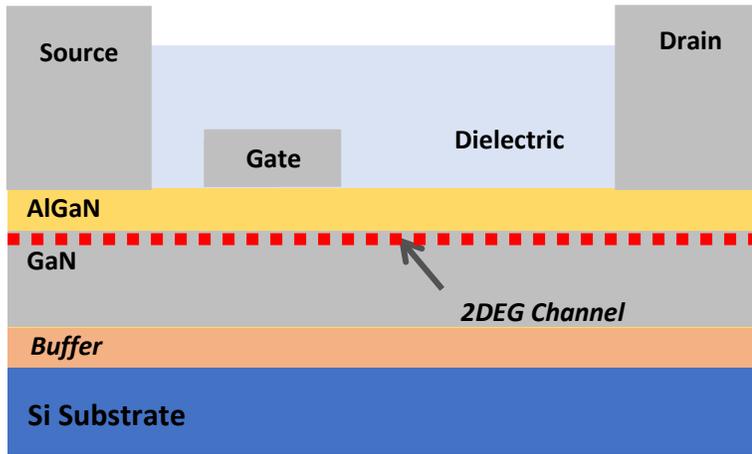
- $V_{gs} > V_{th}$, FET on
- $V_{gs} = 0$, FET off

Dmode



- $V_{gs} = 0$, FET on
- $V_{gs} < |V_{th}|$, FET off

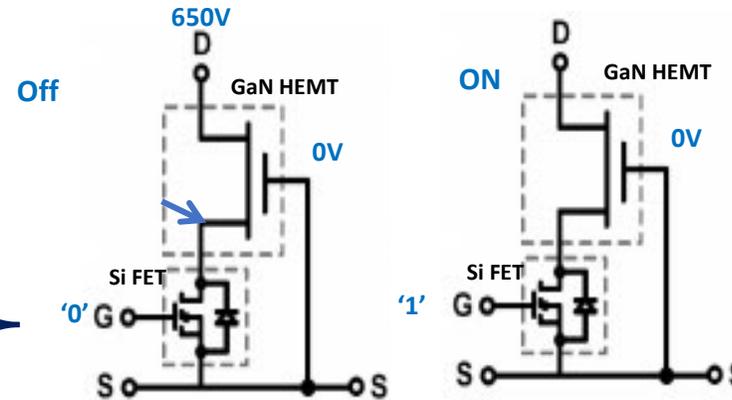
D mode



- $V_{gs}=0$, FET on
- $V_{gs}<|V_{th}|$, FET off

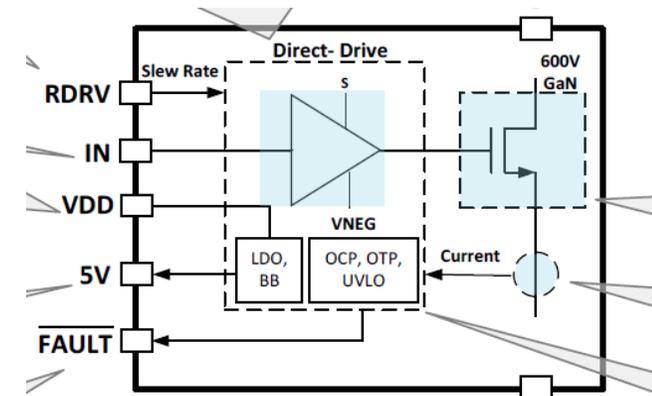
Not for switching power by itself

Cascode (Dmode GaN + LV Si FET)

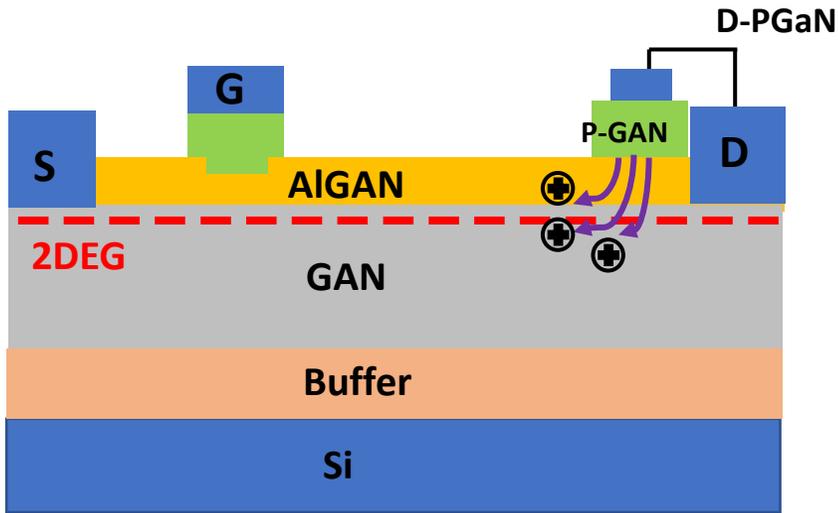


- ✓ Compatible with existing Si driver
- ✓ Low reverse conduction voltage
- ✗ Reduced benefits from all GaN power stage due to the increased $R_{ds(on)} \cdot Q_g$, reverse recovery etc.
- ✗ Large dies
- ✗ Not easy for parallel application

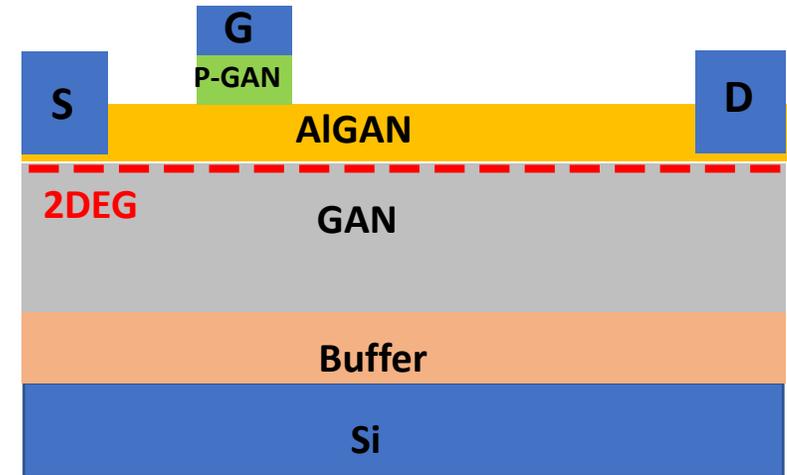
Direct Driving Dmode GaN



- ✓ Direct driving dmode GaN
- ✗ More complicated negative voltage gate driver



E mode

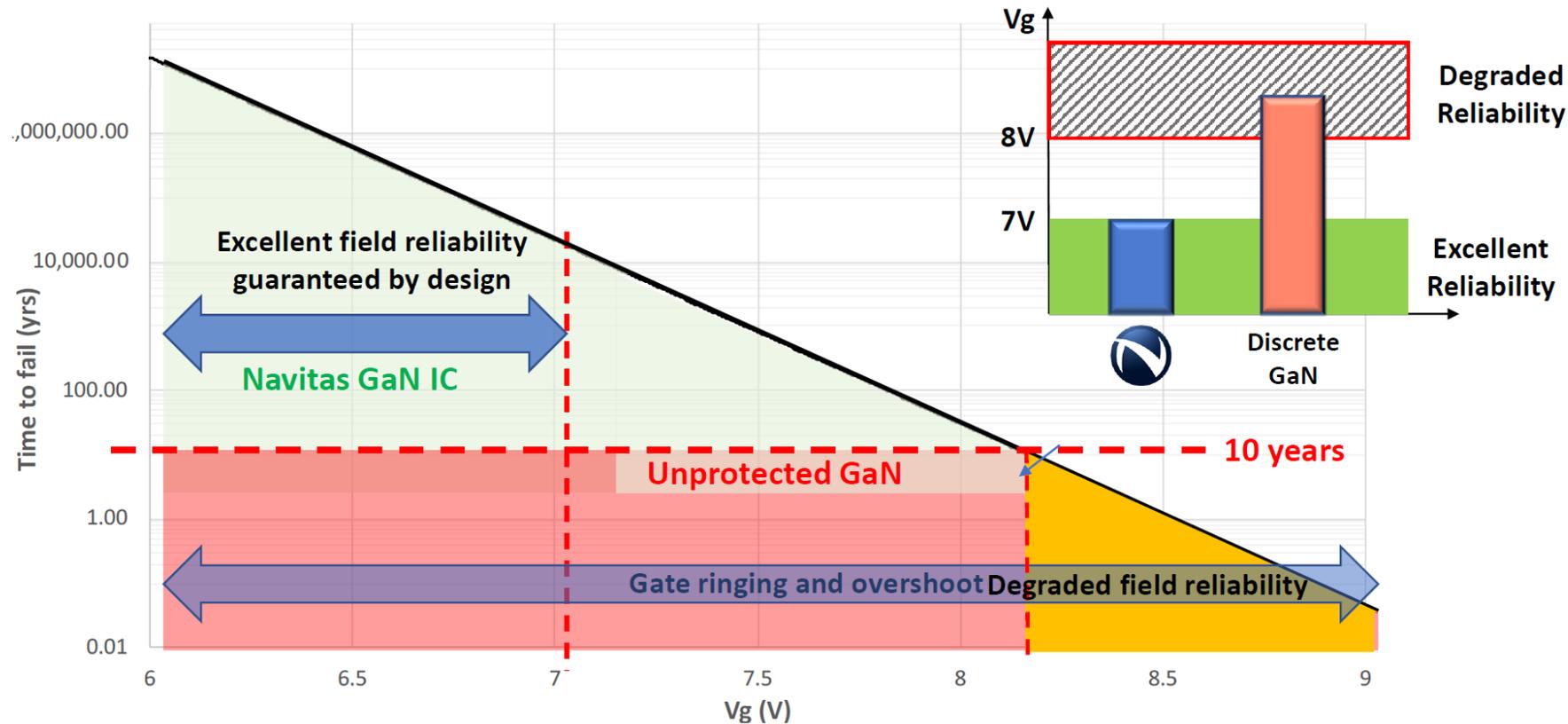


- Recessed Gate
 - ✓ Potential high V_{th}
 - ✗ Challenging process control
 - ✗ Potential Gate leakage challenge

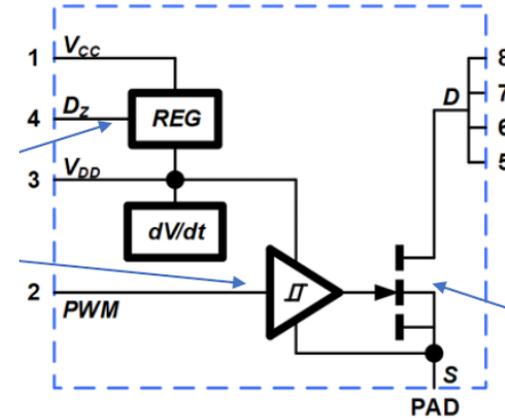
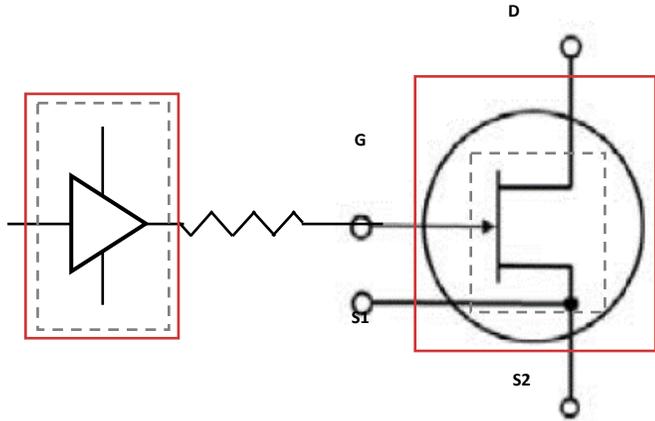
- pGaN Gate Process
 - ✓ Process control
 - ✗ Lower V_{th} , typ. < 2V
 - ✗ Limited gate SOA range

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One Major Challenge in Emode GaN



- Gate generally needs to be $> 6V$ to get the GaN ISAT/ R_{dson} benefits, but its reliability is degraded when $V_g > 8V$ or less. Unlike Si powerFET, it left very narrow margin in system board design if the powerfet is used as discrete.
- High V_g SOA GaN technology is not mature yet for wide mass production.



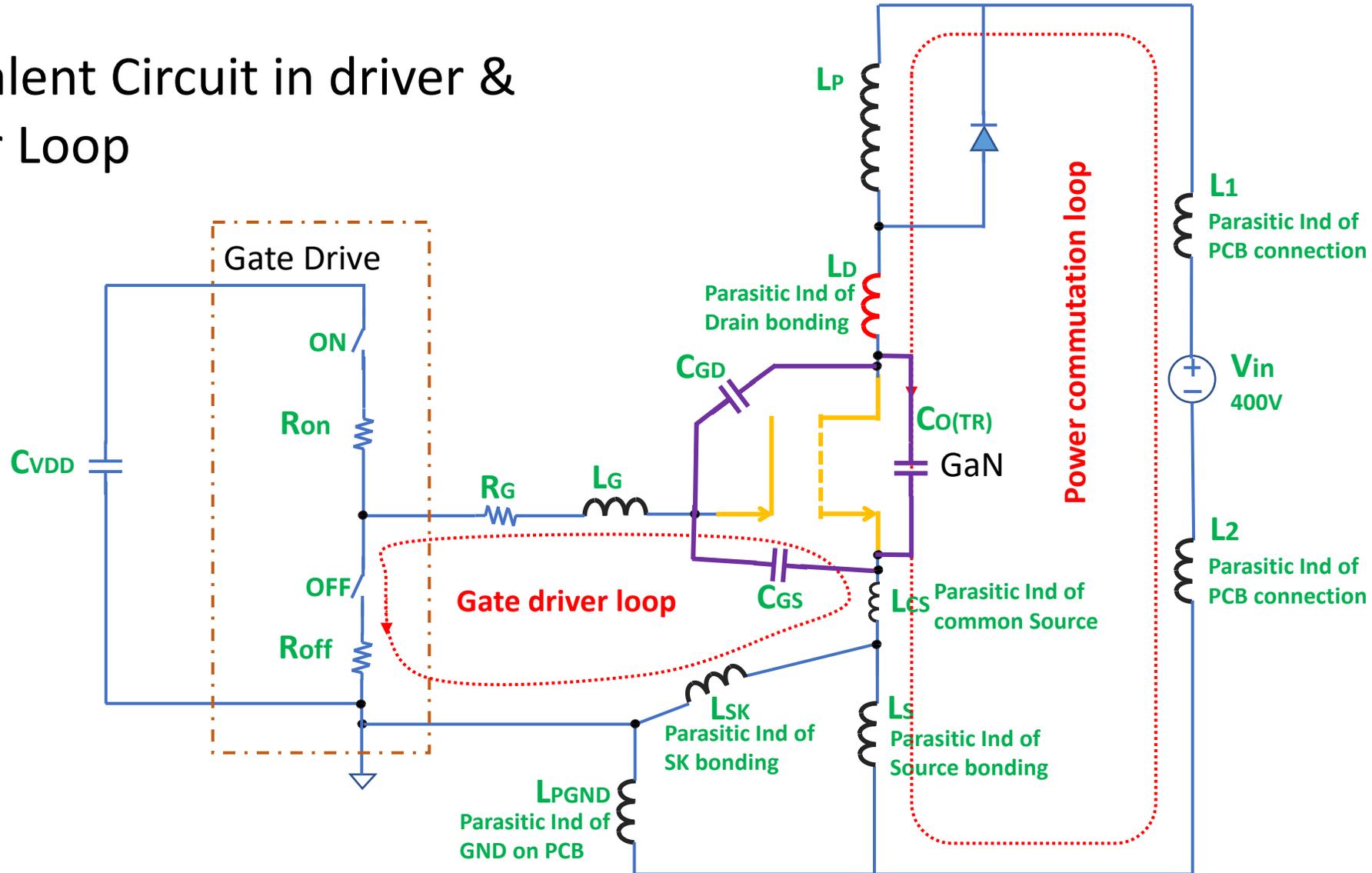
Discrete (or GaN + Si copak)

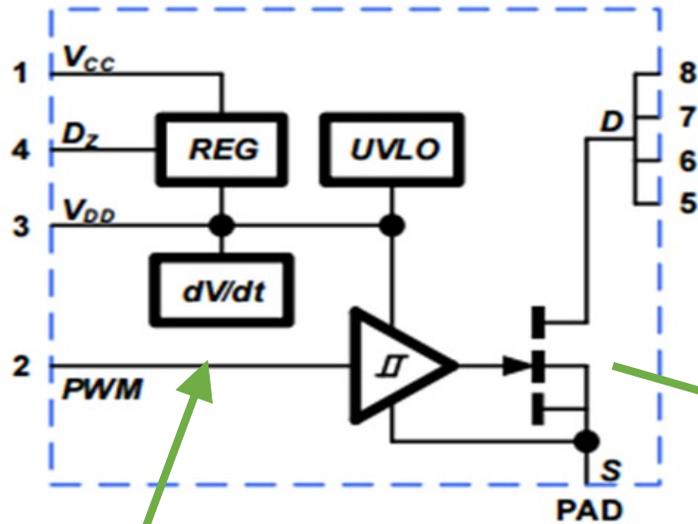
- Gate driver is on a separate die in the same package or a separate chip.
- PowerFET gate is exposed in internal die level or package level.

Integrated

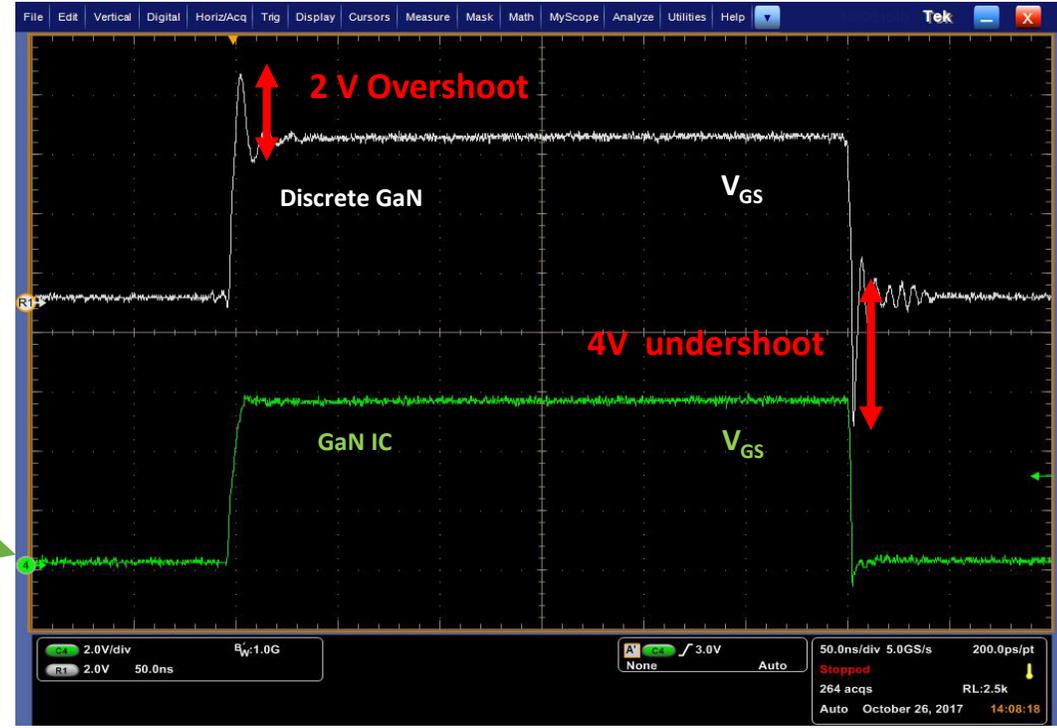
Gate Reliability Challenge

Equivalent Circuit in driver & power Loop



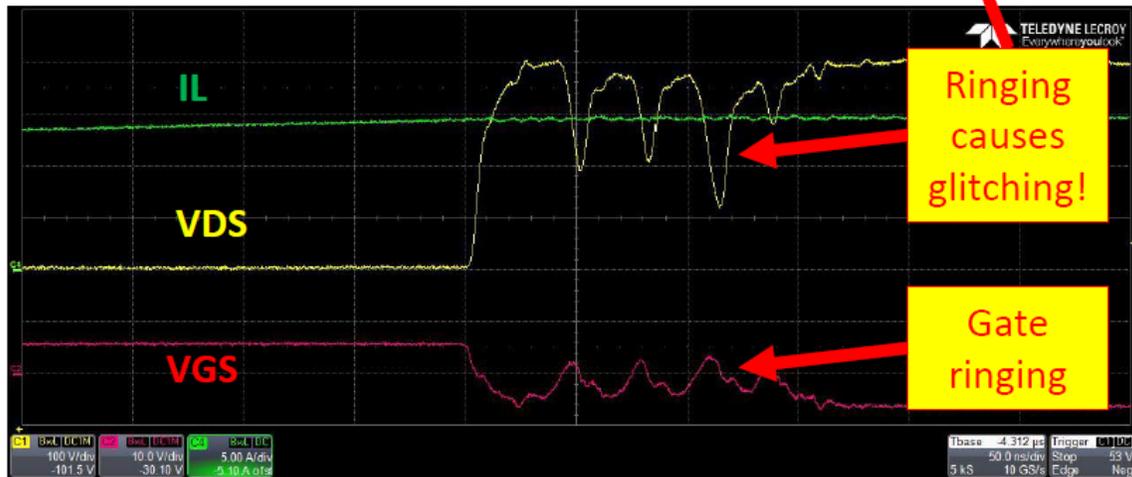
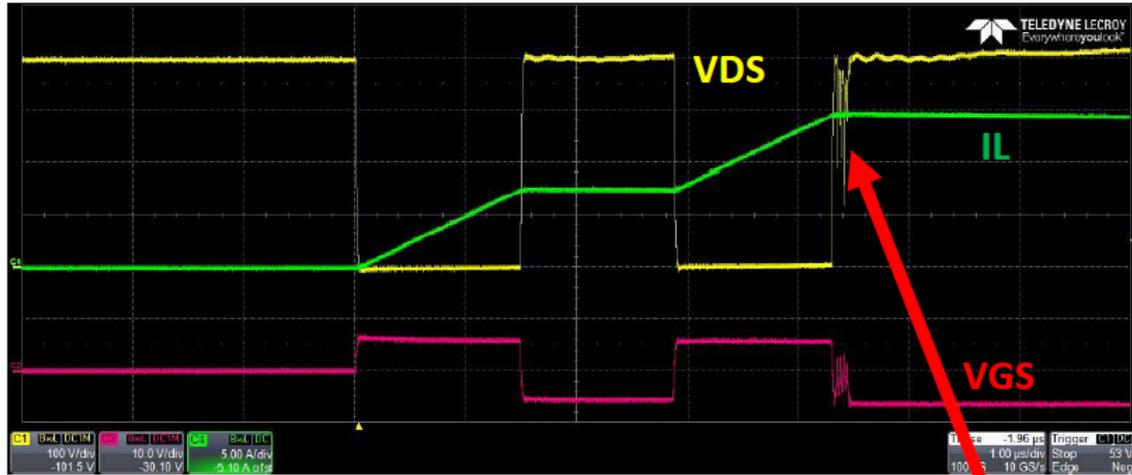


PWM Hysteresis to suppress input noise

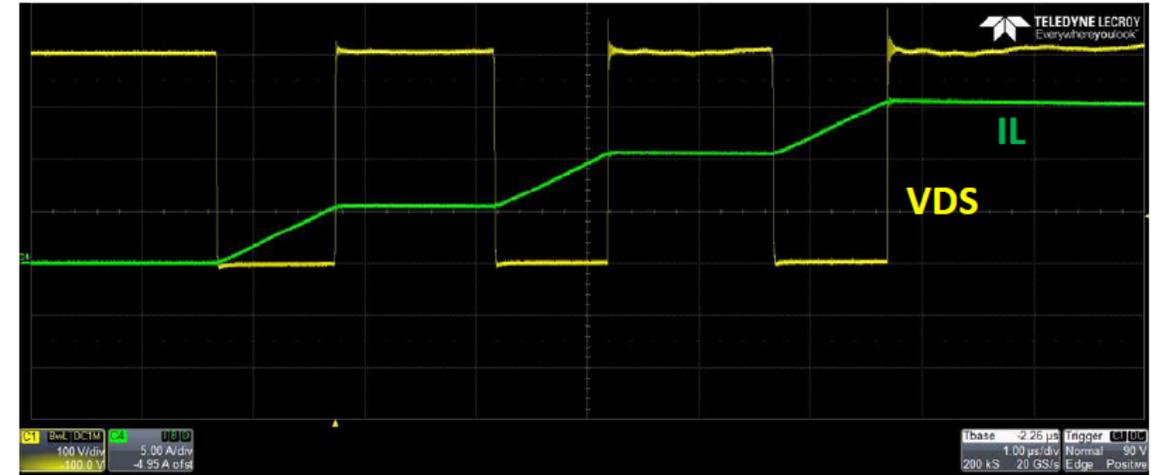


Discrete GaN vs Integrated GaN

Discrete GaN



GaNFast with GaNSense Technology



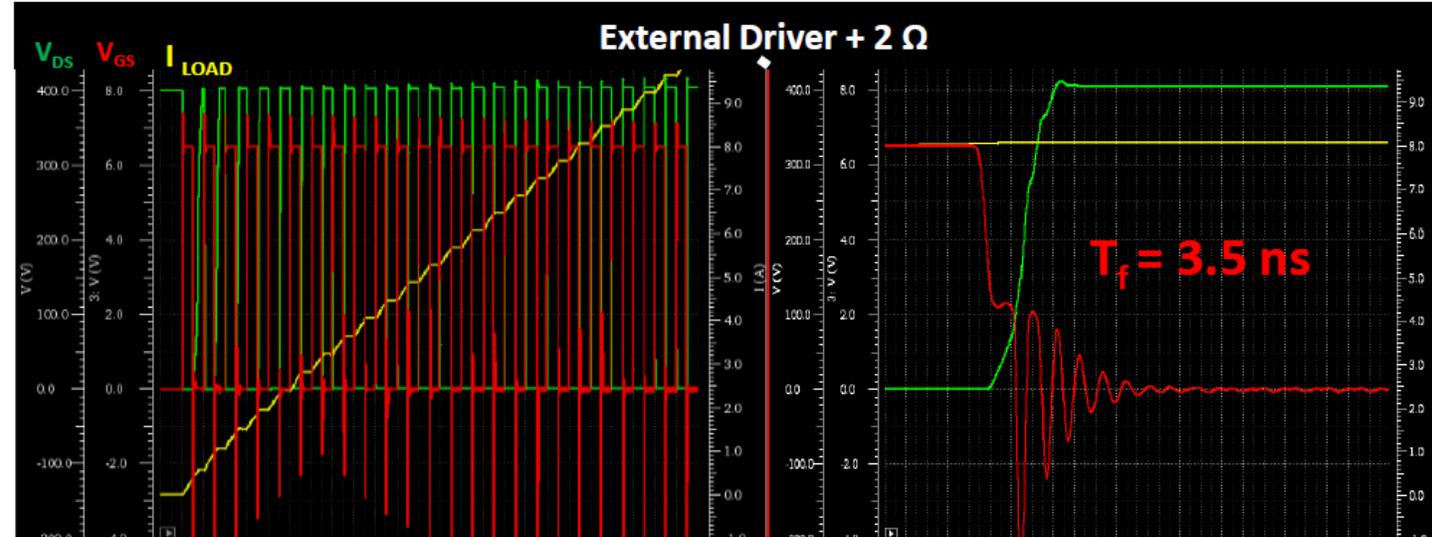
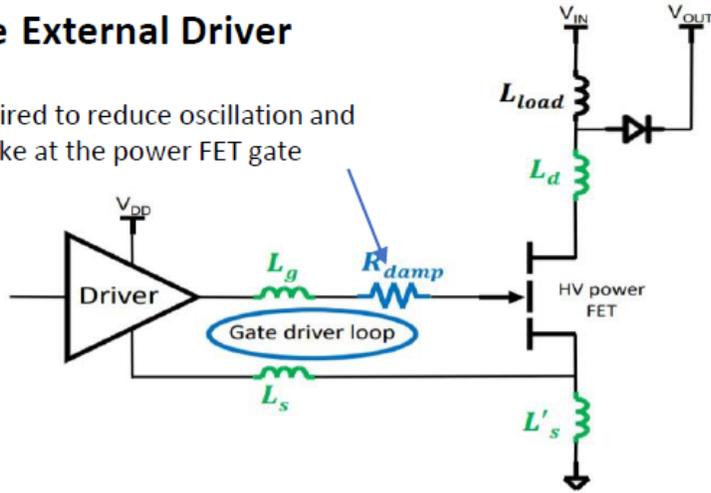
➤ Clean switching, no ringing and no glitching

- Ringing can lead to gate voltage over-stress, poor gate reliability, reduced lifetime
- Glitching can lead to poor EMI and device failure

GaN Integration for Efficiency, Speed & Stability

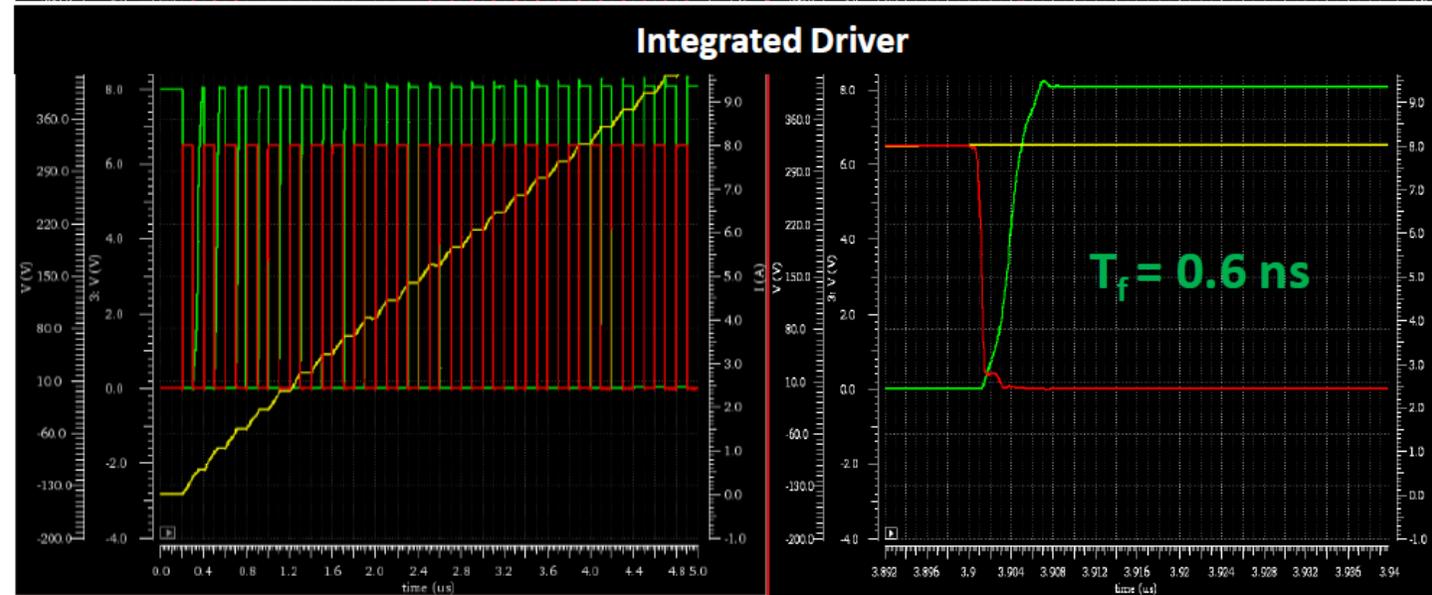
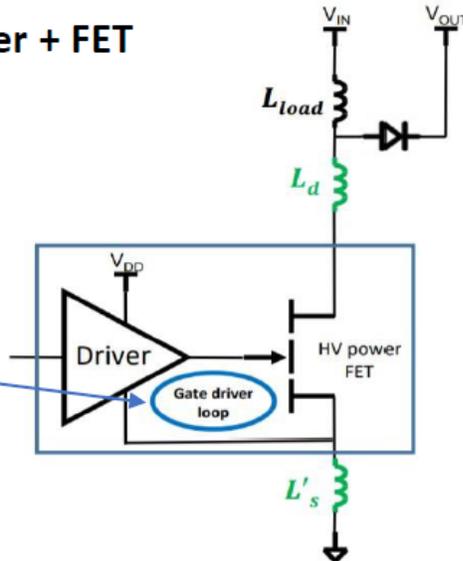
Discrete External Driver

R_{DAMP} required to reduce oscillation and voltage spike at the power FET gate



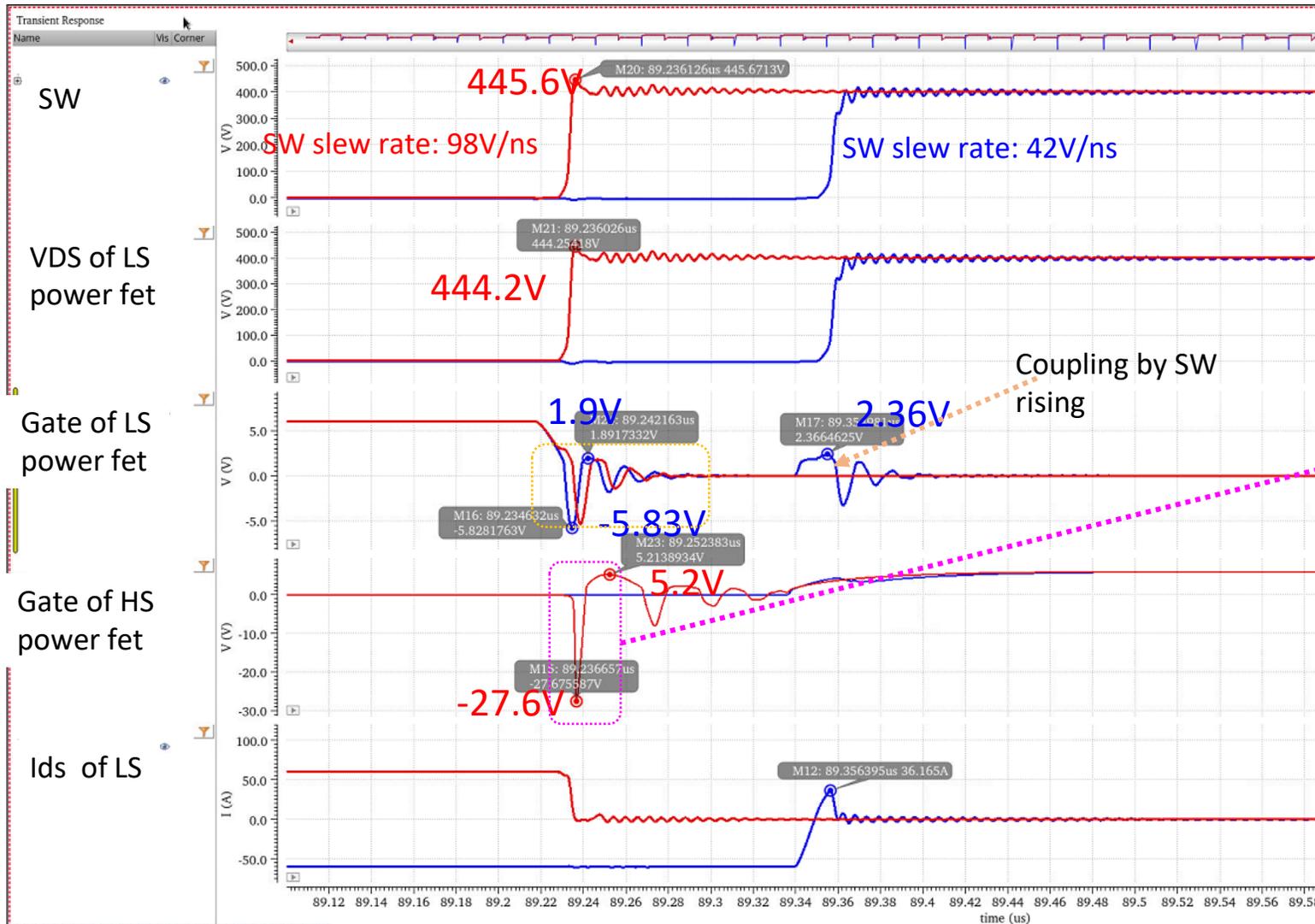
Monolithic GaN Driver + FET

Minimized gate loop eliminates any unwanted noise to effect the control and reliability of the device

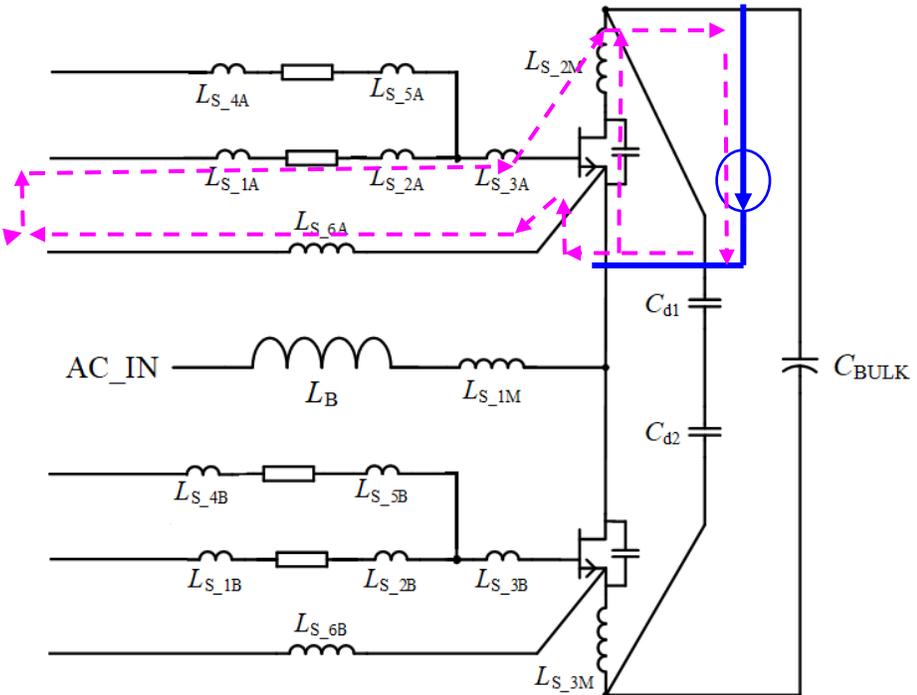


Integrated GaN Driver is a Must in High Power GaN IC Navitas

Buck Mode Iload=60A
Boost Mode Iload=60A



- Excessive gate overshoot / undershoot can be seen in GaN high power systems if powerFETs are discrete and there are noticeable PCB level parasitic inductances.
- Setup: 60A load, 20mohm Rdson HS and 20mohmohm Rdson LS buck/boost modes simulation.



Navitas Patented Integrated Turn Off di/dt Control Navitas

No Turn Off Di/Dt Control

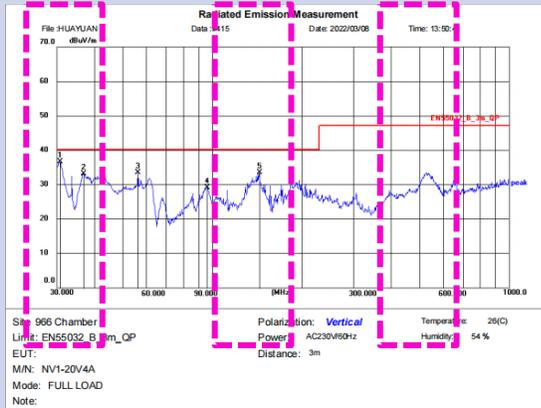
NV6134A

With Turn Off Di/Dt Control

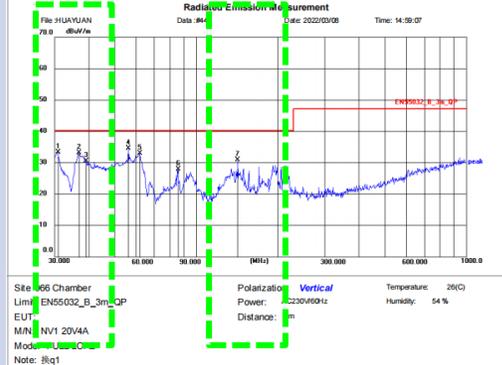
NV6134C

Summary

230V
20V/4A

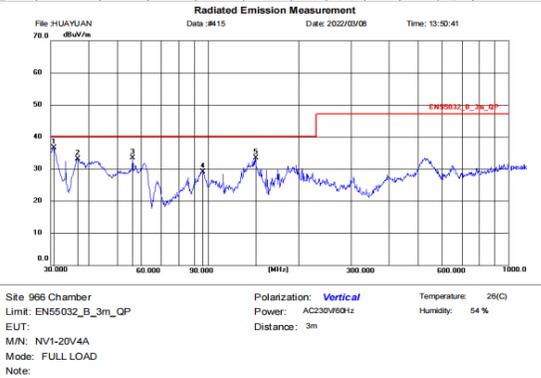


No.	Frequency (MHz)	Reading (dBuV)	Factor (dB/m)	Level (dBuV/m)	Limit (dBuV/m)	Margin (dB)	Detector	Height (cm)	Azimuth (deg.)	P/F	Remark
1 *	30.6379	23.74	12.90	36.64	40.00	3.36	peak			P	
2	36.7662	19.78	13.40	33.18	40.00	6.82	peak			P	
3	56.1974	19.33	14.15	33.48	40.00	6.52	peak			P	
4	96.0986	17.52	11.61	29.13	40.00	10.87	peak			P	

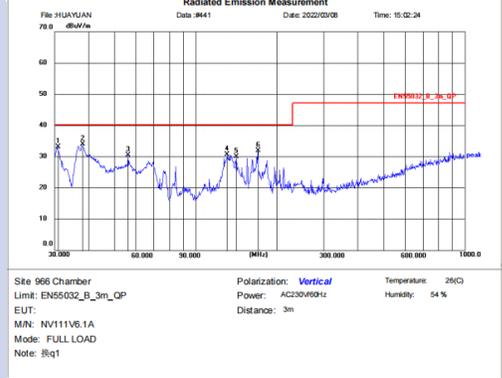


No.	Frequency (MHz)	Reading (dBuV)	Factor (dB/m)	Level (dBuV/m)	Limit (dBuV/m)	Margin (dB)	Detector	Height (cm)	Azimuth (deg.)	P/F	Remark
1	30.7455	20.38	12.91	33.29	40.00	6.71	peak			P	
2	36.7662	19.83	13.40	33.23	40.00	6.77	peak			P	
3	39.1616	16.83	13.77	30.60	40.00	9.40	peak			P	
4 *	56.1974	20.42	14.15	34.57	40.00	5.43	peak			P	
5	61.7781	19.39	13.60	32.99	40.00	7.01	peak			P	
6	85.5977	16.97	10.94	27.91	40.00	12.09	peak			P	
7	142.8243	16.52	14.45	30.97	40.00	9.03	peak			P	

230V
11V/6.
1A



No.	Frequency (MHz)	Reading (dBuV)	Factor (dB/m)	Level (dBuV/m)	Limit (dBuV/m)	Margin (dB)	Detector	Height (cm)	Azimuth (deg.)	P/F	Remark
1 *	30.6379	23.74	12.90	36.64	40.00	3.36	peak			P	
2	36.7662	19.78	13.40	33.18	40.00	6.82	peak			P	
3	56.1974	19.33	14.15	33.48	40.00	6.52	peak			P	
4	96.0986	17.52	11.61	29.13	40.00	10.87	peak			P	
5	143.8295	18.91	14.66	33.57	40.00	6.43	peak			P	



No.	Frequency (MHz)	Reading (dBuV)	Factor (dB/m)	Level (dBuV/m)	Limit (dBuV/m)	Margin (dB)	Detector	Height (cm)	Azimuth (deg.)	P/F	Remark
1	30.7455	20.23	12.91	33.14	40.00	6.86	peak			P	
2 *	38.0783	20.42	13.60	34.02	40.00	5.98	peak			P	
3	56.1974	16.31	14.15	30.46	40.00	9.54	peak			P	
4	131.2965	16.25	14.51	30.76	40.00	9.24	peak			P	
5	141.8262	15.72	14.23	29.95	40.00	10.05	peak			P	
6	170.1948	16.95	15.00	31.95	40.00	8.05	peak			P	

Gen4 added patented turn off di/dt control

- 2-3db better at 30-40Meg
- 5db better margin at 100Meg
- 10db better margin at 550Meg

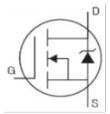
Gen4 added patented turn off di/dt control

- 2-3db better at 30-40Meg
- 3db better margin at 100Meg
- 10db better margin at 550Meg

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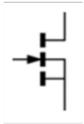
The GaN Revolution: Ultimate Integration

Silicon FET



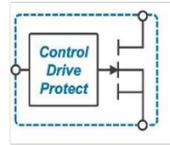
- Old, slow
- High Q_g
- High C_{oss}
- $F_{sw} < 100$ kHz

Discrete GaN



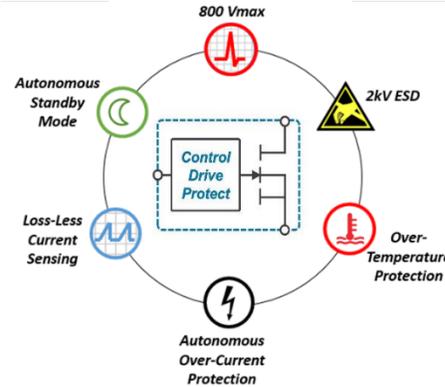
- Exposed gate
- External gate drive
- dV/dt sensitivity
- Layout sensitivity
- ESD sensitivity
- Unknown reliability
- Unknown robustness

GaNFast™ 200-300 kHz



- ✓ Internal Gate
- ✓ Integrated Gate Drive
- ✓ dV/dt Immunity
- ✓ Layout Insensitive
- ✓ 2 kV ESD rating
- ✓ Proven Reliability
- ✓ Proven Robustness

GaNSense™ 500 kHz

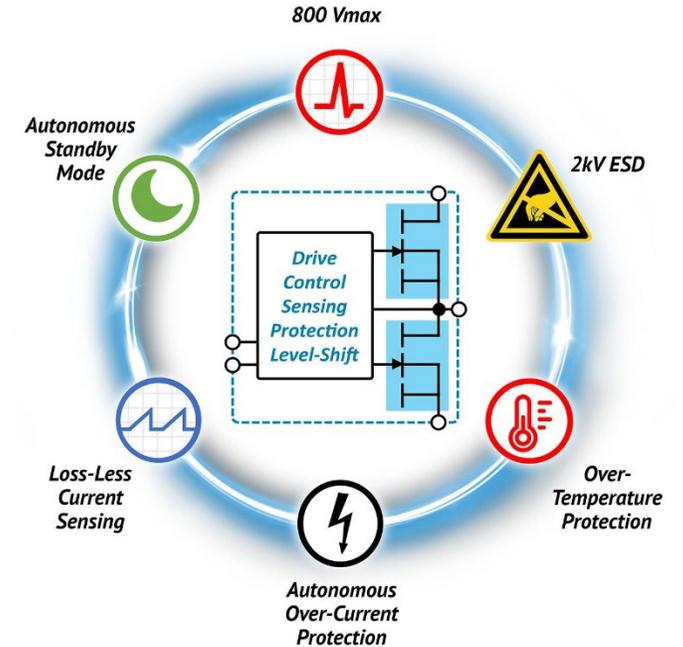


GaNFast plus:

- ✓ Autonomous Standby
- ✓ Autonomous Protection
- ✓ Loss-less Current Sensing
- ✓ High Precision
- ✓ High Efficiency

GaNSense Half-Bridge

1 MHz

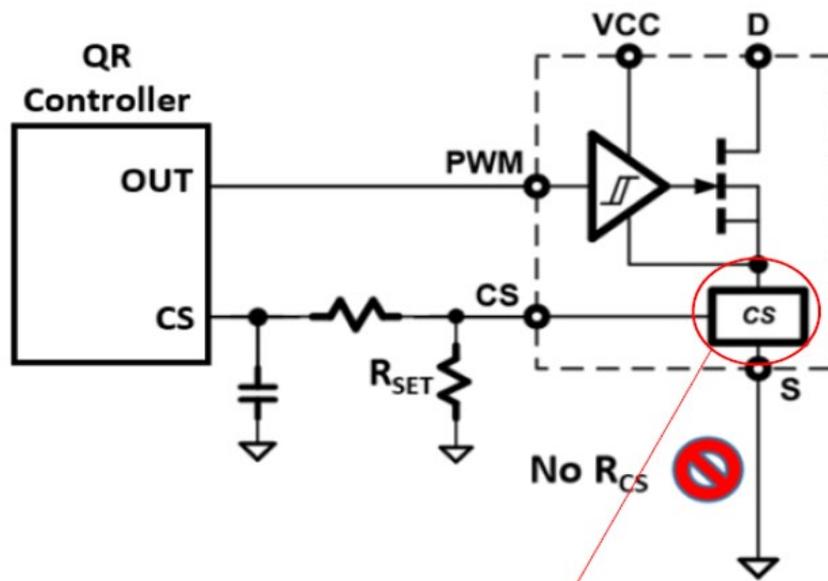


GaNSense plus:

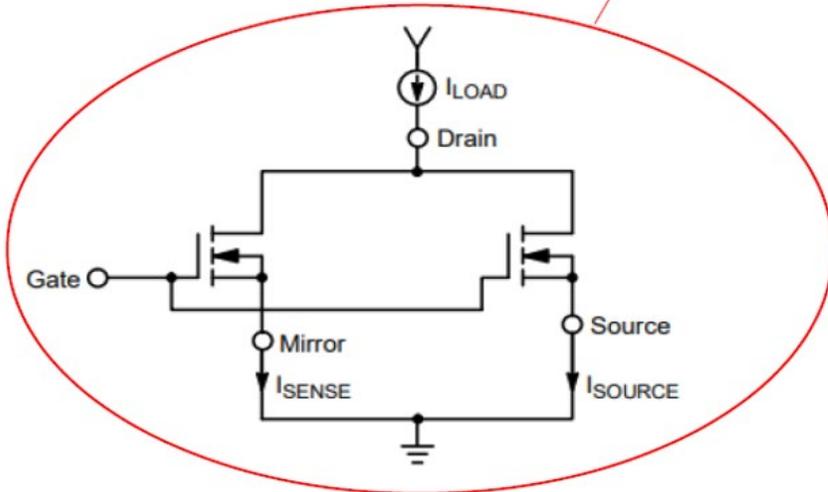
- ✓ Highest integration
 - ✓ integrated HS and LS FETs
 - ✓ Integrated level-shift isolation
 - ✓ integrated boot-strap
 - ✓ Shoot-through protection
 - ✓ Enlarged cooling pads
- ✓ Fastest switching
- ✓ Highest efficiency



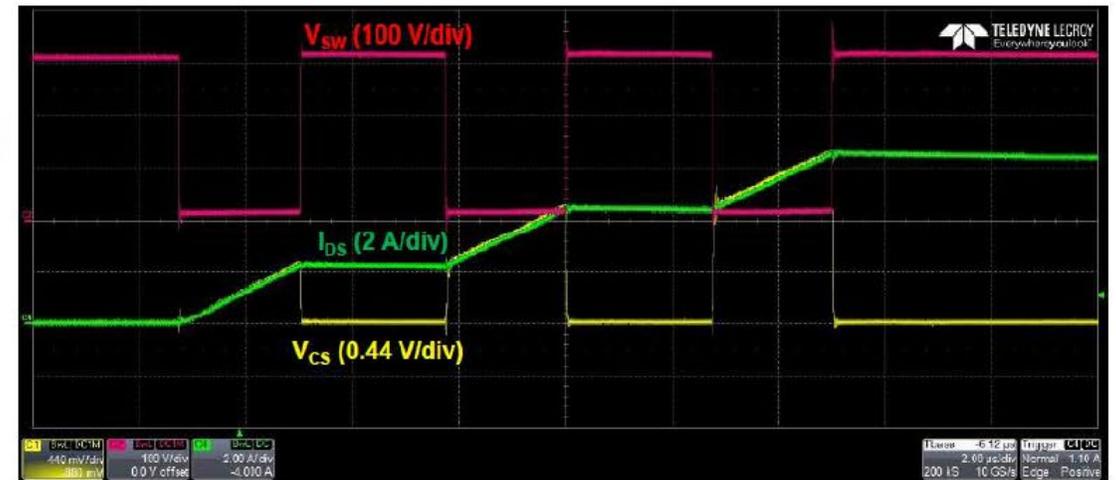
Lossless Current Sensing



DCM Tracking
Example @ 192KHz

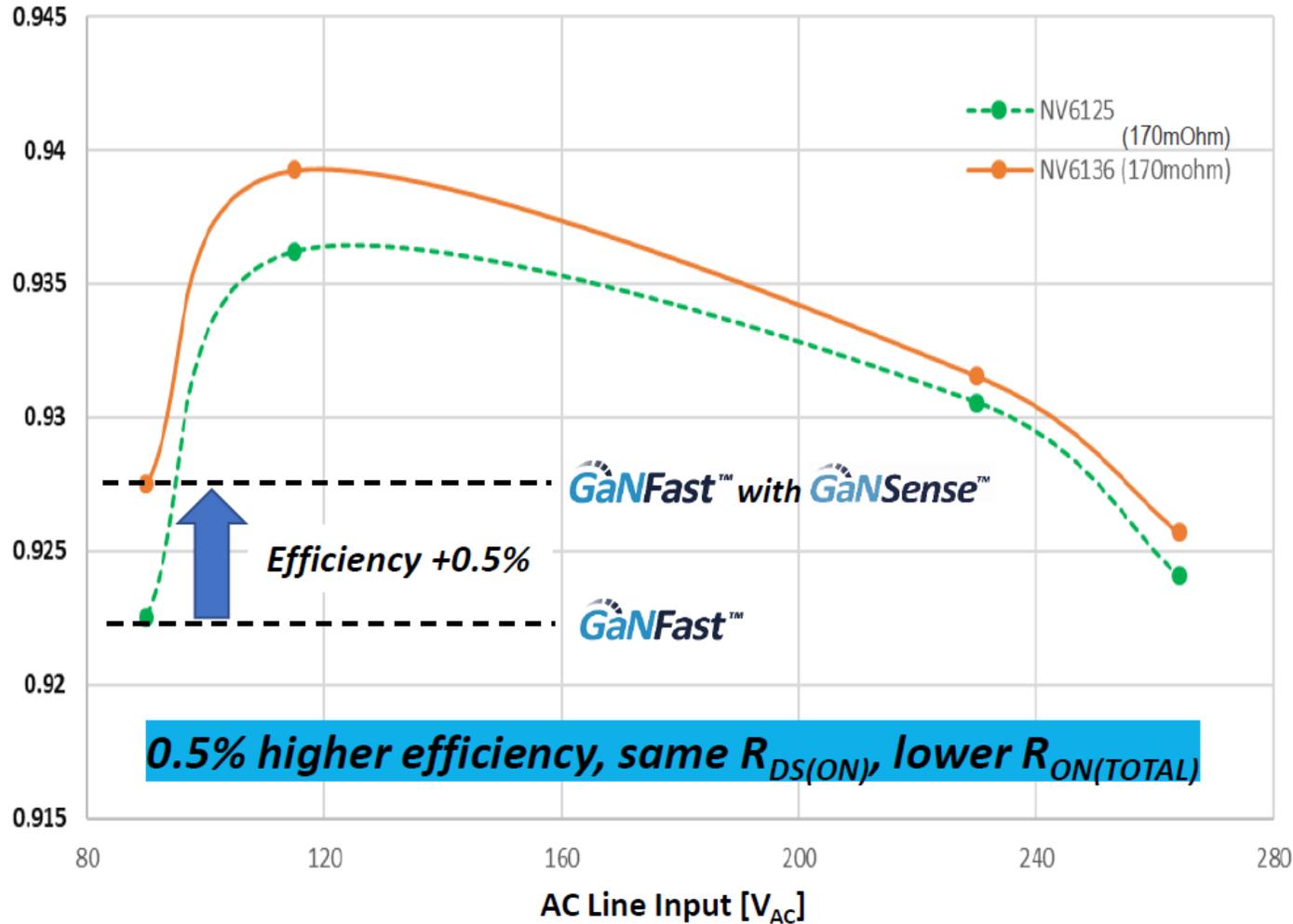


CCM Tracking
Example @ 200KHz

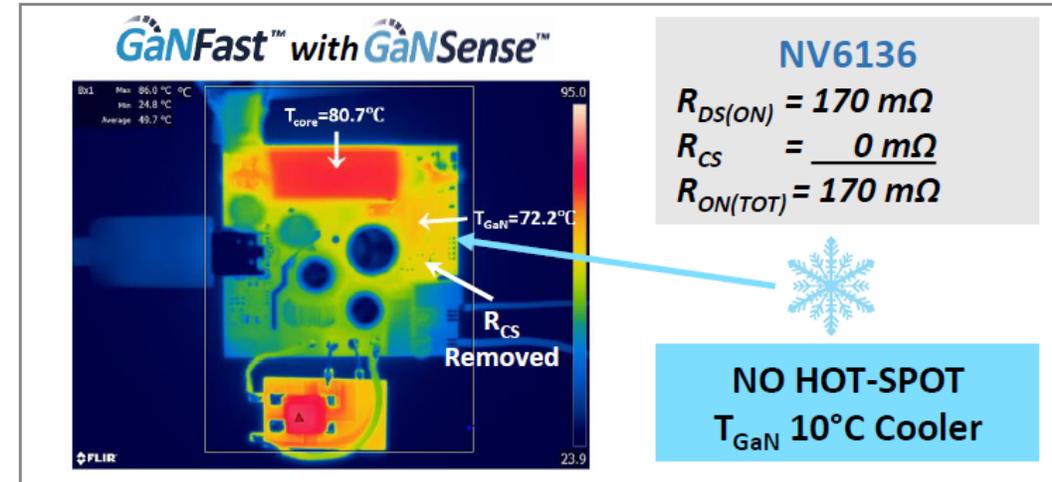
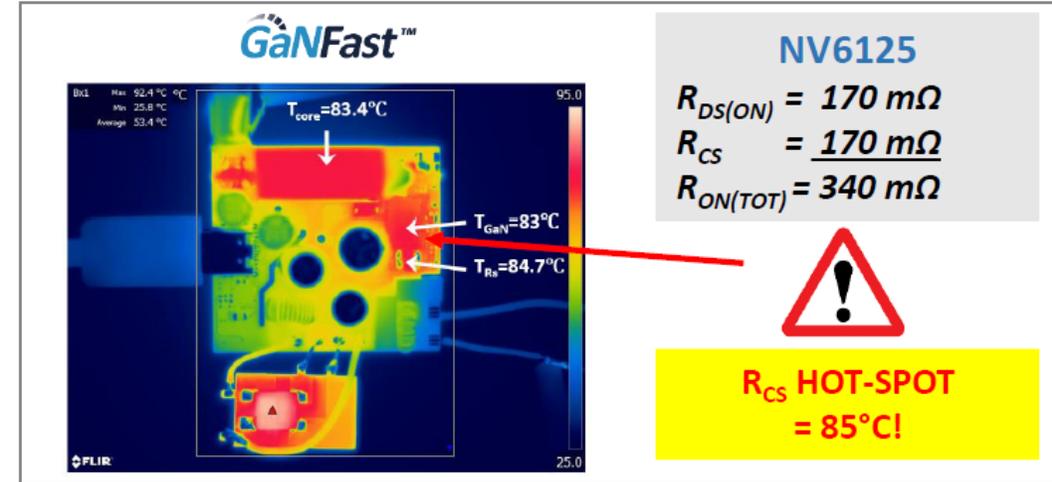


Lossless Current Sensing Efficiency Benefit

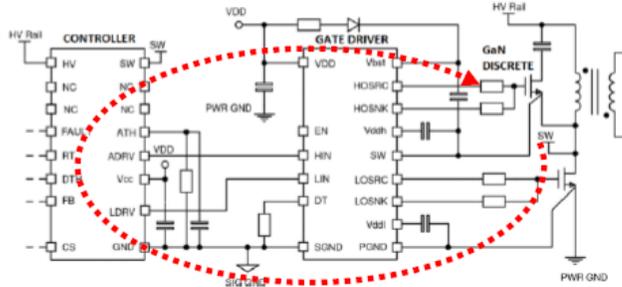
Efficiency (60W HFQR, 20V/3A)



60W HFQR, 90V_{AC}, 20V/3A, 1 Hour



Discrete GaN Solution

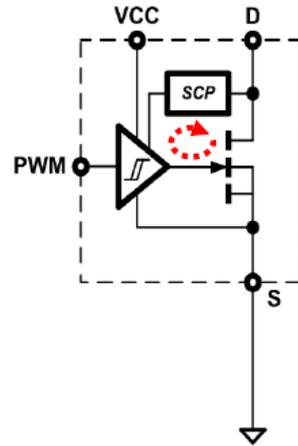


Uses QR controller OCP function

$T_{OCP} = 180 \text{ ns}$

- Existing solutions use ext. R_{CS}
- Filter + controller delay slow

GaNFast™
with
GaNSense™

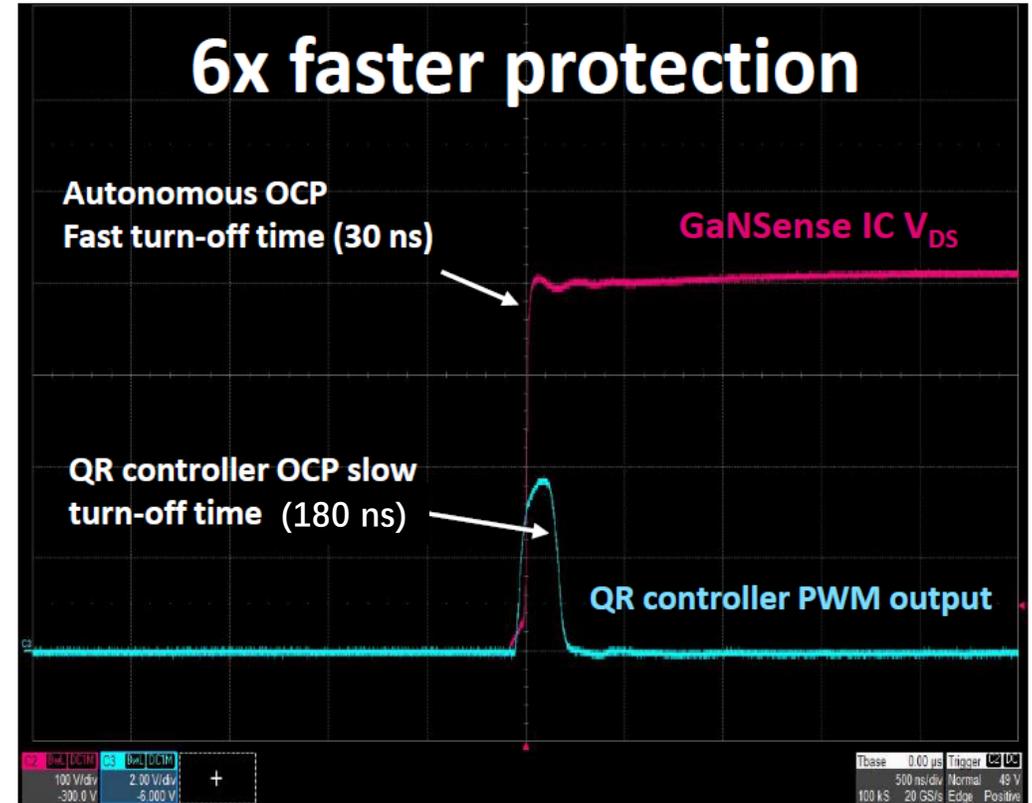


Integrated SCP function

$T_{OCP} = 30 \text{ ns}$

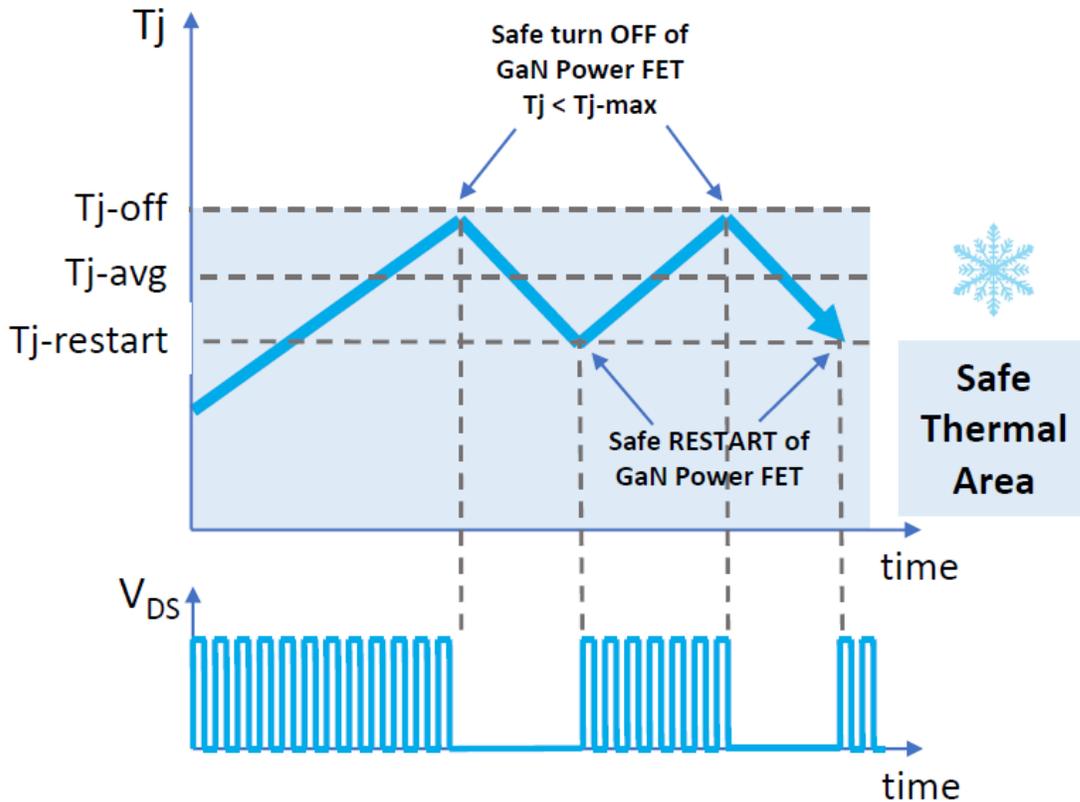
- Autonomous OCP
- Fast-acting self-protection
- Cycle-by-cycle protection
- Excellent robustness

6x faster protection

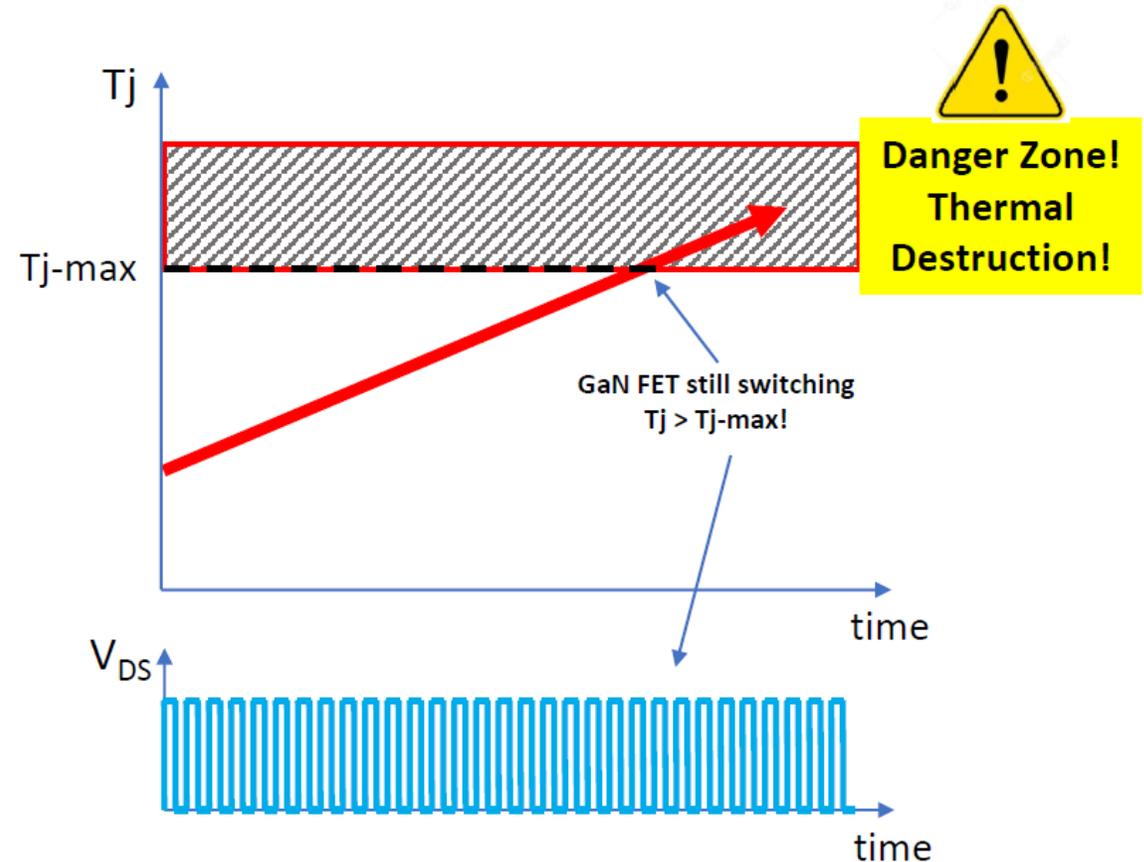


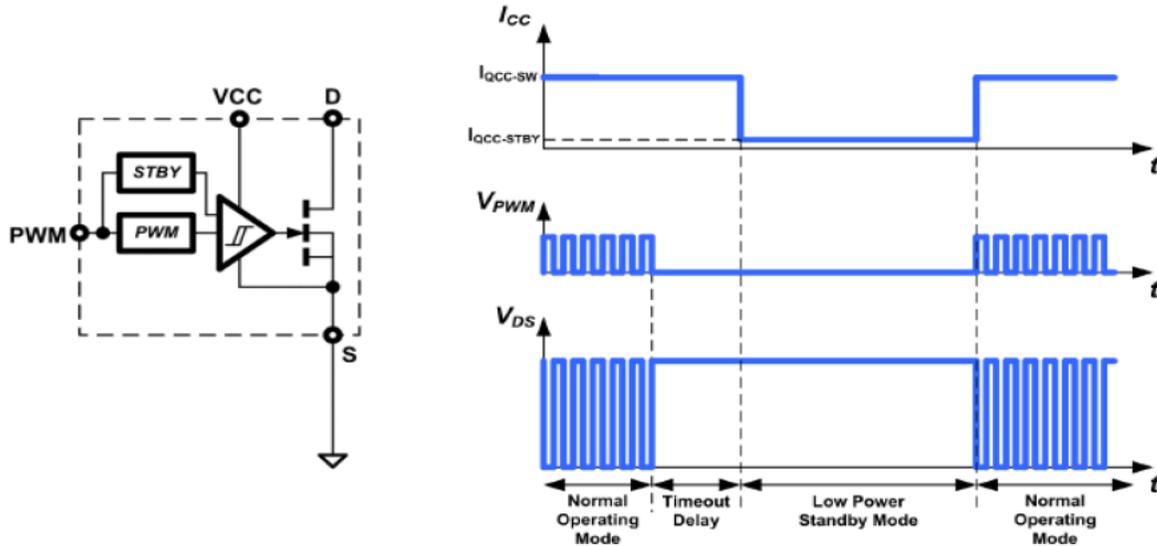
- QR controller OCP = slow turn-off (180 ns)
- NV6136 OCP = fast turn-off (30 ns)

GaNSense IC w/OTP



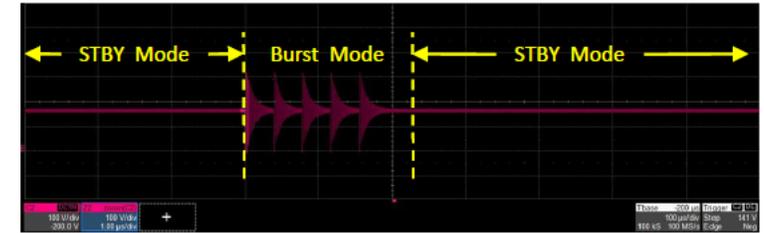
Unprotected GaN





Autonomous low-power standby mode simplified circuit and timing diagram

- GaN IC autonomously enters standby mode in the absence of PWM signals.
- Super fast wakeup at next PWM rising edge.
 - No discernable effect on propagation delay, current sense performance, etc...
- In the High Frequency QR Flyback no load example above, **full system standby losses are reduced 17%**
 - NV6125 Gen 2 GaNFast part (175mΩ typical).
 - NV6136 Gen 3 GaNSense part (170mΩ typical).

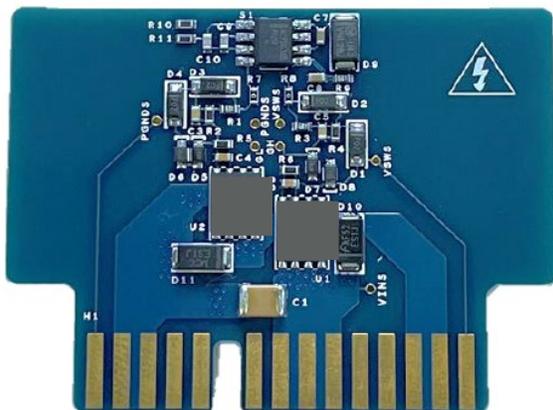


HFQR, no load

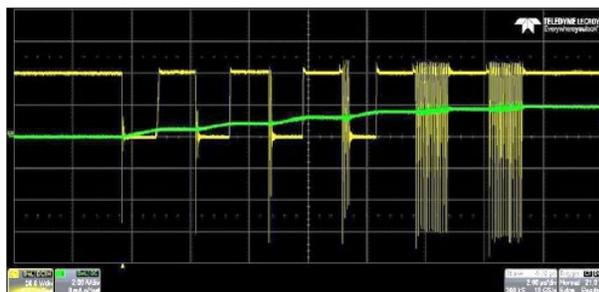
P_{IN} (no load)	115 V _{AC}	230 V _{AC}
NV6125	39 mW	40 mW
NV6136	33 mW	33 mW



Discrete GaN



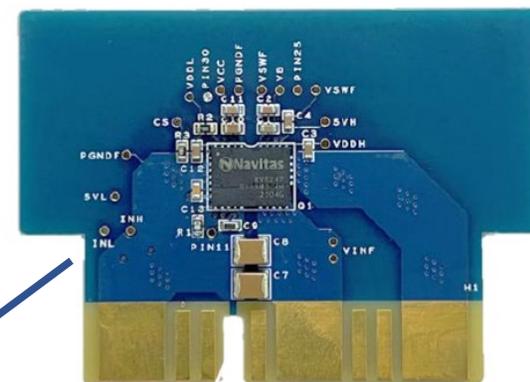
2x Discrete GaN
+28 components



Risky, Erratic, Lossy

2x fewer components
3x Smaller design
Internal Gate protection
No Gate Ringing

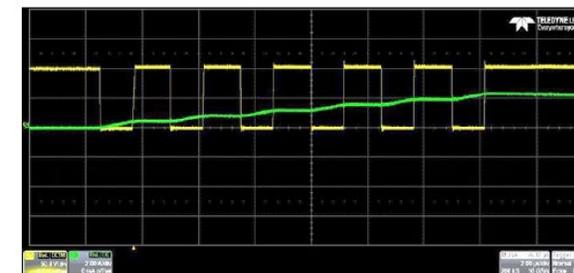
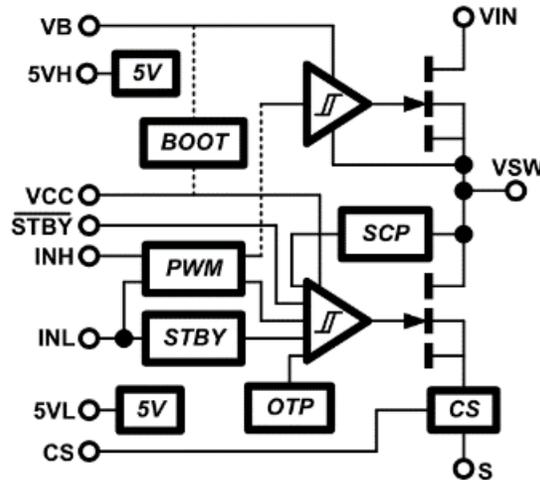
GaNFast IC



1x GaN Power IC
+14 components

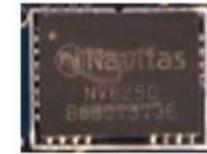
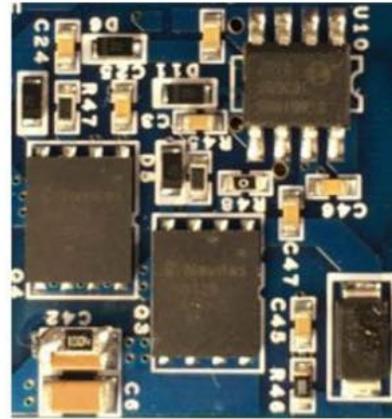
1/2 the Components
1/3 the Area

NV624x HB Family

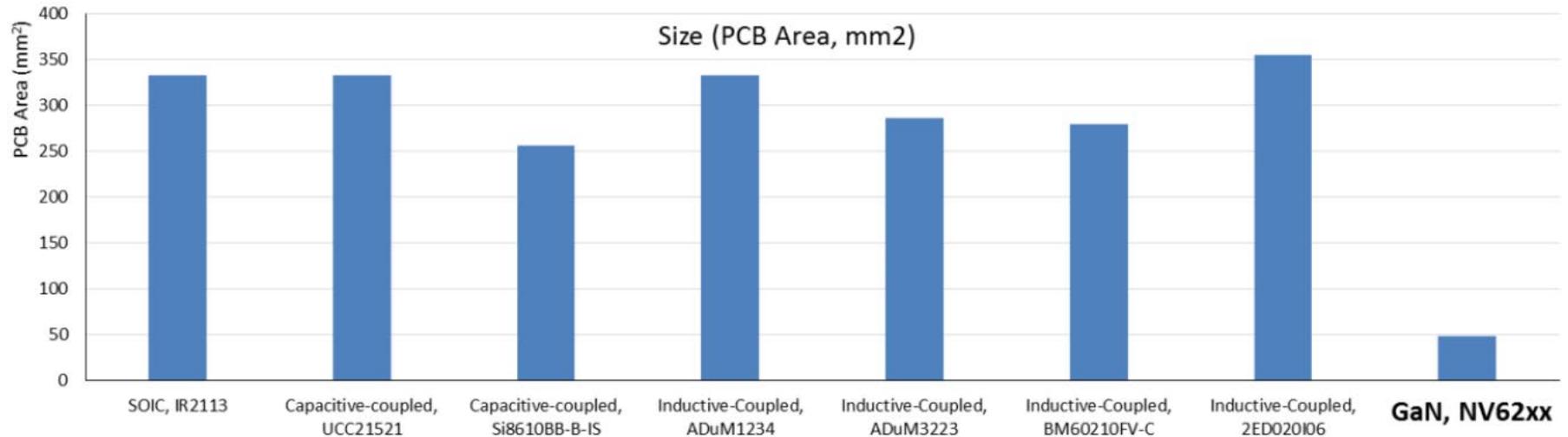


Reliable, Predictable, Efficient

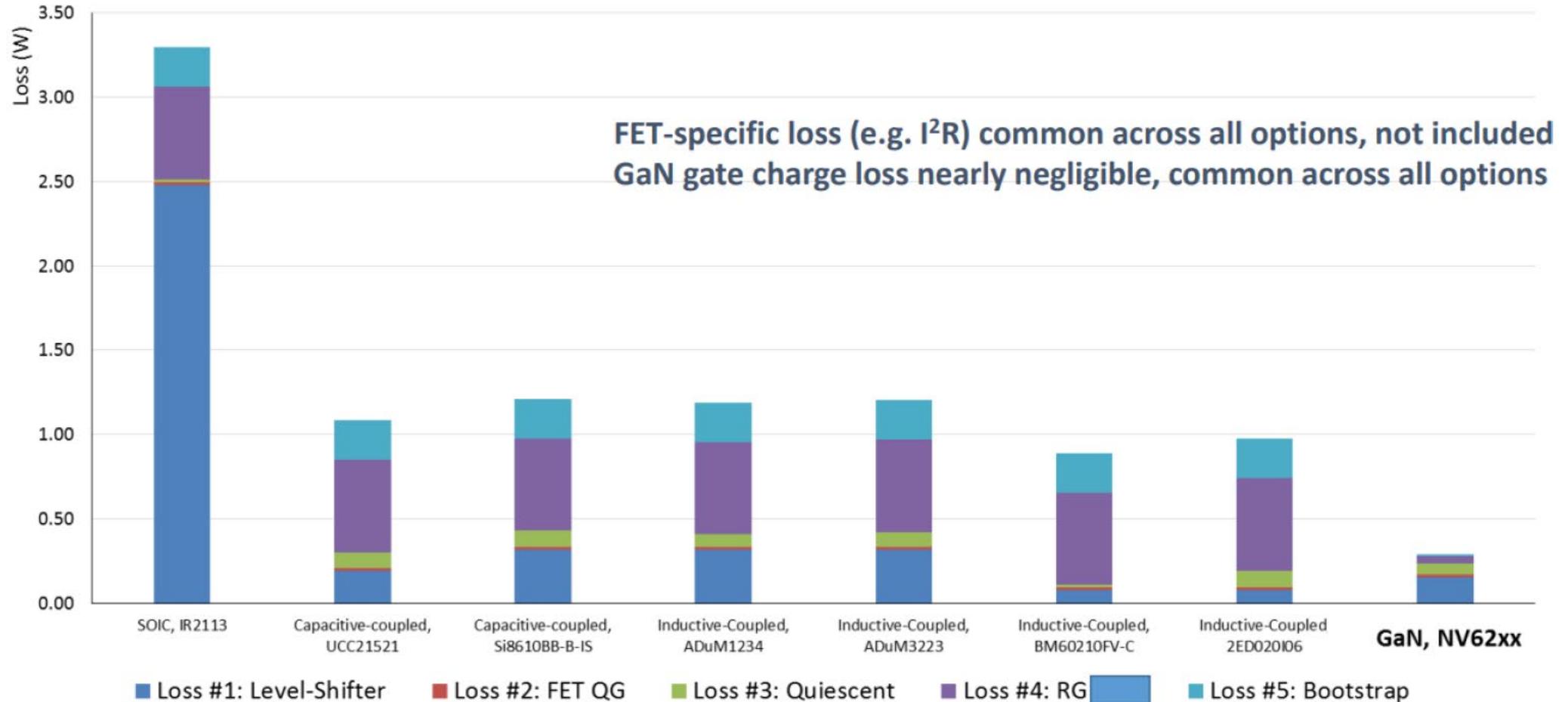
Digital Isolator
2x Single GaN
Power ICs
Bootstrap diode
Passives



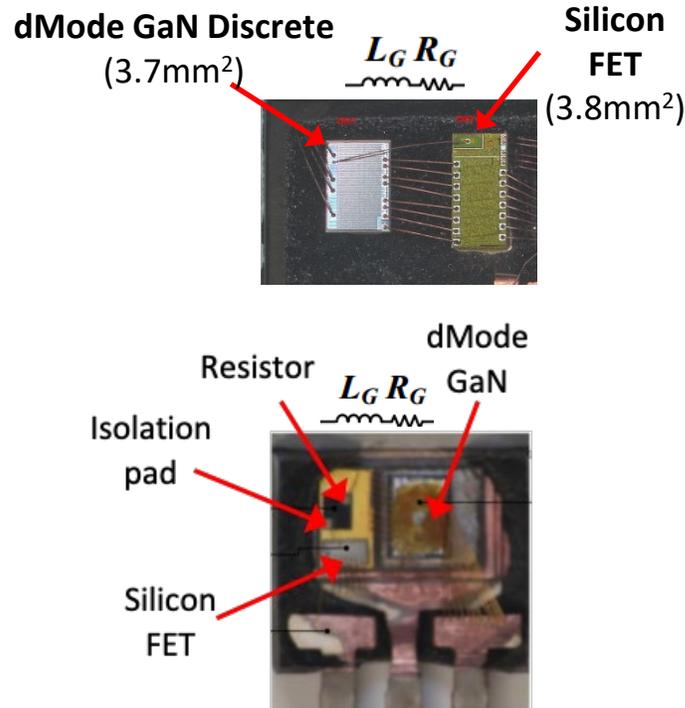
Half Bridge GaN
Power ICs 5X smaller
than alternatives



- 3x Lower Drive and Level Shift Loss at 1 MHz

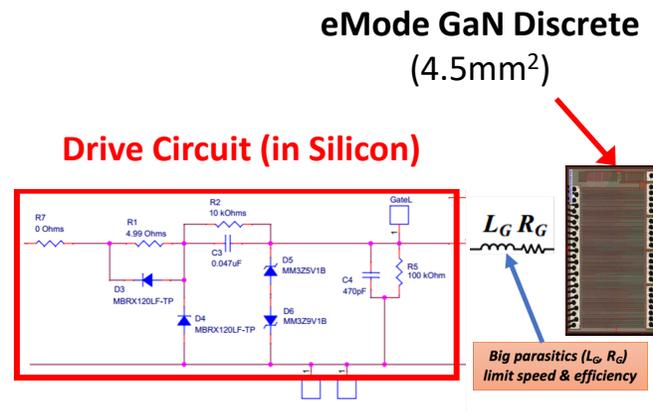


Discrete dMode GaN



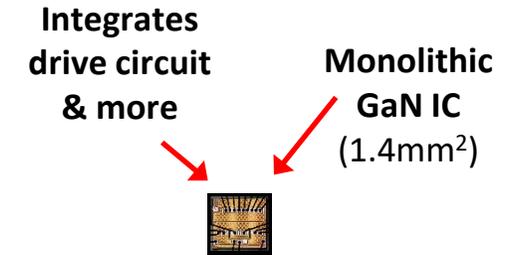
- Extra Si FET + other
 - Cost & complexity
 - Adds parasitics & delay
 - Limits speed & efficiency

Discrete eMode GaN



- Extra Si driver circuit

Navitas eMode GaN IC



- No extra circuits
- No parasitics & delay
- Drive & power matched in GaN
- Integrated features, functions
- Highest speed & efficiency
- Highest robustness and reliability
- Simple customer design
- 50-80% smaller chip

(1) 'dMode' = depletion mode = 'normally on' transistor, causes short circuit unless additional transistor added.

(2) 'eMode' = enhancement mode = 'normally off' transistor.

- GaN is the next generation power semiconductor that offers superior performance.
- GaN power devices require monolithic integration of driver and power stage to enable highest frequency, performance, and reliability.
- Further integration of real time protection and features delivers highest efficiency, performance, and reliability.



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2022

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