The 29th International Symposium on Power Semiconductor Devices and ICs
ISPSD 2017
May 28 -June 1, 2017
Sapporo, Japan
Conference site: Royton Sapporo

Navitas

Power Accelerated

GaN Power IC Technology

Past, Present, and Future

The 29th International Symposium on Power Semiconductor Devices and ICs
Plenary Session

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May 29, 2017

GaN Power IC Technology

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- Why GaN on Silicon?
- GaN IC Development History
- Navitas AllGaN™ Power ICs
- Application examples
- Future directions
- Summary

GaN Power IC Technology

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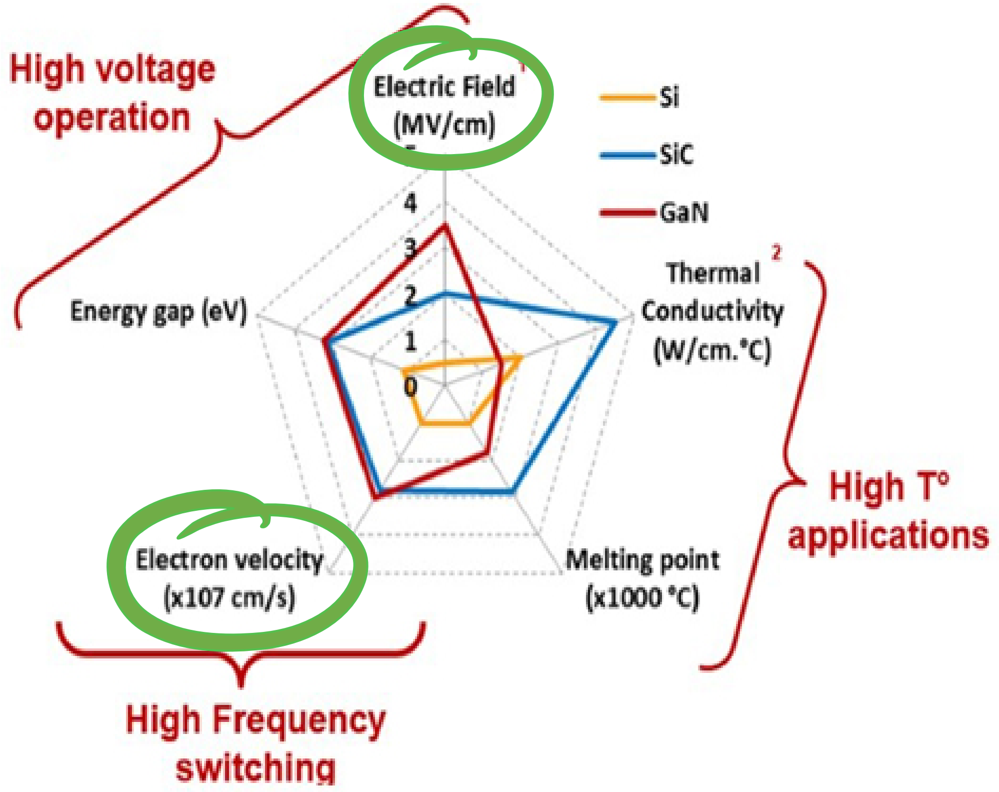
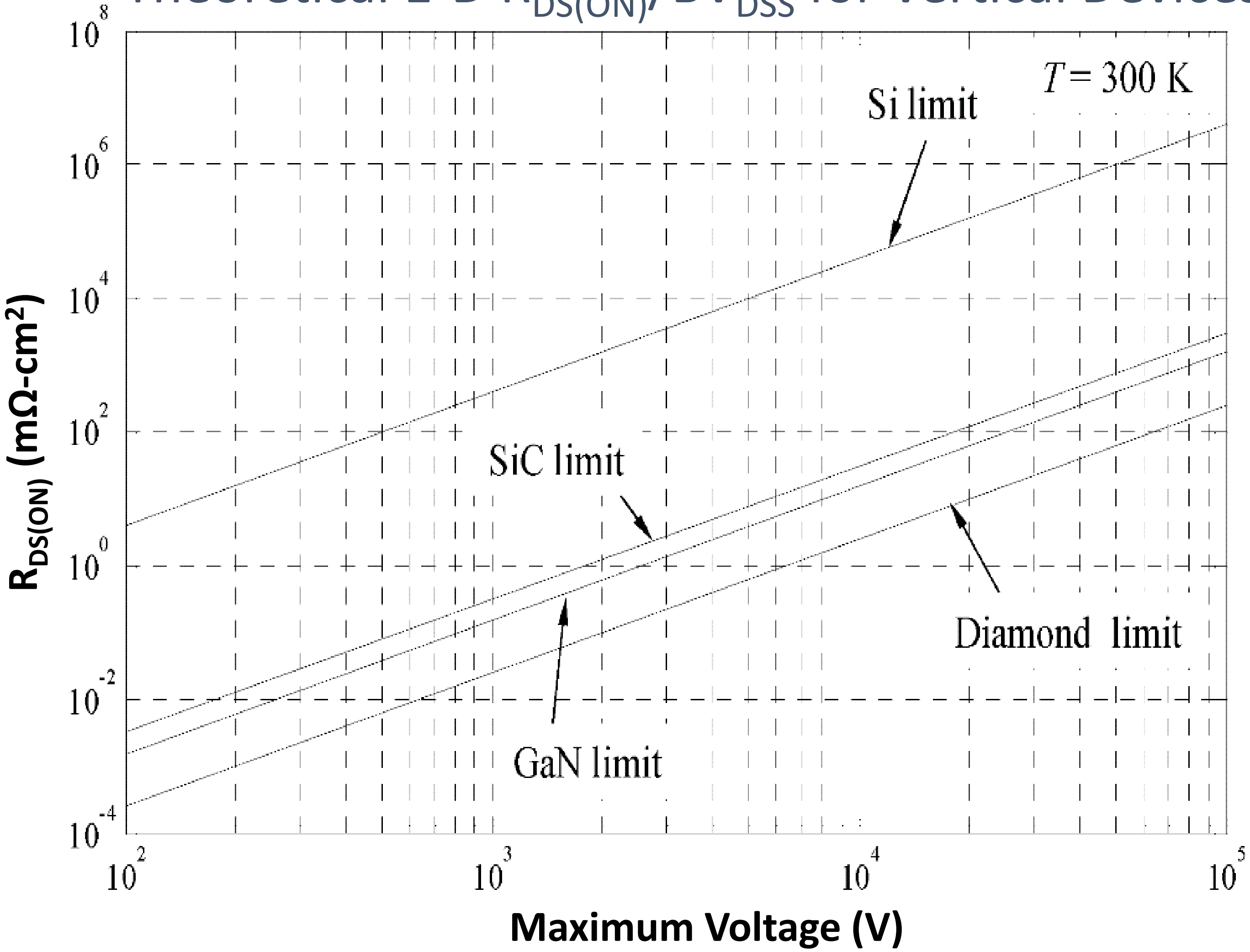
Performance Limits of Power Semi Materials

Important material attributes



Theoretical 1-D $R_{DS(ON)}/BV_{DSS}$ for Vertical Devices



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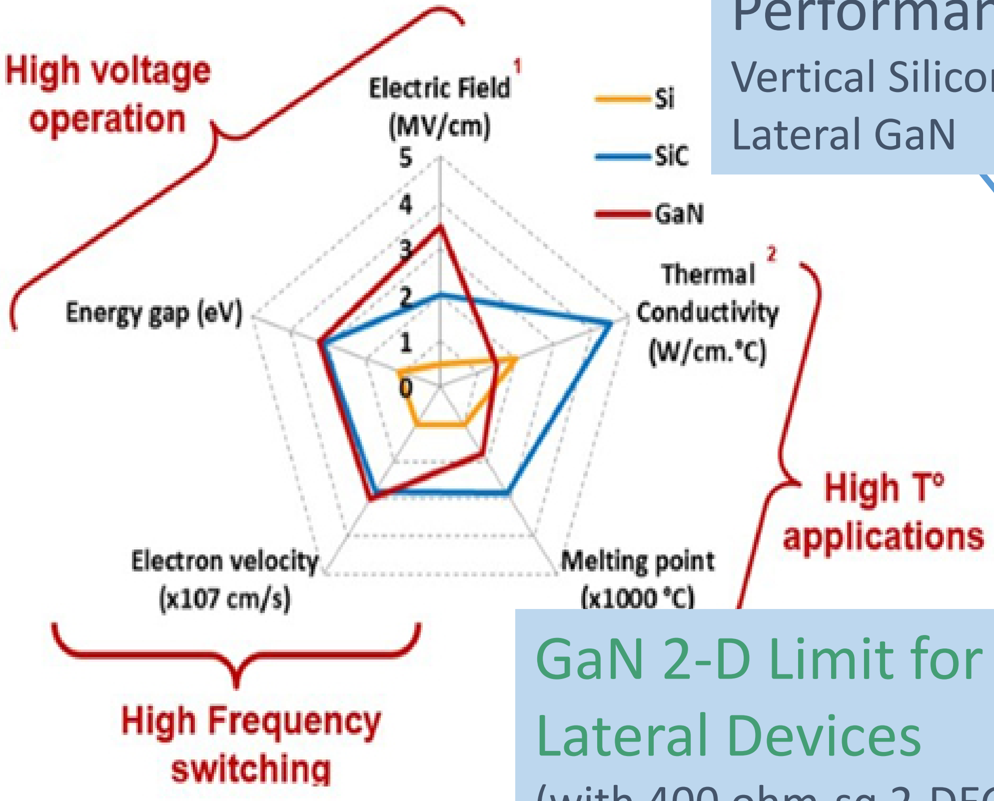


Current Performance

Vertical Silicon

Lateral GaN

GaN 2-D Limit for Lateral Devices

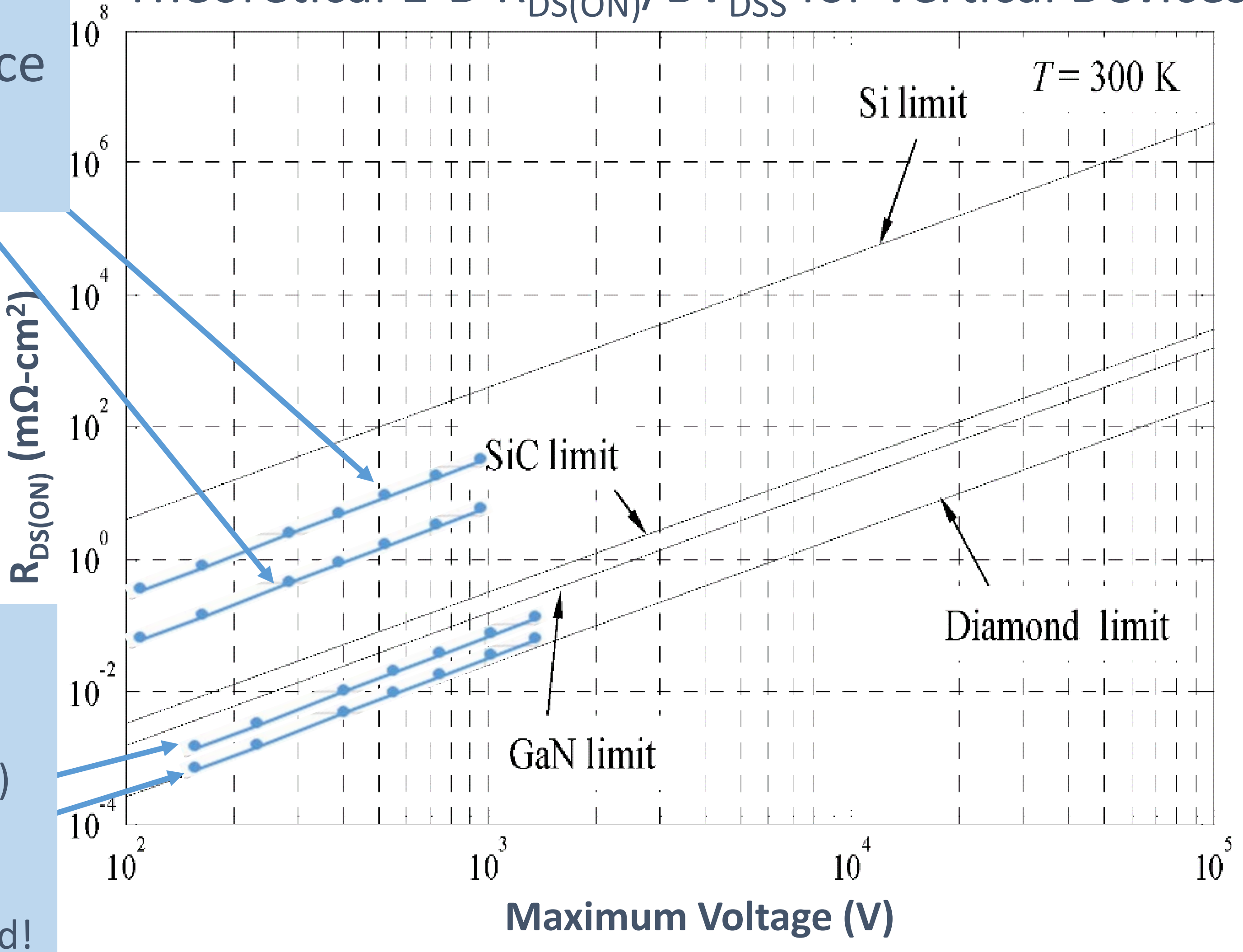
(with 400 ohm-sq 2-DEG)

2.5 MV/cm

3.5 MV/cm

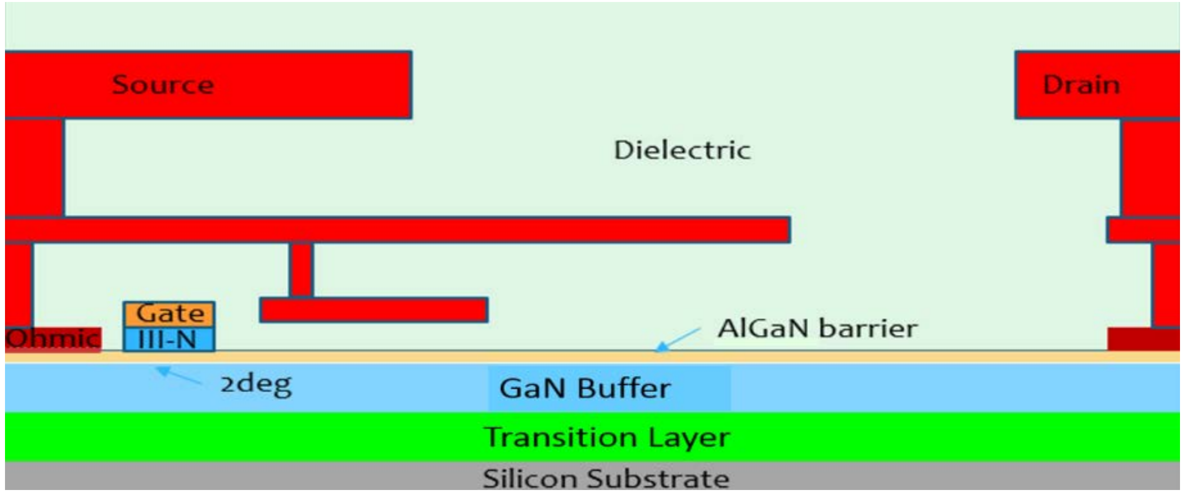
Almost matches Diamond!

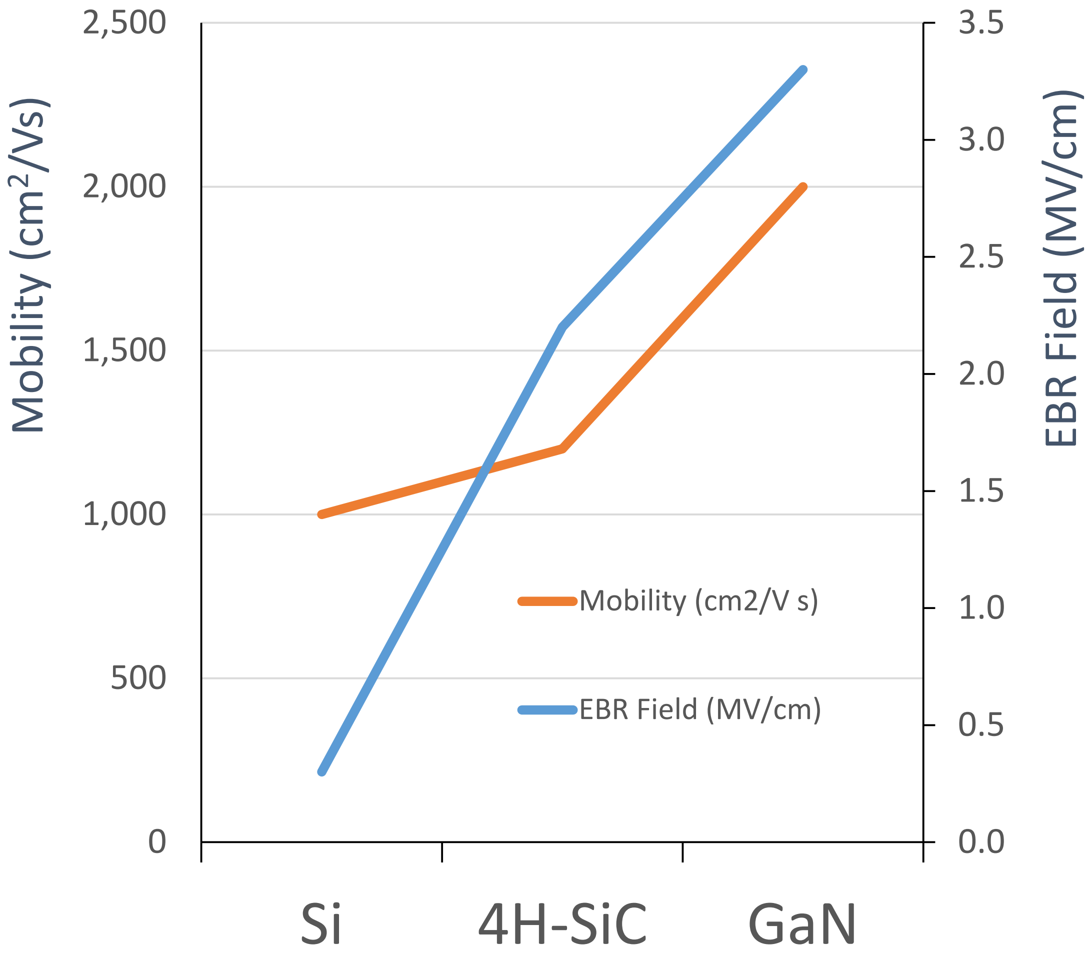
Theoretical 1-D $R_{DS(ON)}/BV_{DSS}$ for Vertical Devices



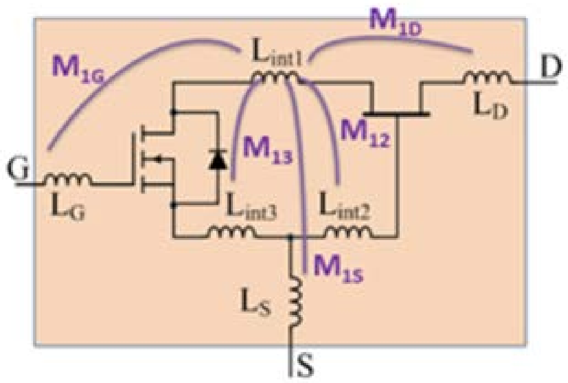
Lateral GaN Advantage for Off-line Applications

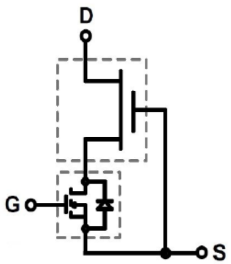
- WBG GaN material allows high electric fields so high carrier density can be achieved
- Two-dimensional electron gas with AlGaN/GaN heteroepitaxy structure gives very high mobility in the channel and drain drift region
- Lateral device structure achieves extremely low Q_g and Q_{OSS} and allows integration
- Integration on silicon substrates means mature low cost wafer fabrication is available



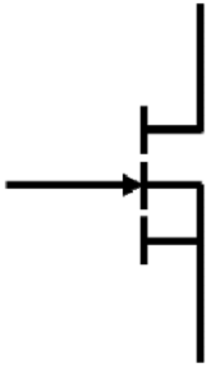


Comparison of Different GaN Technologies





TO-220 Package



- Cascode GaN Switch
  - Relatively easy to control gate
  - Traditional packages
  - Large package inductance
  - Prone to oscillation
  - No dV/dt control
  - Complicated multi-die package

- E-mode GaN Switch
  - Extremely low gate charge
  - No reverse recovery loss
  - Easy to package
  - Low package inductance
  - Can control dV/dt
  - Hard to control gate

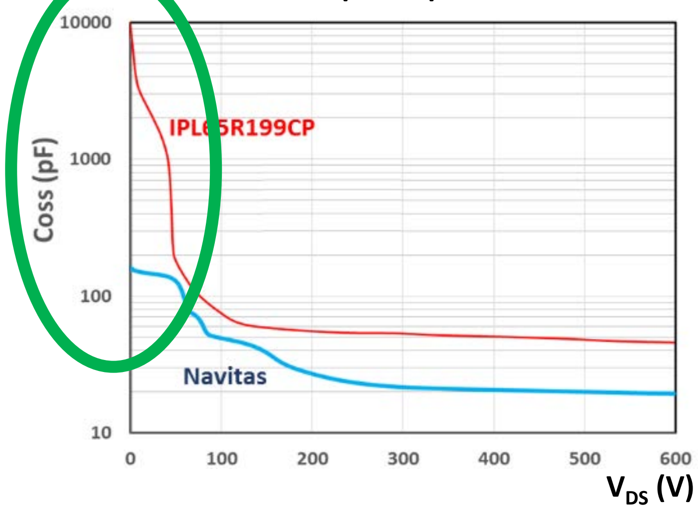
GaN vs Silicon Output Characteristics

- Switching loss:
  $P_{LOSS} = E_{OSS}(V_{DS}) * F_{SW}$
- C_{OSS} → Delay (limits F_{SW})
- Too slow → partial ZVS → **E_{OSS} loss**

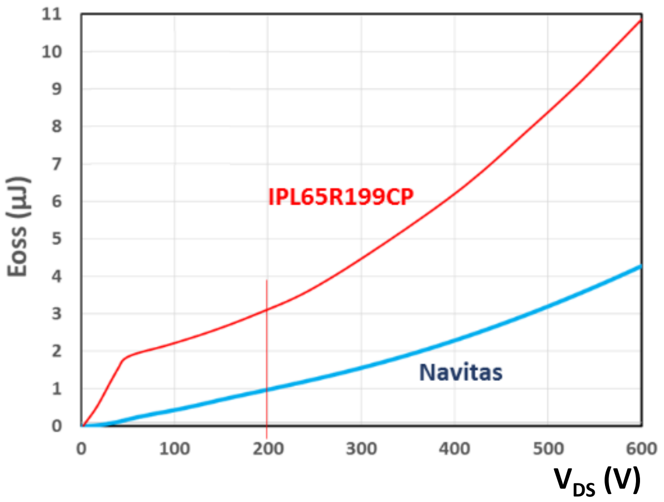
- Si C_{OSS} is 50x-100x higher than GaN at $V_{DS} < 30V$
- Si P_{LOSS} is 3x higher than GaN at 200V (partial ZVS)
- Big effect at full or light load condition

- Further information: "C_{OSS} Hysteresis in Advanced Superjunction MOSFETs", Harrison, APEC 2016

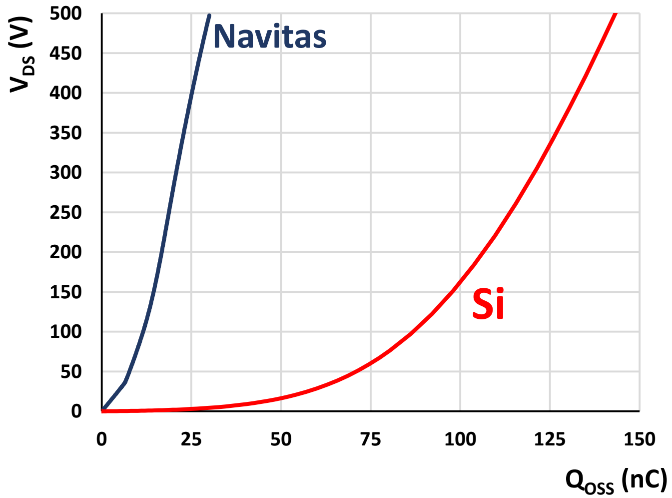
Output Capacitance



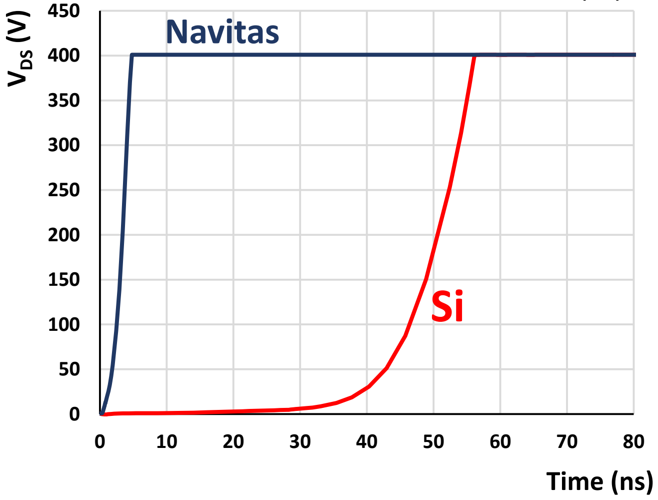
Energy Loss



Output Capacitance Charge (normalized per $R_{DS(ON)}$)



Switching Delay (Inductive Load, normalized per $R_{DS(ON)}$)



Hard-Switch → Soft-Switch with GaN Power IC

Primary Switch Power Loss:

Minimized Minimized

$$P_{FET} = P_{COND} * k + P_{DIODE} + P_{T\text{-}ON} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

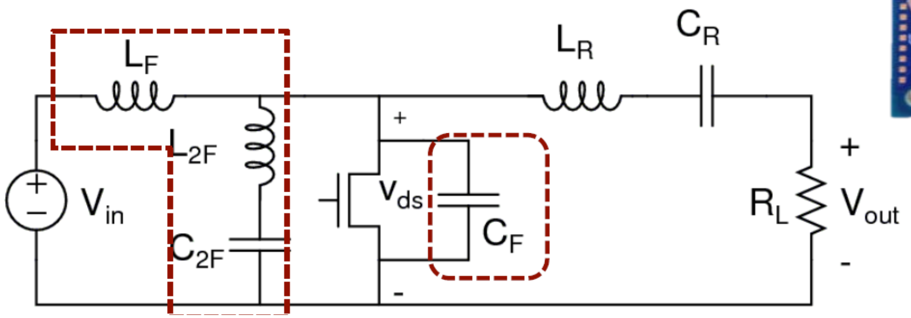
- k-factor >1 due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓10x 2-3x (GaN C_{OSS} charging/discharging loss negligible up to 2MHz)
- P_{DRIVER} ↓10x (GaN P_{DR} negligible up to 2MHz)
- P_{QRR} = 0
- P_{DIODE} ↓3x 2x (synchronous rectification with improved dead-time control)
- $P_{T\text{-}OFF}$ = 0 Reduced (near-zero drive loop impedance with integration)

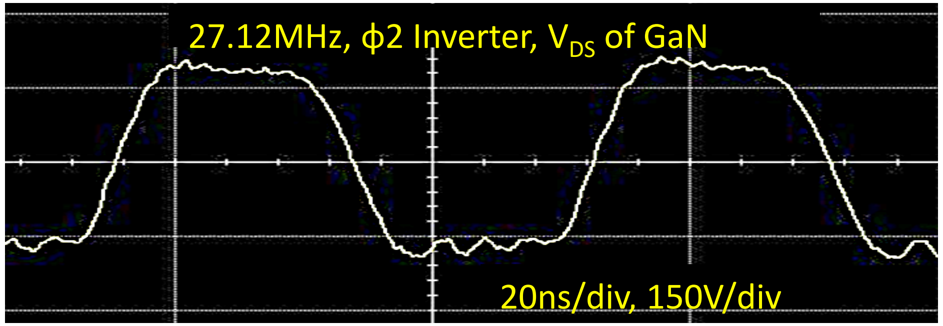
>10x frequency increase possible with higher efficiencies

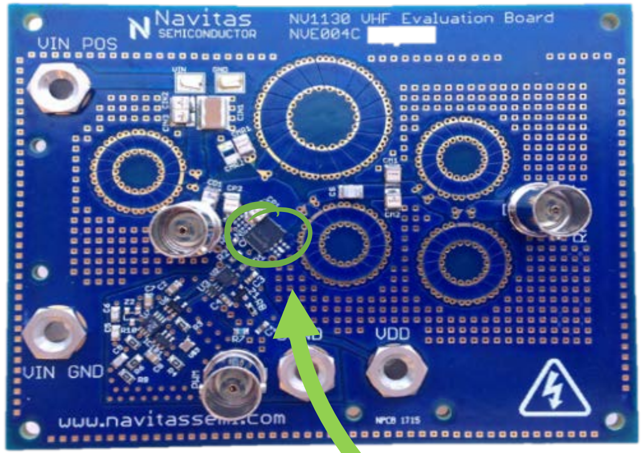
27 MHz, 40 MHz…

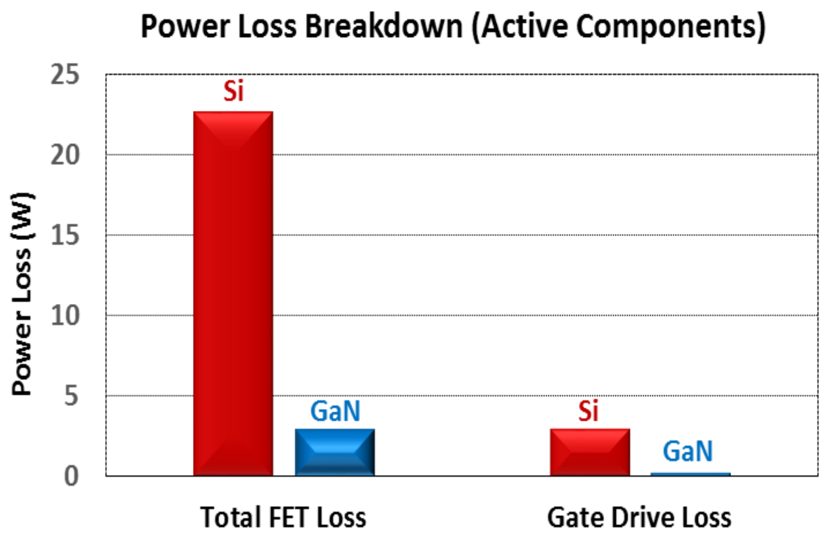
Class Phi-2 DC/AC converter

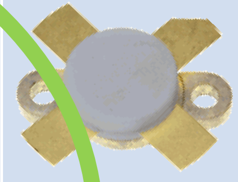
- 50% less loss than RF Si
- 16x smaller package
- Air-core inductors
- Minimal FET loss
- Negligible gate drive loss









Technology	V	Pack (mm)		F_{SW} (MHz)	Eff. (%)	Power (W)
RF Si (ARF521) Microsemi POWER PRODUCTS GROUP	500	M174 22x22		27.12	91%	150
Navitas	650	QFN 5x6		27.12	96%	150
				40.00	93%	115

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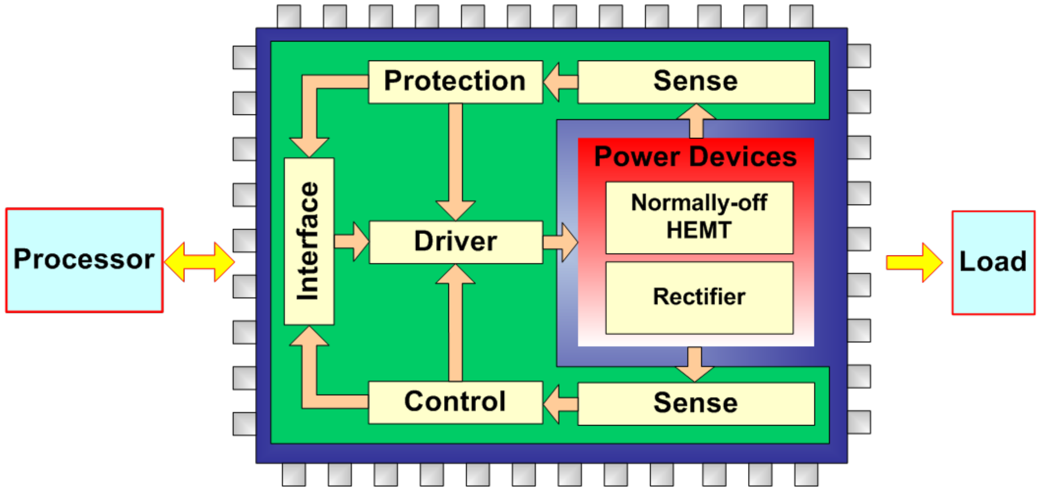
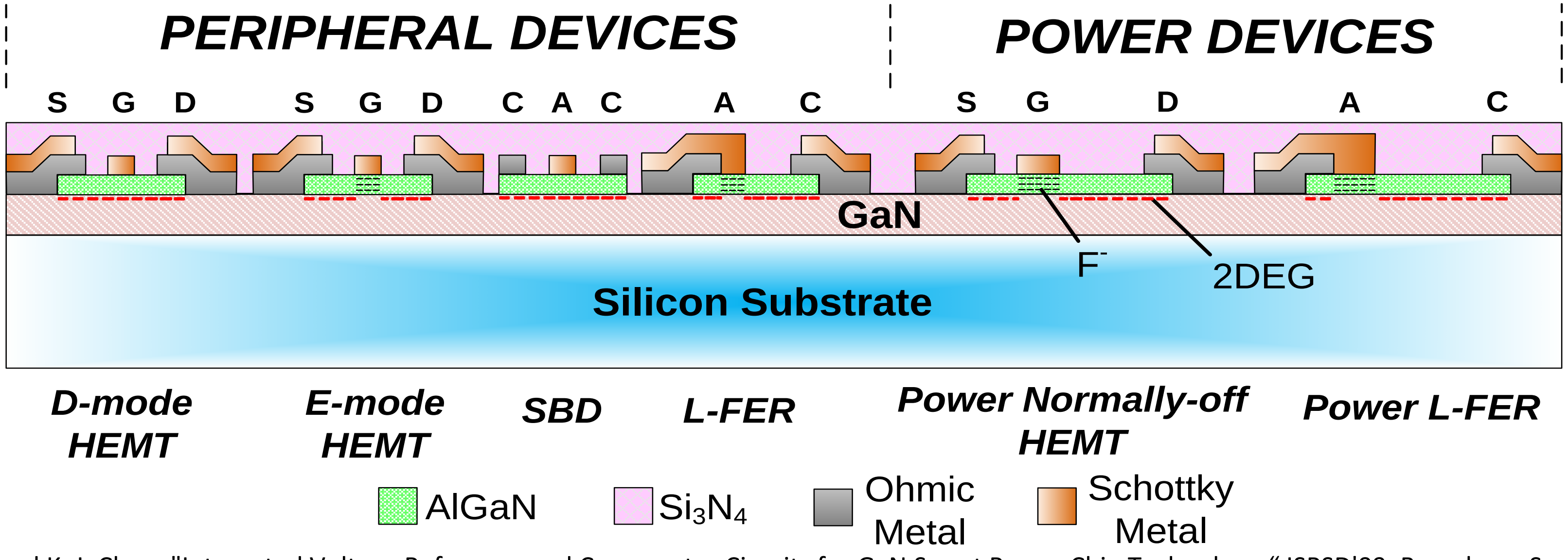
Early years of GaN Power IC Technology

- Concept of GaN power ICs developed as potential of GaN for power widely explored
- Ideal device has simple digital I/O, and all necessary functions to manage a load, such as gate drive, sensing, protection, & control
- Integrated dMode & eMode small signal HEMT, Schottky, Power HEMT, and power rectifier were proposed and demonstrated
- Threshold shift into positive range used F- implant, with some stability issues

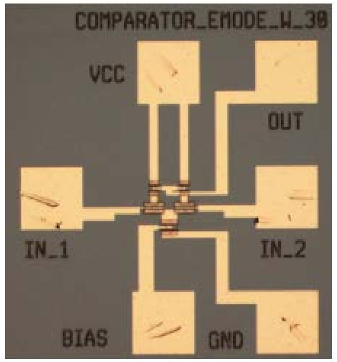


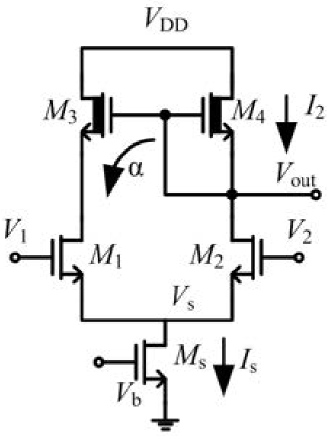


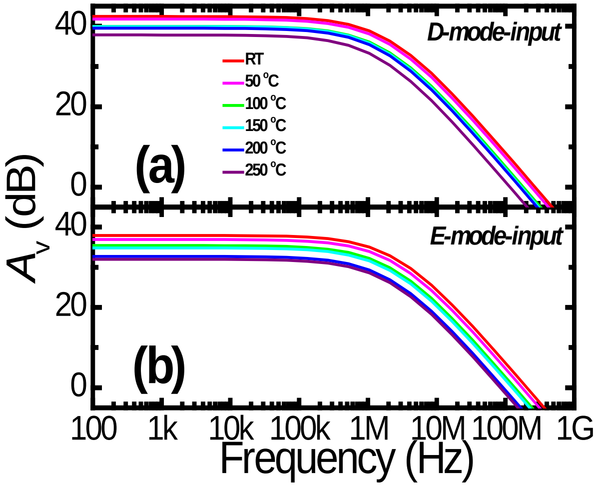
K. Y. Wong, W. J. Chen, and K. J. Chen, "Integrated Voltage Reference and Comparator Circuits for GaN Smart Power Chip Technology," ISPSD'09, Barcelona, Spain, June 14-17, 2009

Developing Fundamental Analog Blocks in GaN

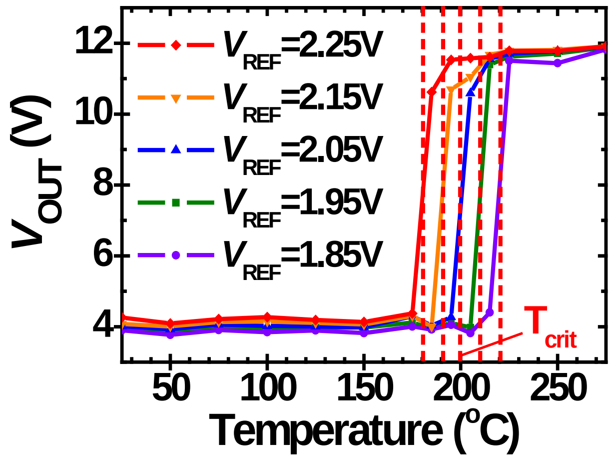
- Since then, a variety of circuit blocks and functions have been reported:
- Comparator, with both eMode and dMode input pairs
- Temperature sensors and references
- Integrated controller functions such as sawtooth generator and PWM comparator



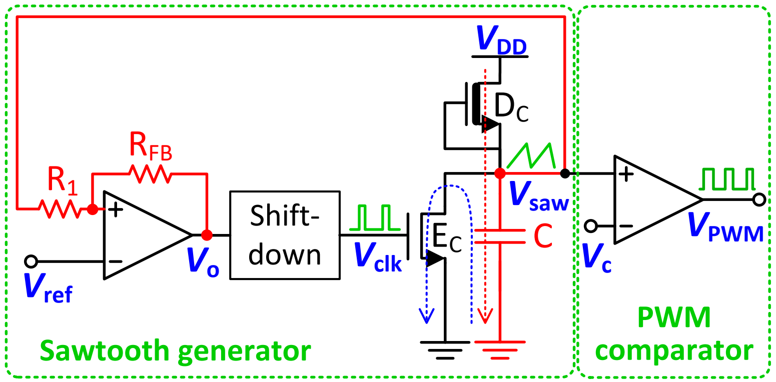




X. Liu and K. J. Chen, "GaN Single-Polarity Power Supply Bootstrapped Comparator for High Temperature Electronics," IEEE Electron Device Letters, vol. 32, No. 1, pp. 27-29, Jan. 2011



A. M. H. Kwan, Y. Guan, X. Liu, and K. J. Chen, "Integrated over-temperature protection circuit for GaN smart power ICs," Jpn. J. Appl. Phys., 52, 08JN15, 2013



H. Wang, A. M. H. Kwan, Q. Jiang, and K. J. Chen, "A GaN Pulse Width Modulation Integrated Circuit," ISPSD2014, Waikoloa, Hawaii, USA, June 15-19, 2014

Multiple Power Devices on Chip

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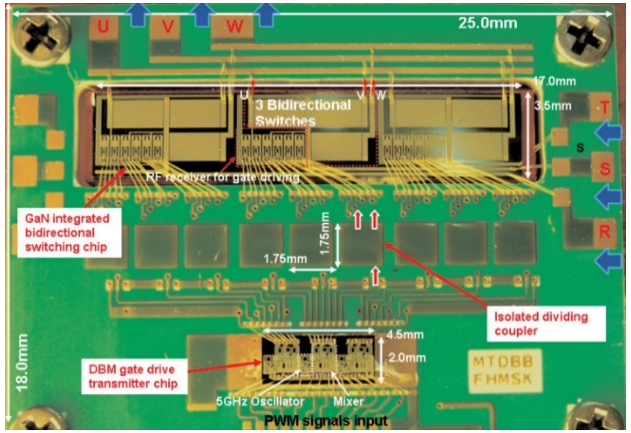
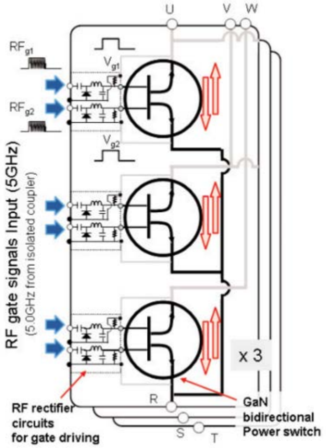
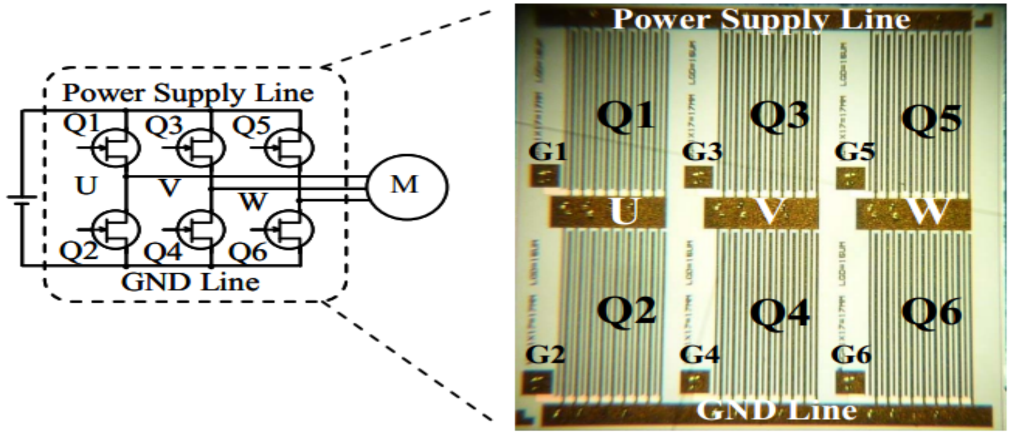
- One reported 3-phase inverter intended for medium voltage motor driver
- A novel integration of 9 bidirectional switches in AC/AC 3-phase to 3 phase matrix converter
  - Gate drive function is by eighteen rectifier circuits that receive 5 Ghz pulse trains during Intended on periods
- A low voltage assymetric synchronous buck circuit for point-of-load converter
  - An early demonstration of an integrated output buffer stage to provide a gate drive output buffer function

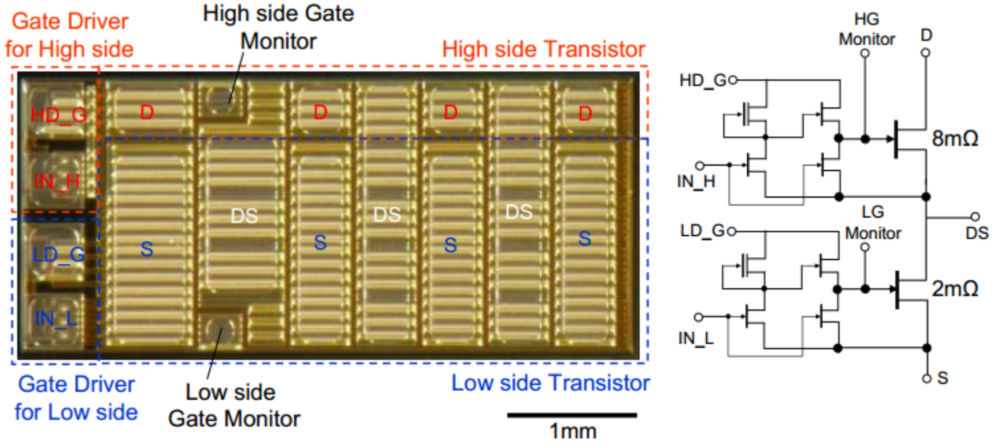




S. Nagai, Y. Yamada, N. Negoro, H. Handa, Y. Kudoh, H. Ueno, M. Ishida, N. Otuska, D. Ueda, "A GaN 3×3 Matrix Converter Chipset with Drive-by-Microwave Technologies, Intl. Solid State Circuits Conf. 2014



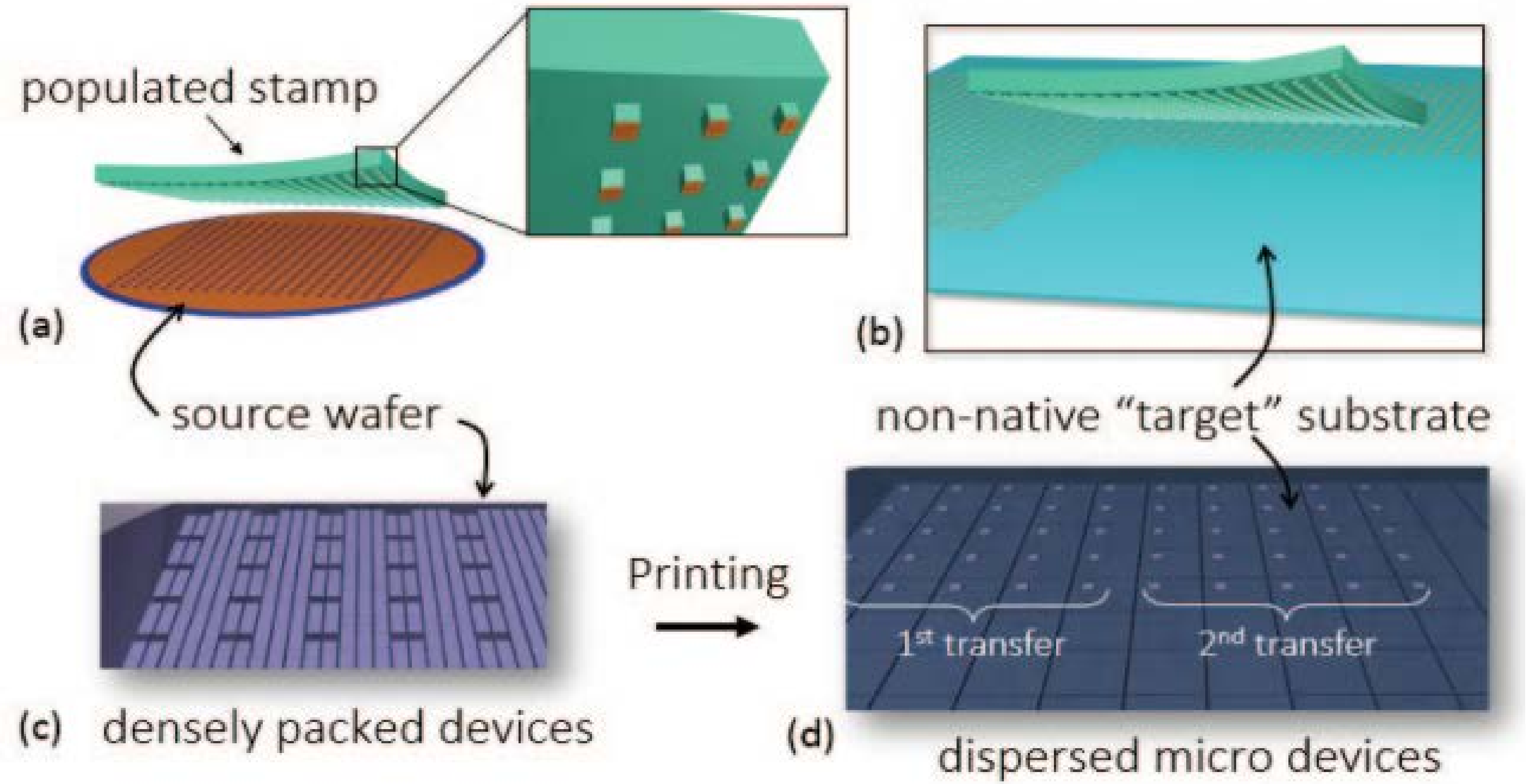
Y. Uemoto, T. Morita, A. Ikoshi, H. Umeda, H. Matsuo, J. Shimizu, M. Hikita, M. Yanagihara, T. Ueda, T. Tanaka, D. Ueda, "GaN Monolithic Inverter IC Using Mormallu-off Gate Injection Transistors with Planar Isolation on Si Substrate," 2009 IEDM, Dec 2009



S. Ujita, Y. Kinoshita, H. Umeda, T. Morita, S. Tamura, M. Ishida, T. Ueda, "A Compact GaN-based DC-DC Converter IC with High-Speed Gate Drivers Enabling High Efficiencies," ISPSD2014, Waikoloa, Hawaii, USA, June 15-19, 2014

Hybrid Integration: Chip-on-Chip Bonding

- An alternative to full monolithic power IC integration:
- Select GaN transistors from a source wafer to provide high voltage and/or high frequency capability
- Using a designed stamp, pick the devices on an interval that matches the size of the target IC.
- Transfer and release to form the power GaN on CMOS chip on chip

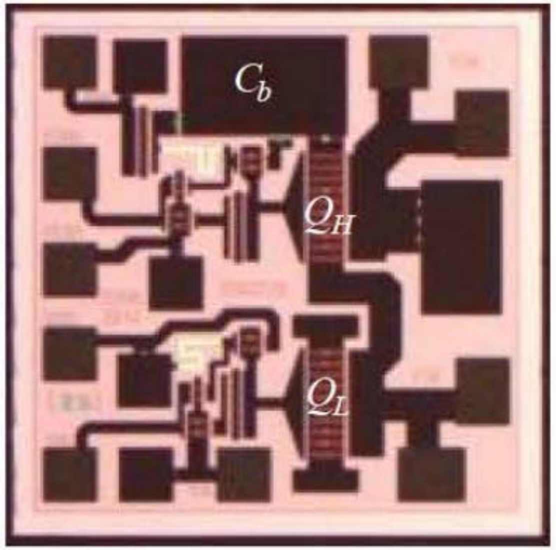


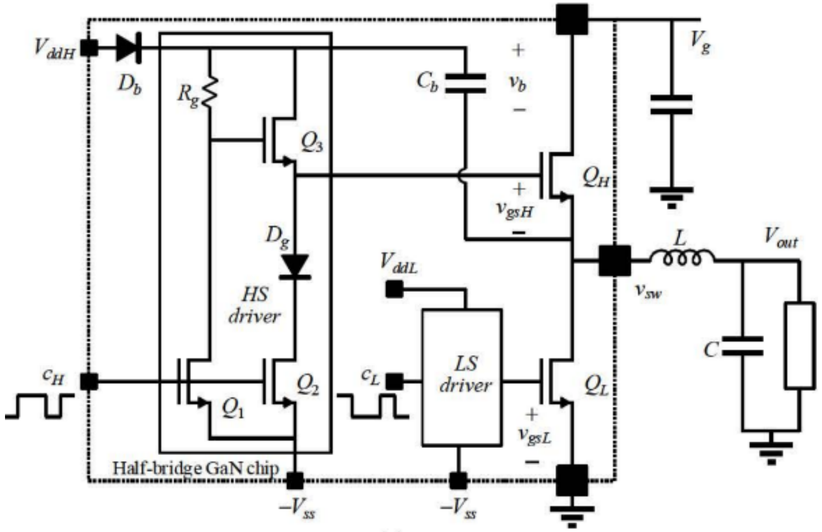
R. Lerner, S. Eisenbrandt, C. Bower, S. Bonafede, A. Fecioru, R. Reiner, P. Waltereit, " Integration of GaNHEMTs onto Silicon CMOS by Micro Transfer Printing," ISPSD2016, Prague, Czech Republic, May, 2016

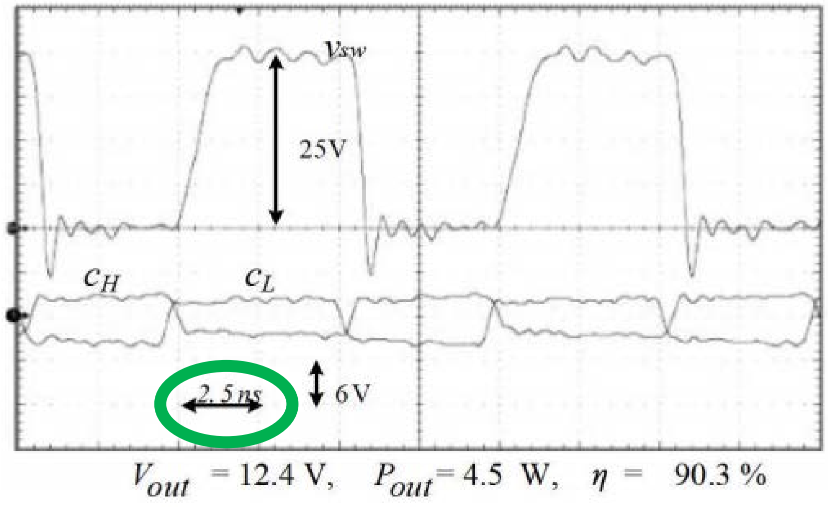
Pushing GaN Power IC Technology >100 MHz

- This monolithic GaN buck converter example is showing operation with near 90% total efficiency up to 100Mhz and 45V input.
- At these frequencies, high Q RF compatible air core magnetics and low ESR ceramic capacitors are essential

Switching frequency, f_s [MHz]	20	50	100	200	400	100
Input voltage [V]	25	25	25	25	20	45
Maximum output power [W]	16.0	10.1	7.1	3.4	5.0	6.0
Peak power stage efficiency [%]	95.0	94.2	93.2	86.5	72.5	91.7
Peak total efficiency [%]	92.5	91.7	89.2	82.0	67.0	90.2
Inductance (L) [nH]	160	90	47	22	12.5	90
Duty cycle (D) [%]	75	75	75	75	50	50



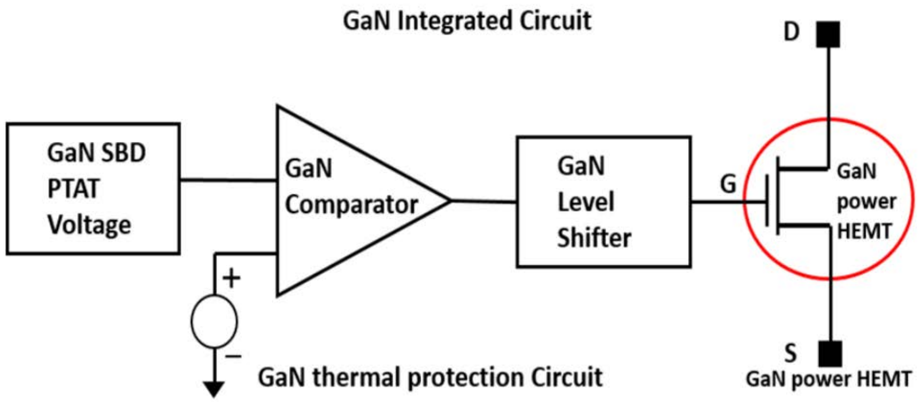


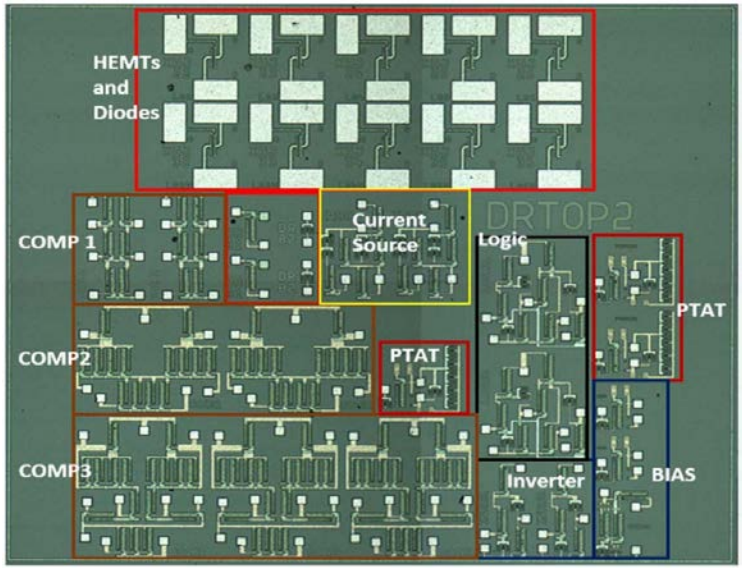


Alihossein Sepahvand, Yuanzhe Zhang, Dragan Maksimovic, "High Efficiency 20-400 MHz PWM Converters using Air-Core Inductors and Monolithic Power Stages in a Normally-Off GaN Process," APEC 2016 March 21, 2016, Long Beach, Ca. USA

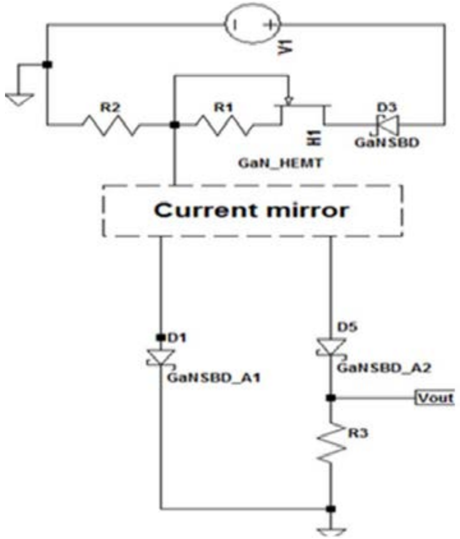
Recent Cell Library Development and Application

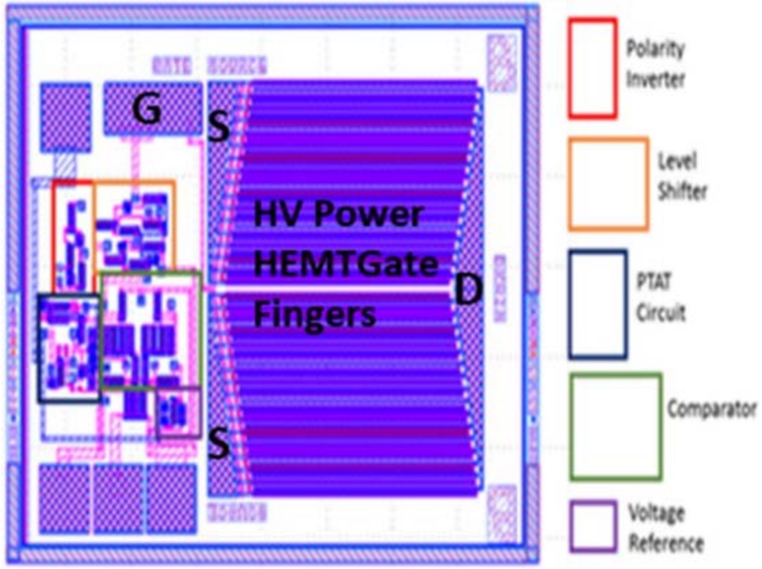
- A cell library includes current sources, comparators, bias and logic circuity, a PTAT generator, and a reference
- All of this is integrated in the example to provide a high voltage GaN single transistor Power IC with thermal protection





PTAT Voltage Generator

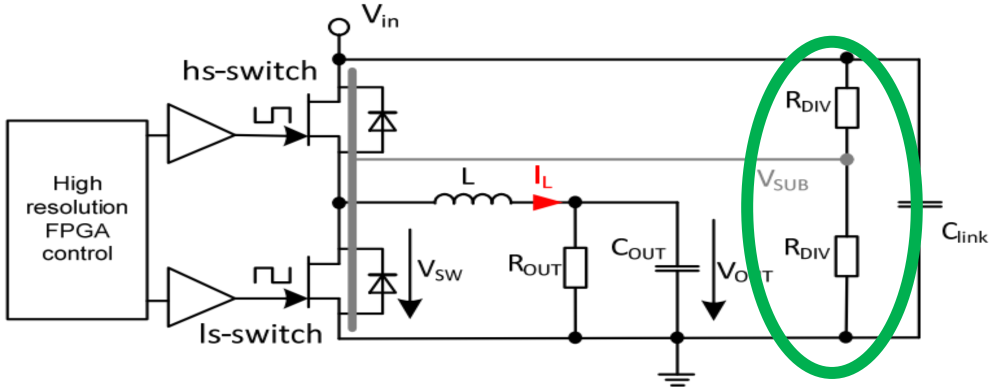


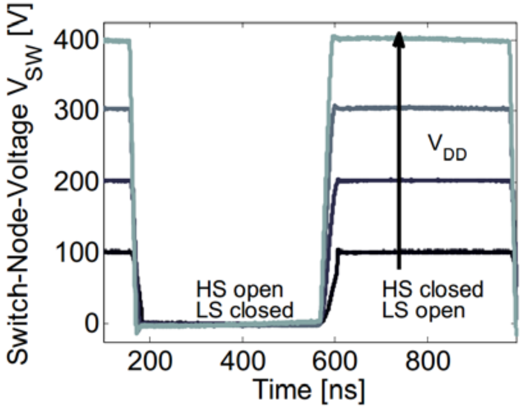


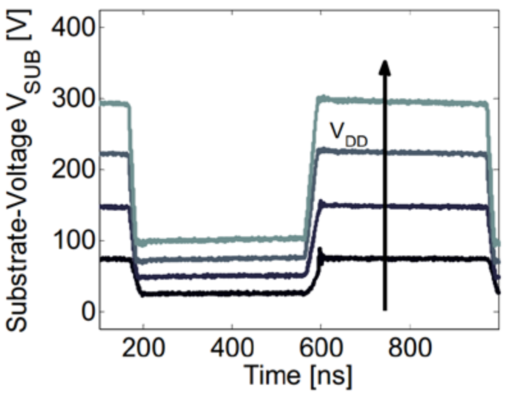
Dilip Risbud, Kenneth Pedrotti, "Analog and digital cell library in High Voltage GaN-on-Si Schottky Power Semiconductor Technology," WiPDA, Nov. 7-9, 2016 Fayetteville, Ar, USA

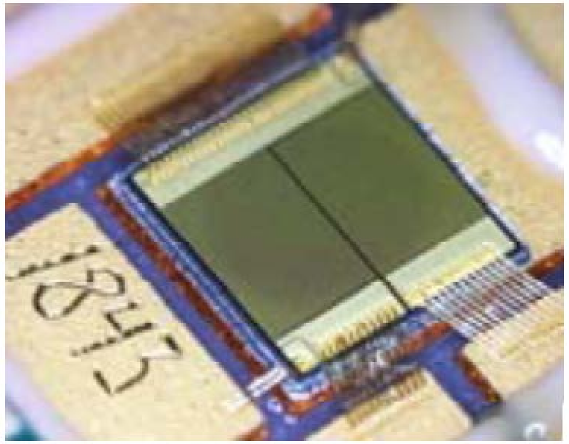
A Demonstration of Half Bridge Integration

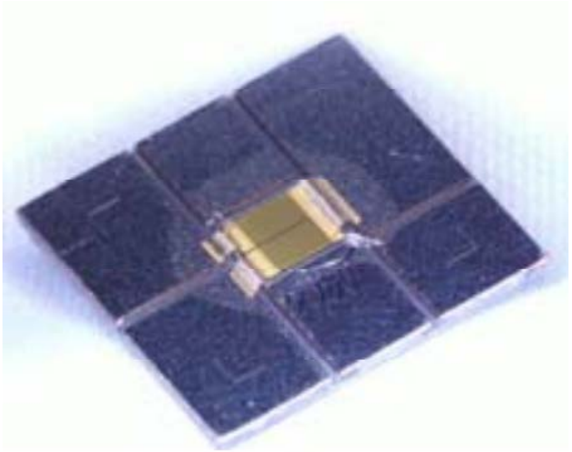
- In order to suppress current collapse, the chip substrate is connected to a passive network formed by the R_{DIV} divider and the chip capacitance that causes it to closely follow the switch node.

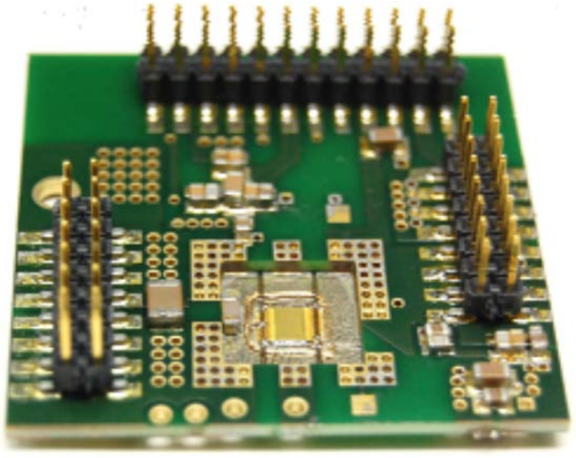












B. Weiss, R. Reiner, P. Waltereit, R. Quay, O.Ambacher, A. Sepahvand, D. Maksimovic, "Soft-Switching 3MHz Converter based on Monolithically Integrated Half-Bridge GaN-Chip," WiPDA, Nov 7-9, 2016, Fayetteville, Ar, USA

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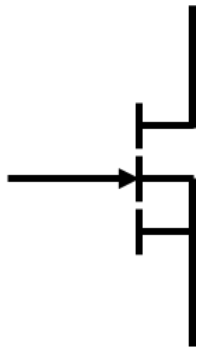
Navitas AllGaN™ Power ICs

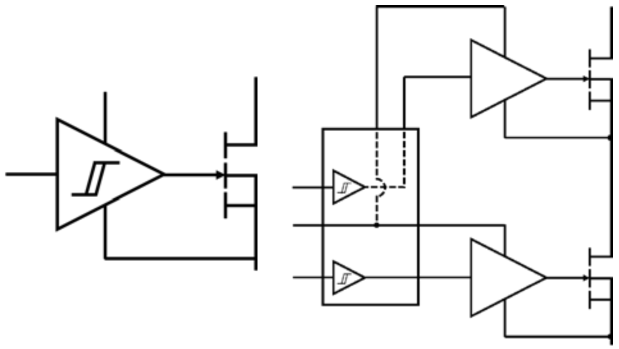
Fastest, most efficient GaN Power FETs



>20x faster than silicon
>5x faster than cascoded GaN
Proprietary design

+

iDrive First & Fastest Integrated GaN Gate Drivers



>3x faster than any other gate driver
Proprietary design
30+ patents granted/applied

=

World's First AllGaN™ Power IC

Up to 40MHz switching, 5x higher density & 20% lower system cost

Multiple Discretes → Monolithic Integration

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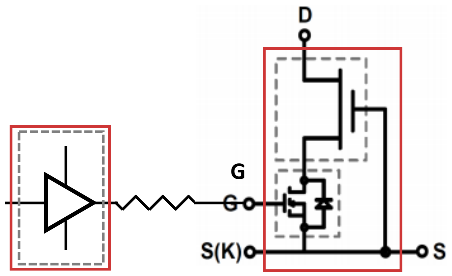
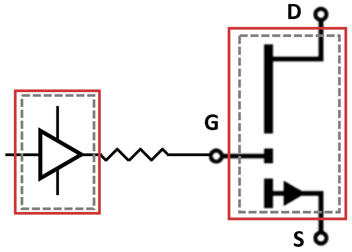
Normally-ON
(dMode)
Co-pack Cascode FET
Discrete, External Driver
Multiple Chips, Two Packages



transphorm

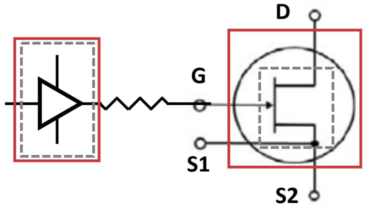
ON Semiconductor

Normally-OFF
(eMode)
Discrete
External Custom Driver
Two Chips, Two Packages



GaN Systems

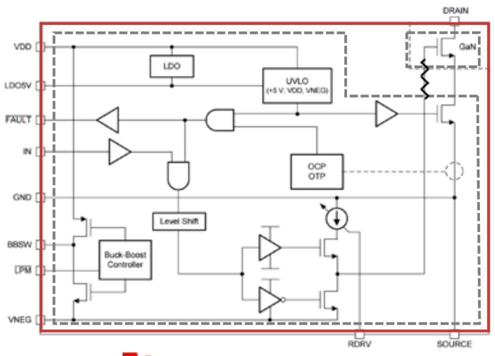
EPC EFFICIENT POWER CONVERSION



Panasonic

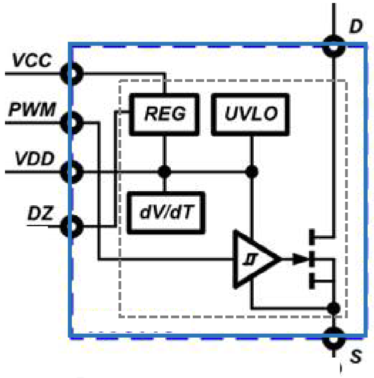
Infineon

Normally-ON
(dMOde)
Co-pack Cascode FET & Driver IC
Charge Pump Negative Rail
Two Die, One Package



Texas Instruments

Normally-OFF
(eMode)
GaN Power IC
1 Die, 1 Package



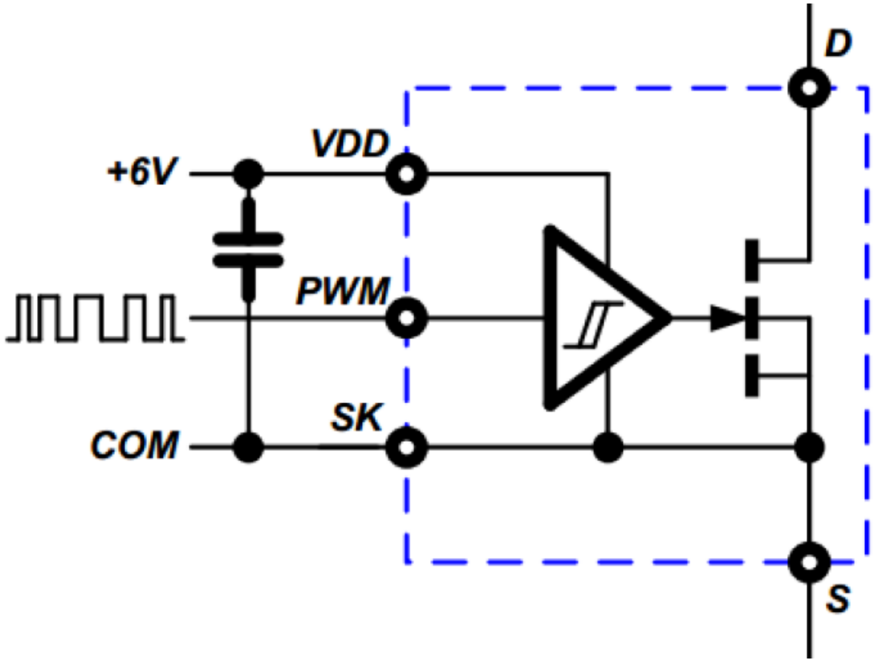
Navitas

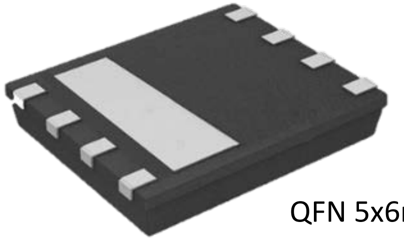
Fast, Easy, Low Cost

Removing Speed Limits:

Navitas GaN Power IC

- **Monolithic** integration
- 10X lower drive loss than silicon
- Driver impedance matched to power device
- Short prop delay (10ns)
- Zero inductance turn-off loop
- Digital input (hysteretic)
- Rail-rail drive output
- Reduces layout sensitivity





QFN 5x6mm

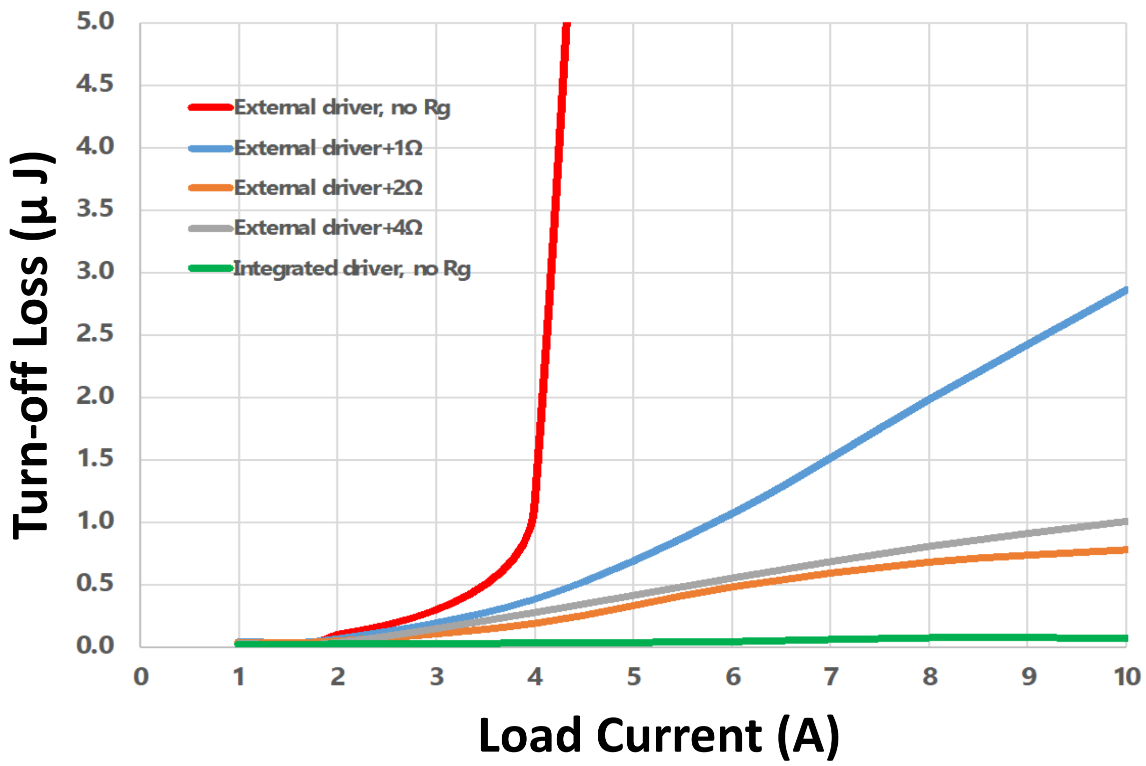
Speed & Integration → Eliminate Turn-off Losses

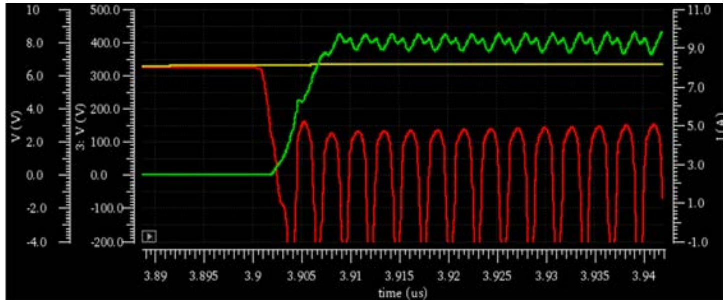
External drivers

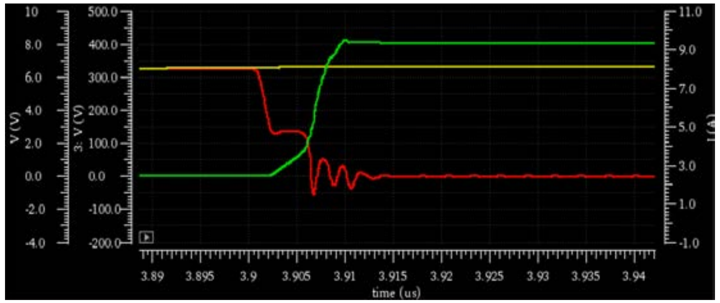
- Just 1-2 nH of gate loop inductance can cause unintended turn-on
- Gate resistors reduce spikes but create additional losses

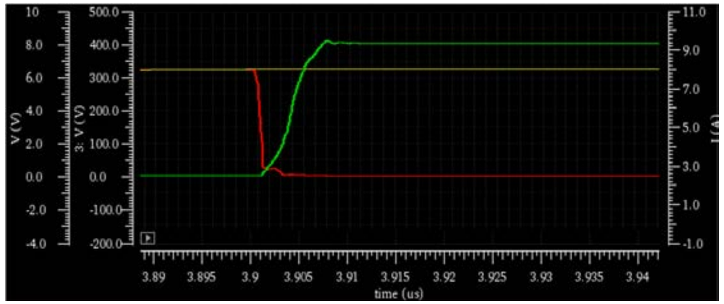
Integrated GaN drivers (iDrive™)

- Eliminate the problem
- Negligible turn-off losses



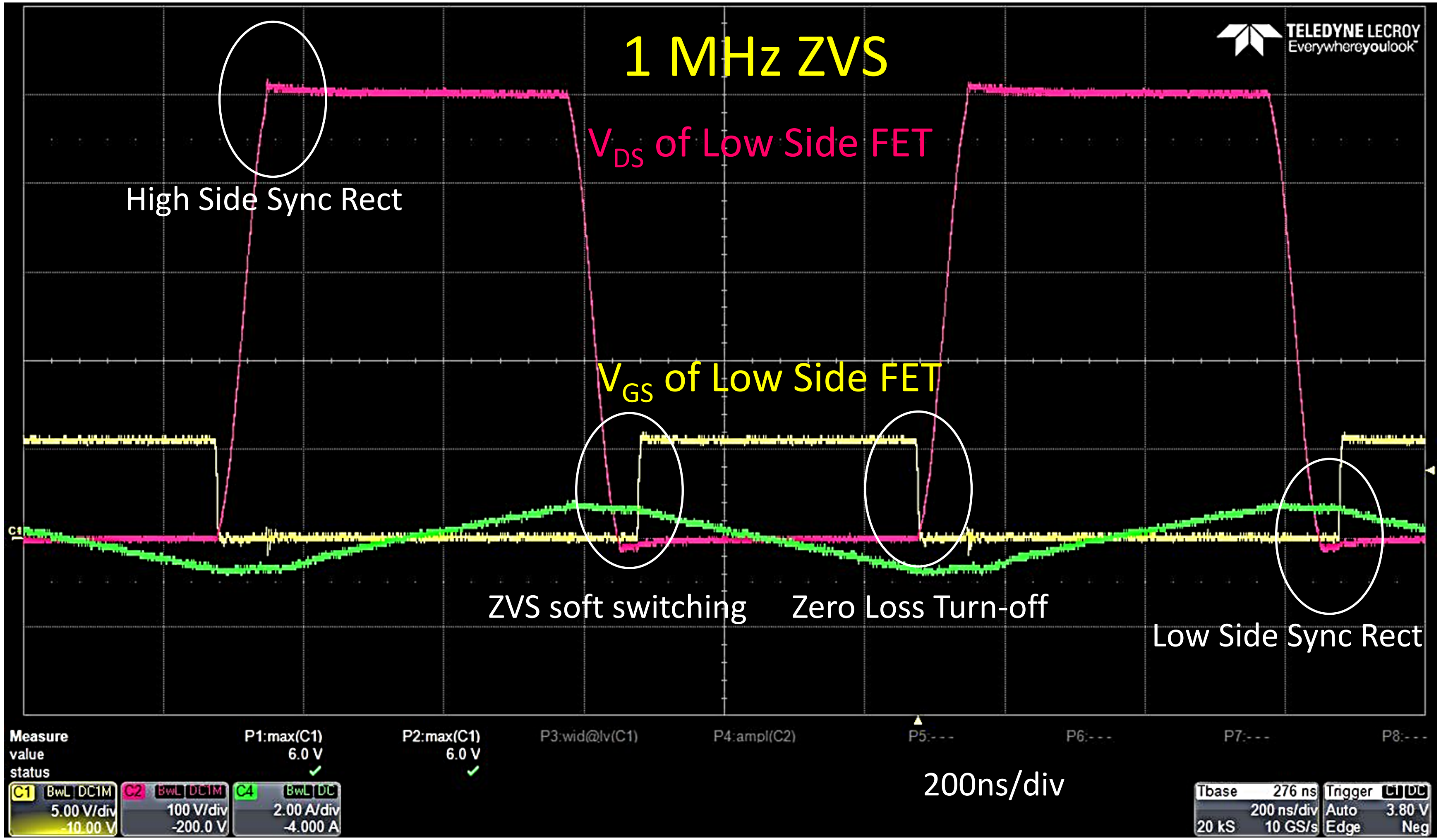






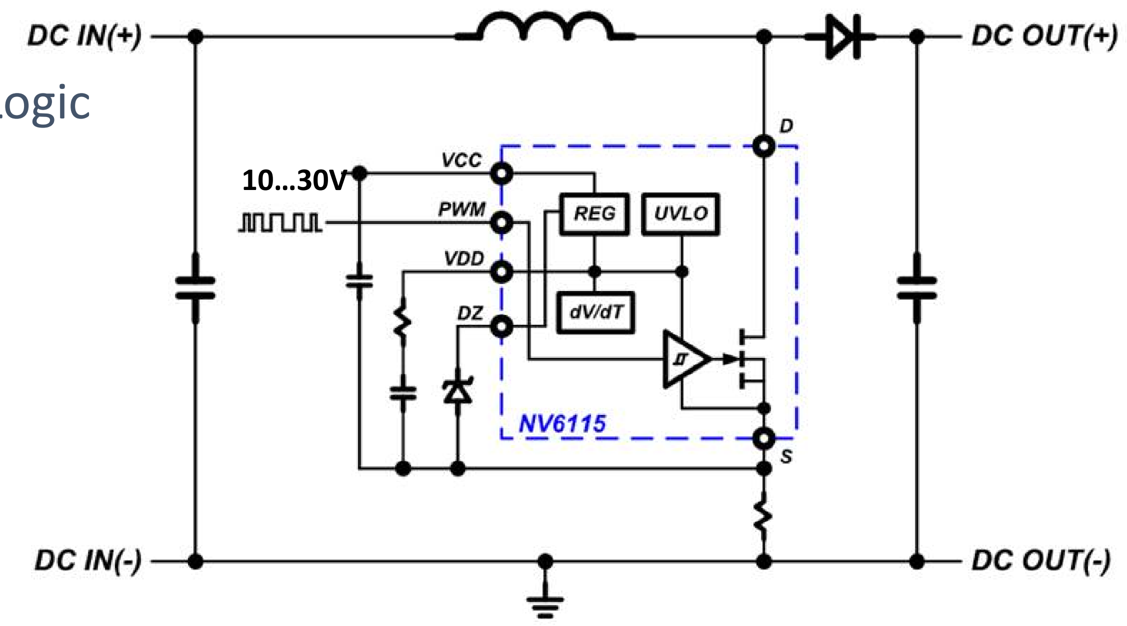
GaN Power IC – *Fast & Efficient*

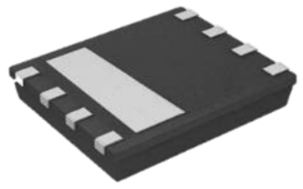
- 500 V Switching
- No overshoot / spike
- No oscillations
- ‘S-curve’ transitions
- Zero Loss Turn-on
- Zero Loss Turn-off
- Sync Rectification
- High frequency
- Small, low cost magnetics



GaN Power IC: High-Speed FET, Drivers & More

- **Monolithic** integration of GaN FET, GaN Driver, GaN Logic
- 650 V eMode power device
- 10x lower drive loss than silicon (<35 mW at 1 MHz)
- Driver impedance matched to power device
- Very fast (prop delay including turn-on/off 10ns)
- Zero inductance turn-off loop
- High dV/dt immunity (200 V/ns)
- Regulated gate voltage
- Controllable turn-on dV/dt
- Digital input

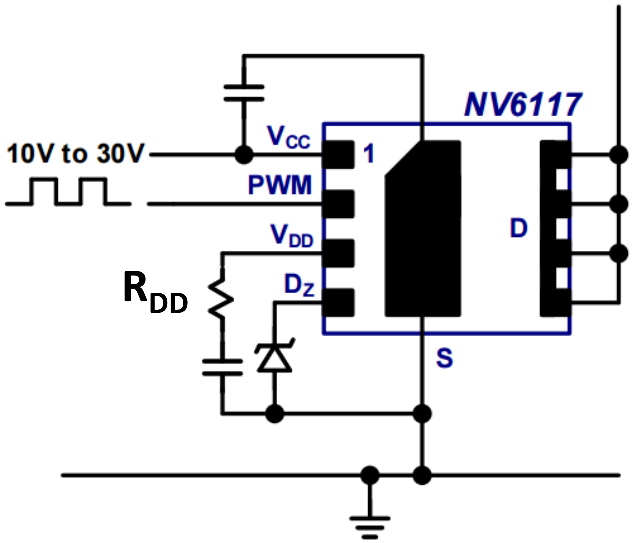


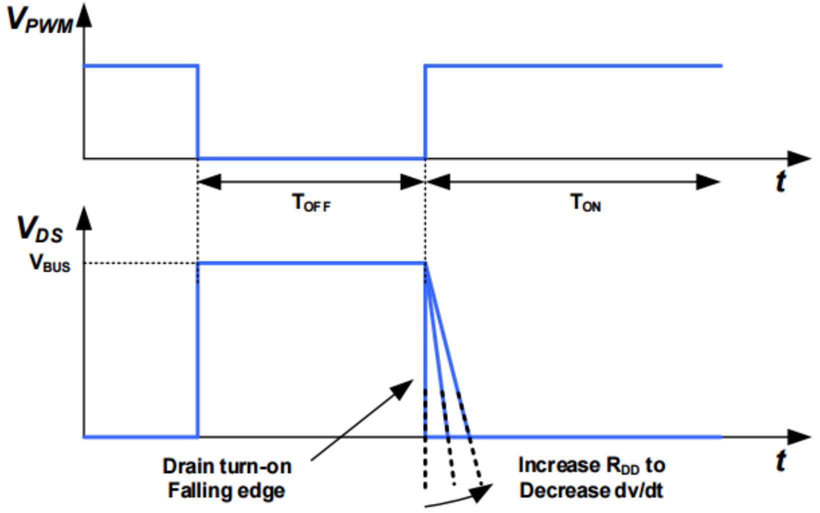


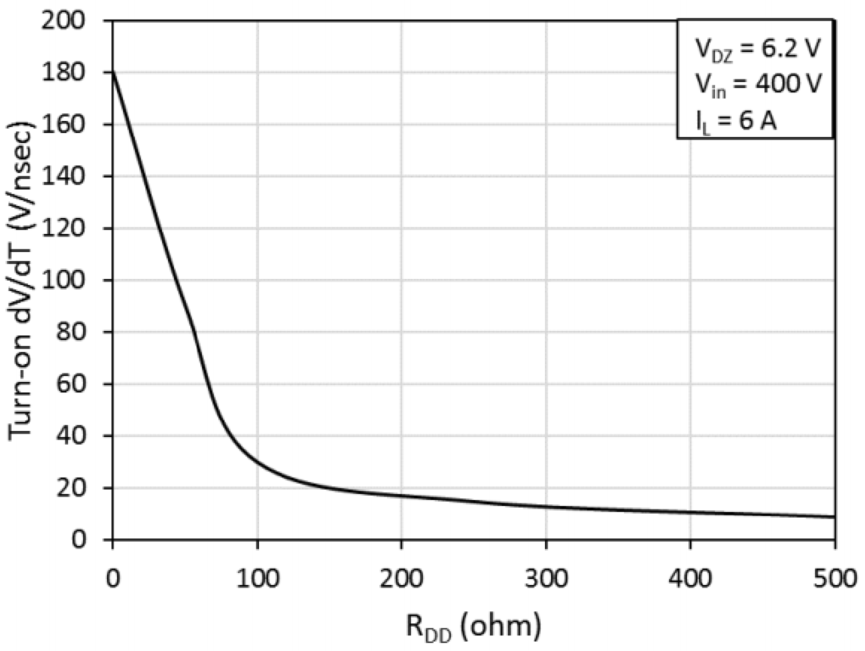
QFN 5x6mm

D. Kinzer, S. Oliver "Monolithic HV GaN Power ICs" in *IEEE PELS Power Electronics Magazine*, vol. 3, no. 3, pp. 14-21, September 2016

GaN Power IC – Voltage Slew Rate Control







- dV/dt controllable from 180 V/ns to 10 V/ns for EMI optimization

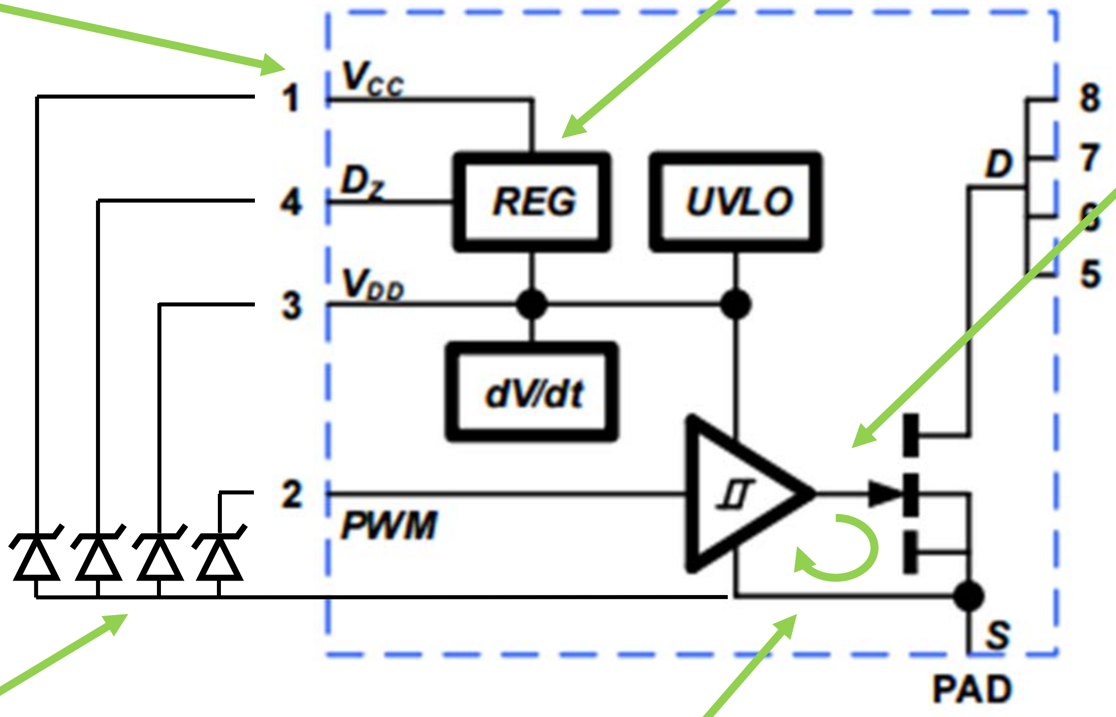
Reliability Benefits of GaN Power IC

Navitas

V_{MAX} on V_{CC} & V_{PWM} pins have 30 V rating

Built-in regulator precisely controls gate voltage applied to eMode gate

Sensitive eMode gate node protected from system noise and spikes



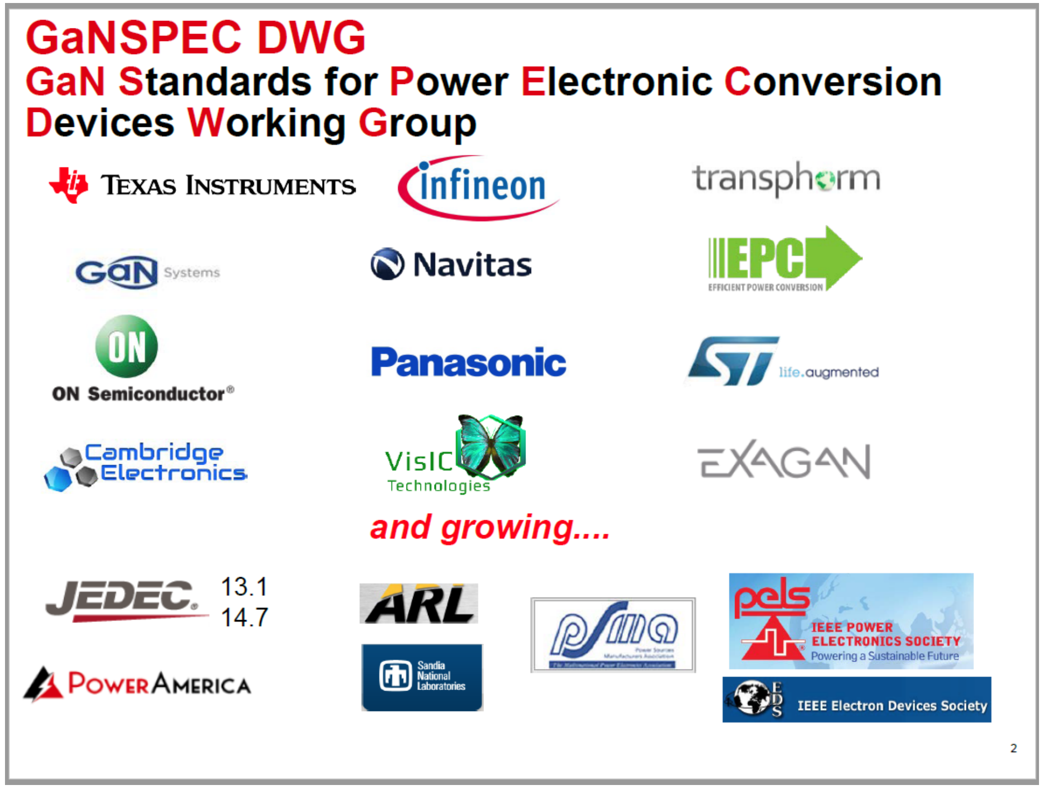
ESD protection integrated into all pins (>1000 V HBM, >1000 V CDM)

Eliminates parasitic inductance, turn-off losses, and false turn-on of eMode gate

All benefits while delivering the performance advantage of Navitas' GaN Power ICs!

Taking GaN Beyond JEDEC & Industry Norms

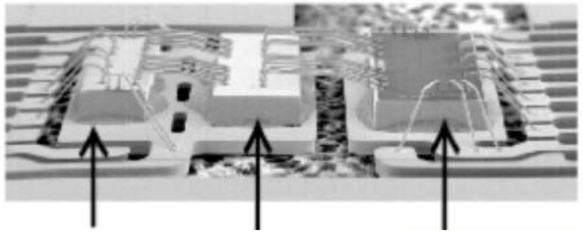
- GaNSPEC DWG
  - GaN Standards for Power Electronic Conversion Devices Working Group
- Broad industry cooperation
- Defining new standards and guidelines for GaN quality & reliability
  - Test methods
  - Reliability & qualification procedures
  - Datasheet parameters

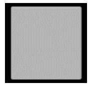


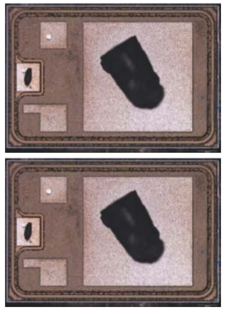
APEC 2017 Industry Presentation

Navitas

High-Frequency Half-Bridge Integration







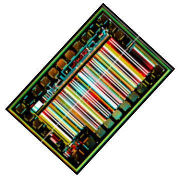
I/F Chip Si CMOS

On-chip Transformer SiO_2 / Polyimide

Gate Driver Chip Si CMOS

Bootstrap Diode Si / SiC

Half-Bridge FETs Si



AllGaN™ Technology
Lateral 650V GaN-on-Si

Disparate technologies:
Hybrid isolator, discrete driver, discrete power, bootstrap diode

Monolithic platform:
Lateral GaN-on-Si, Half-Bridge GaN Power IC

High Loss → **Low Loss**

High Loss:

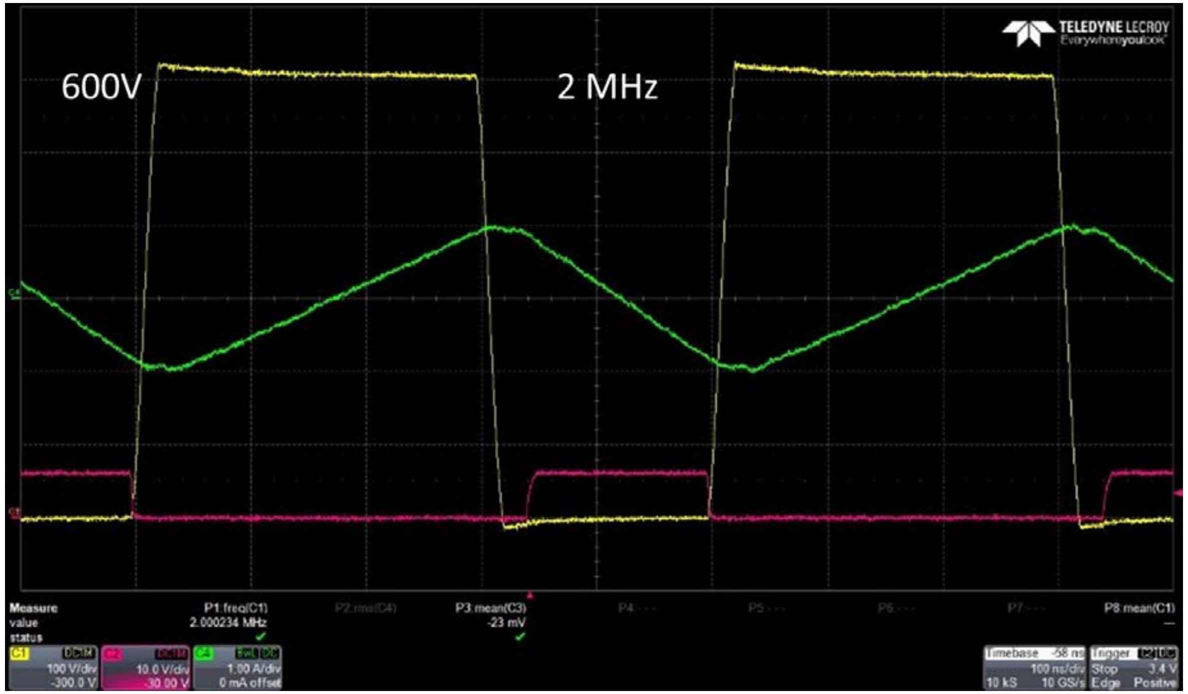
1) Driver loss, R_G loss
2) Bootstrap diode Qrr, Vf
3) Pulsed high current level shifter power

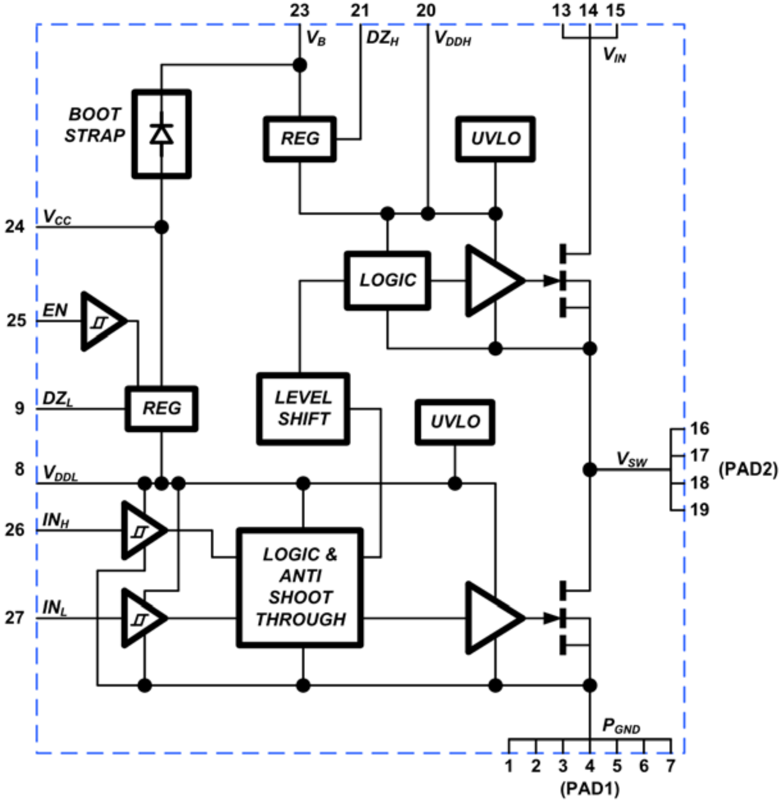
Low Loss:

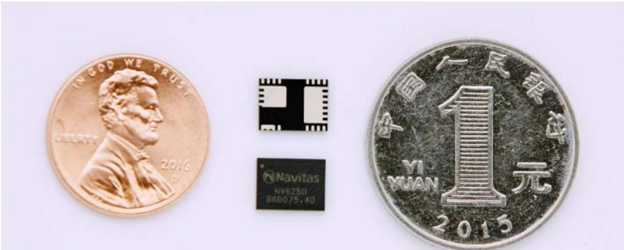
1) No gate driver loop parasitics, matched driver-FET capability, negligible loss vs frequency
2) Zero Q_{rr} ,low V_{DSON} in synchronous charging
3) Extremely fast, low-power level shifter, multi-MHz operation, short propagation delay

AllGaN™ Half-Bridge GaN Power IC

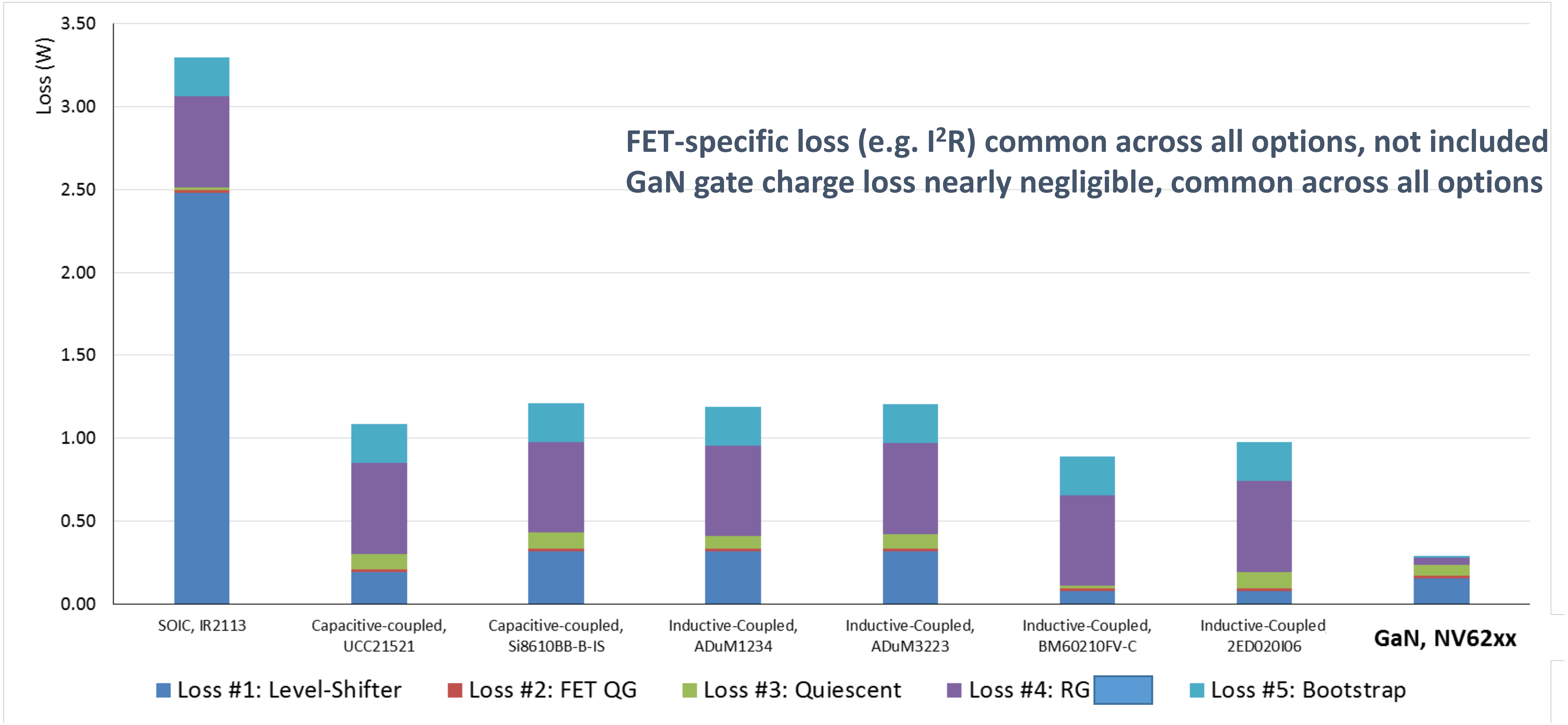
- Integrated 650V 10A Power Circuit
  - 2x GaN FETs & 2x GaN drivers
  - Gate voltage regulation
  - Level-shift circuit, bootstrap charging
  - UVLO, ESD, shoot-through protection





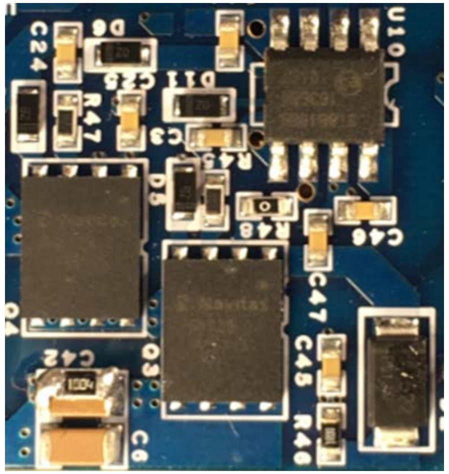

6 x 8 mm QFN

3x Lower Drive and Level Shift Loss at 1 MHz

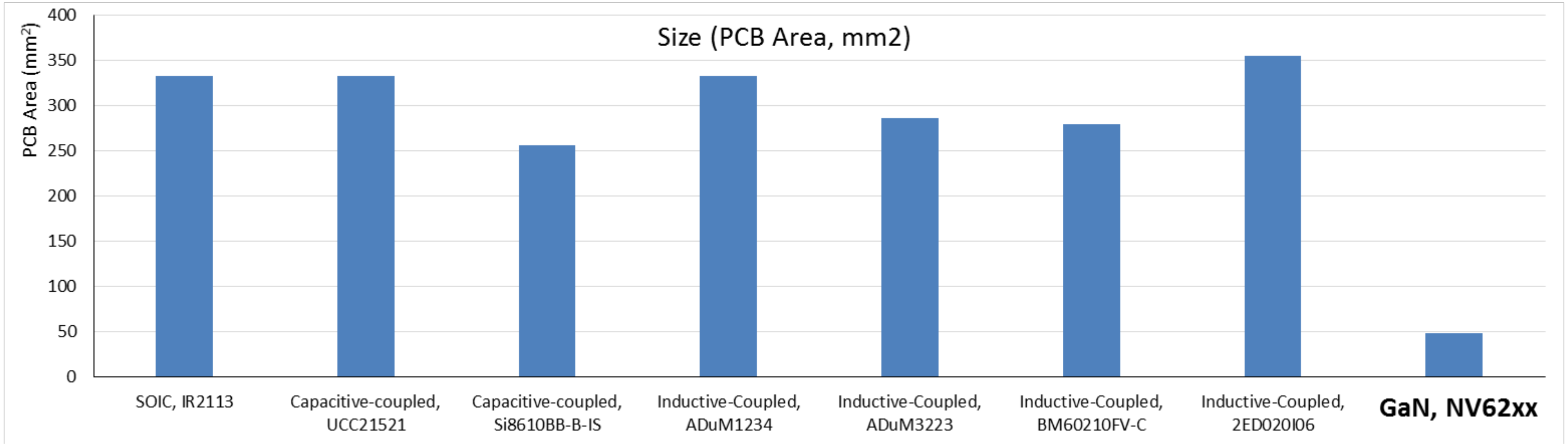


5x Smaller Footprint than Best Single GaN

Digital Isolator
2x Single GaN Power ICs
Bootstrap diode
Passives



Half Bridge
GaN Power ICs
5X smaller than
alternatives

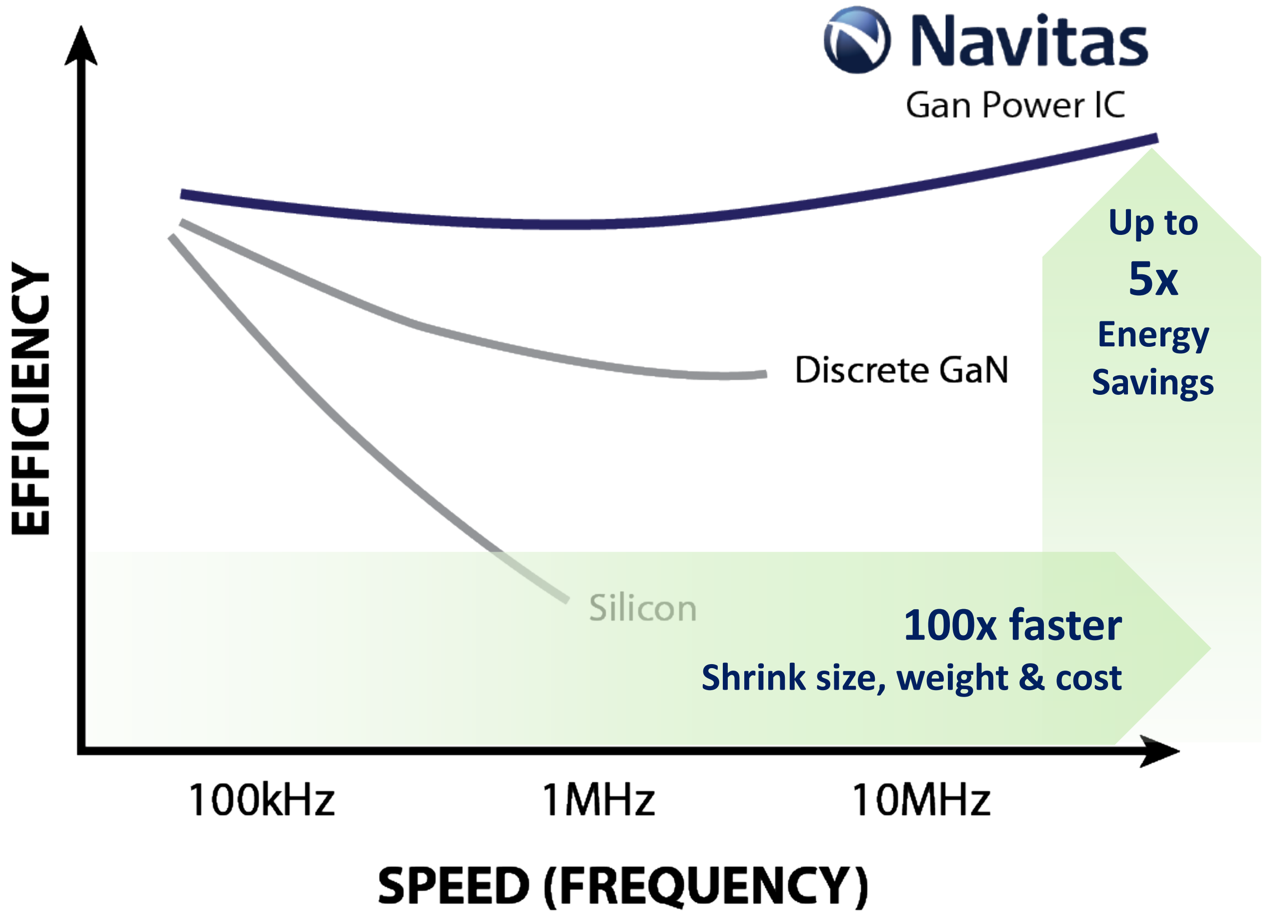


GaN Power IC Technology

- Why GaN on Silicon?
- GaN IC Development History
- Navitas AllGaN™ Power ICs
- **Application examples**
- Future directions
- Summary

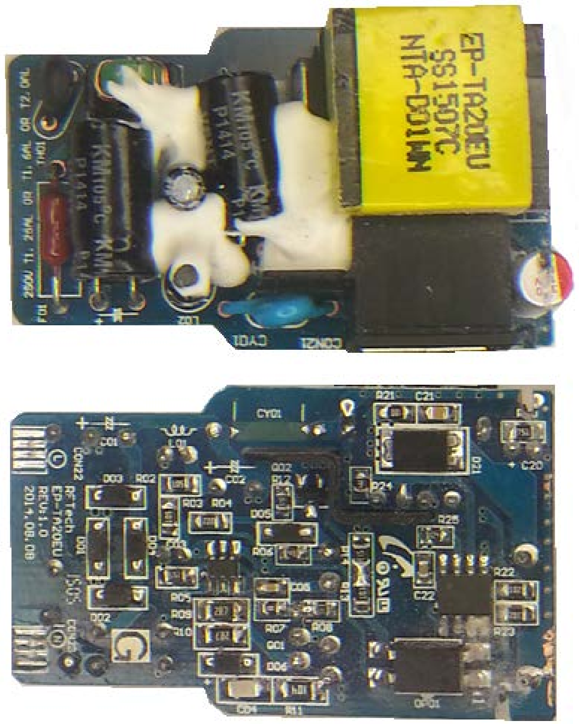
Power Electronics: *Speed & Efficiency are Key*

- **Speed** enables ***small size***, ***low-cost*** and ***faster charging***
- **Efficiency** enables ***energy savings***
- With Silicon or Discrete GaN power devices, you can get one ***or*** the other
- With GaN power ICs, you get ***both at the same time*** with unequaled **Speed & Efficiency**

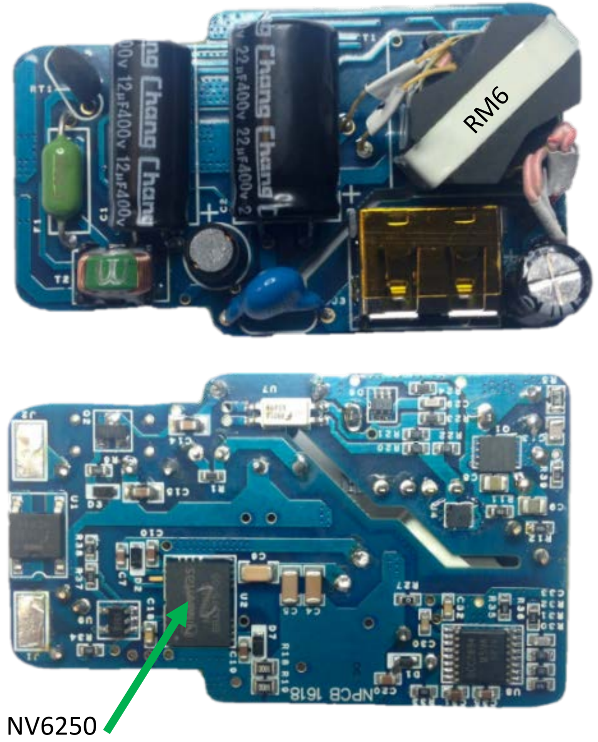


66% Higher Power with Half-Bridge GaN Power IC

Original 15 W AC/DC charger case



Original 15 W, Si-based QR Flyback
~100 kHz, <90% efficient

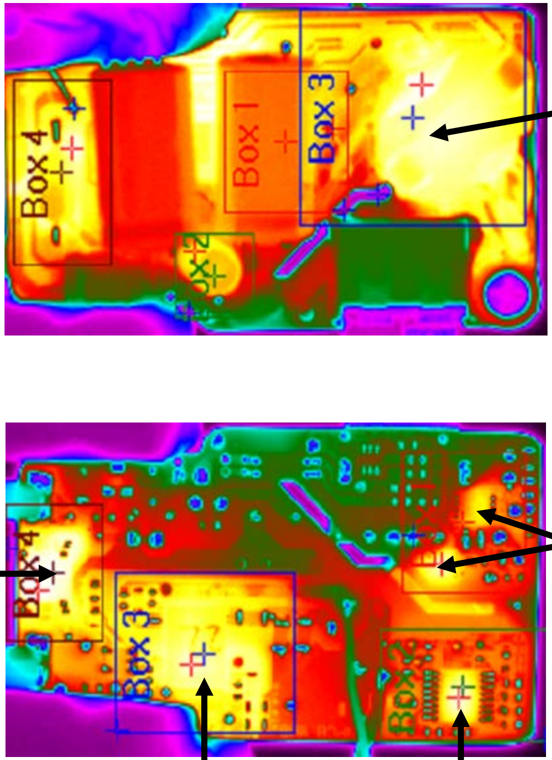


Upgraded 25 W Active Clamp Flyback
Half-Bridge GaN Power IC
~400 kHz, >94% efficient

25W Cool Thermals (12.5V, 2A)

Navitas

25°C ambient
Full load
90 V_{AC} input
No heatsinking



Transformer
62°C

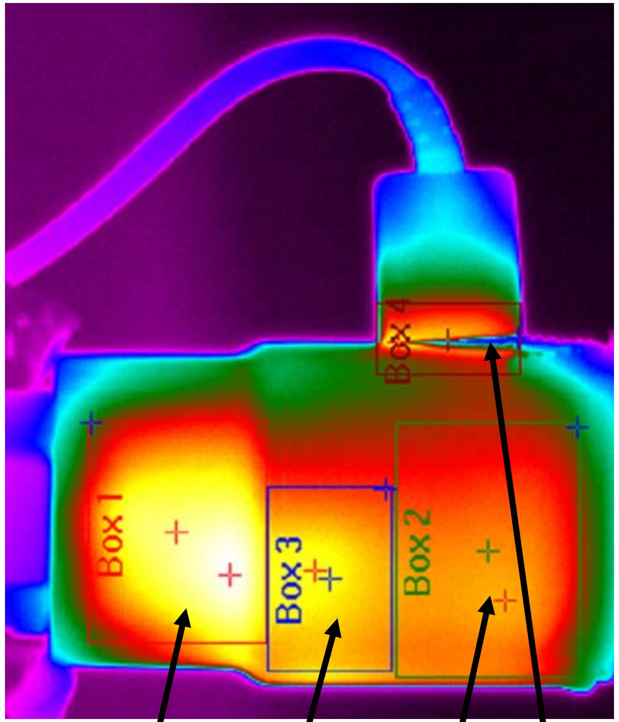
AC
Rectifier
65°C

SR FET
+ SR IC
62°C

GaN Power IC
63°C

ACF IC
63°C

No case



Peak: 49.7°C
Average: 45.8°C

Peak: 45°C
Average: 43.3°C

Peak: 46.6°C
Average: 45.1°C

Peak: 47.2°C
Average: 41.6°C

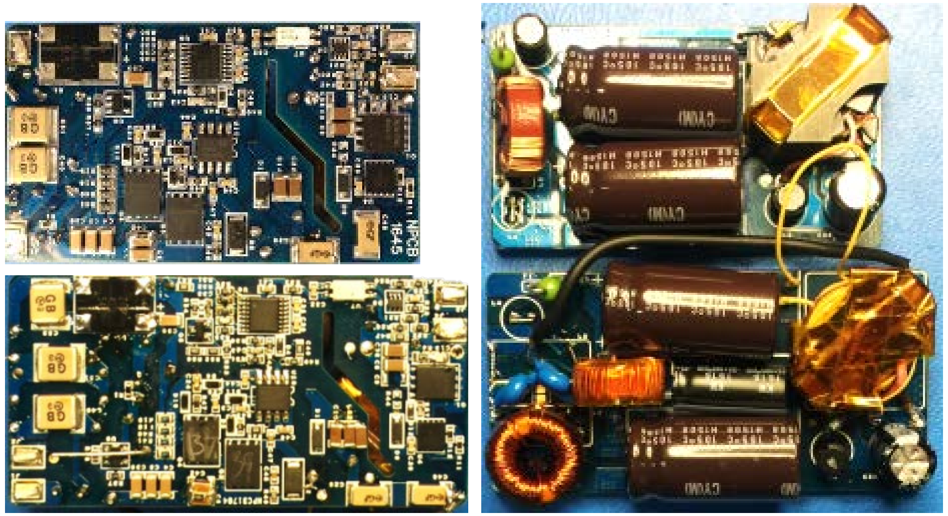
Cased

45W, 65W 24W/in³ ACF

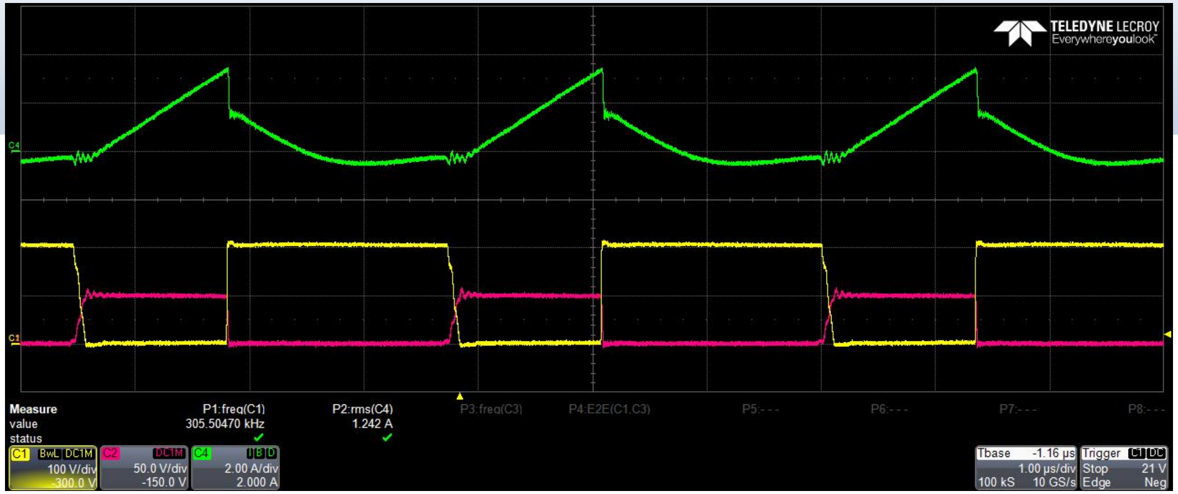
45W = 59.1 x 33.5 x 15.7 mm = 24 W/in³ (uncased)
2x NV6115 (160mΩ)

45W

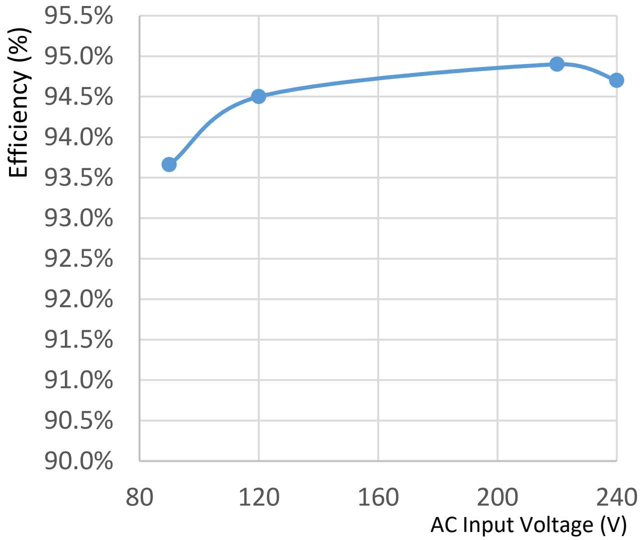
65W



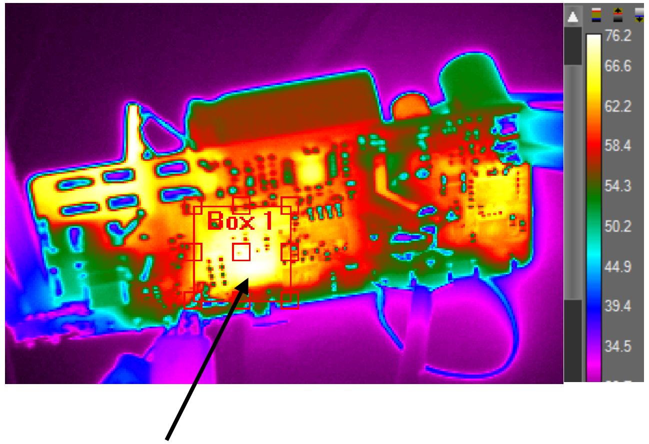
65W = 66.7 x 33.5 x 15.7 mm = 30 W/in³ (uncased)
1x NV6115 (160mΩ) + 1x NV6117 (110mΩ)



ACF switching waveforms, 300 kHz

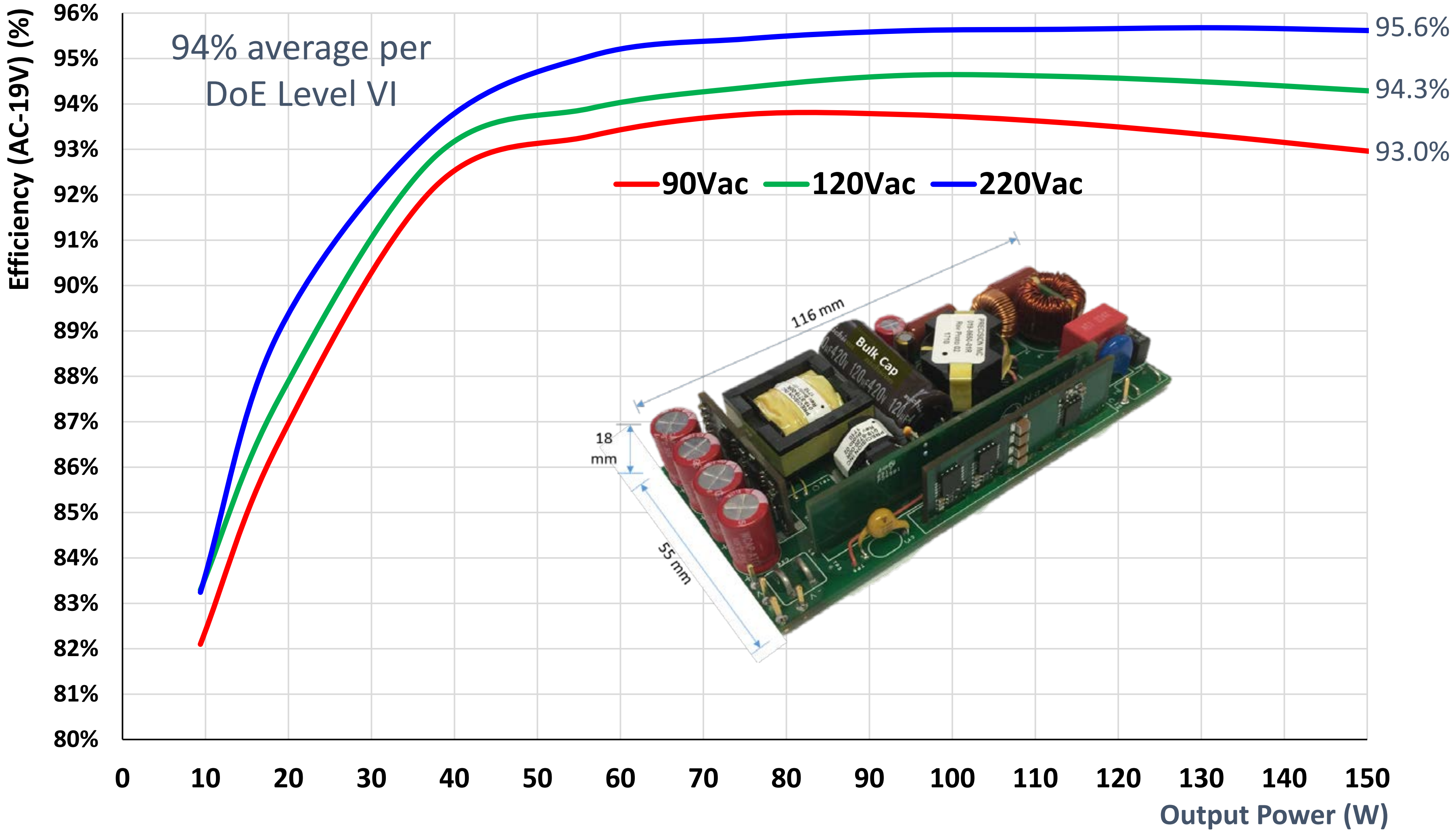


65W Efficiency vs. AC line
(25°C ambient, no airflow, full load)

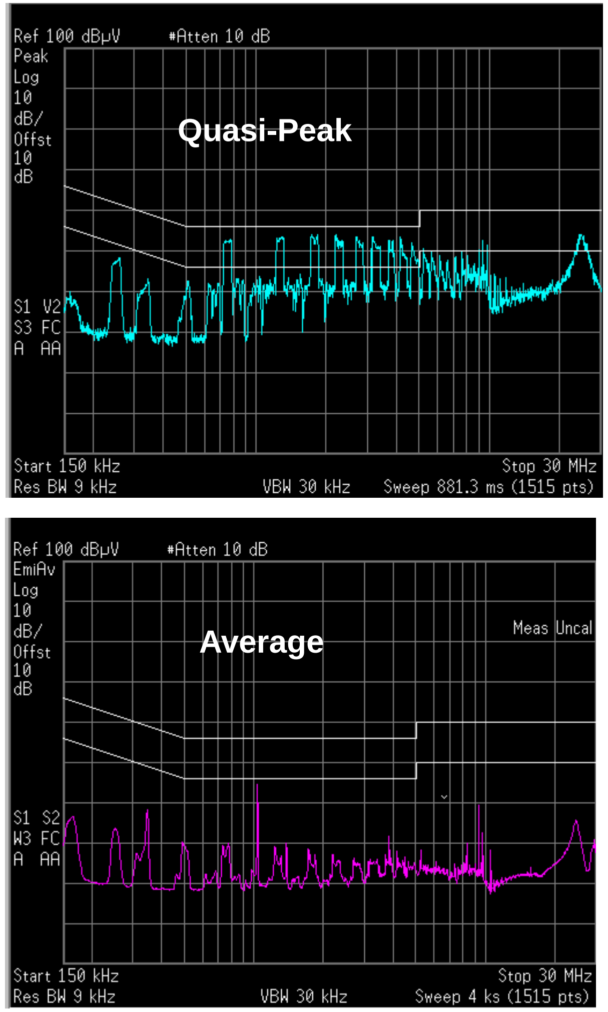


65W Thermal Performance
($90V_{AC}$, 25°C ambient, no airflow, full load)

150W AC-19V, ~300 kHz, 21 W/in^3



Conducted EMI



1 MHz, 3.2 kW 65W/in^3 AllGaN™ AC/DC

Navitas

NC STATE UNIVERSITY

Heatsink
(PFC Boost Switch)

PFC choke
(Hitachi ML91S)

3x paralleled input current-limiting relays

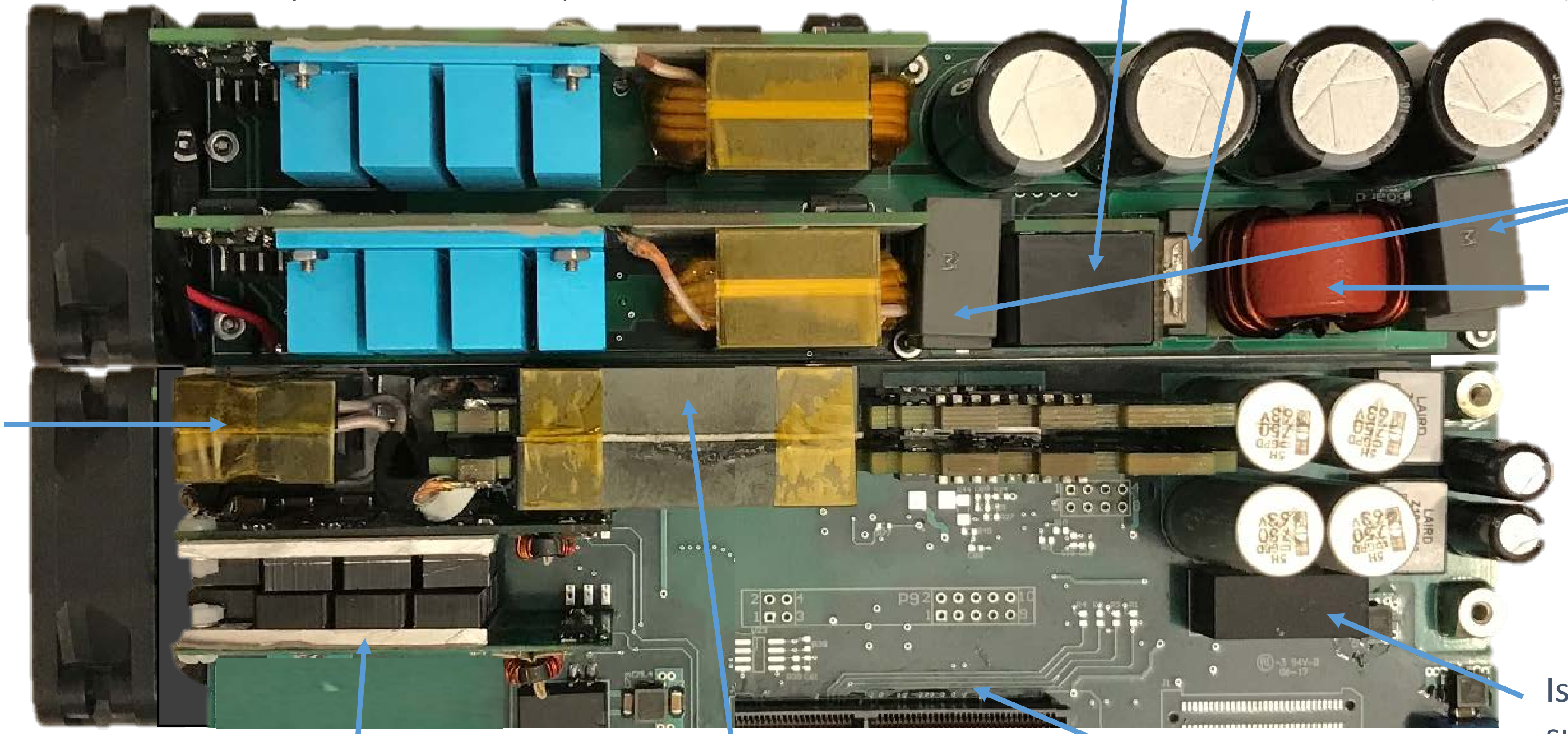
2x DM choke (in series)

AC input

2x + 2x X-caps

CM choke
(no EMI test yet)

Coupled Res
Inductor



48 V Output

Isolated power
supply for SR

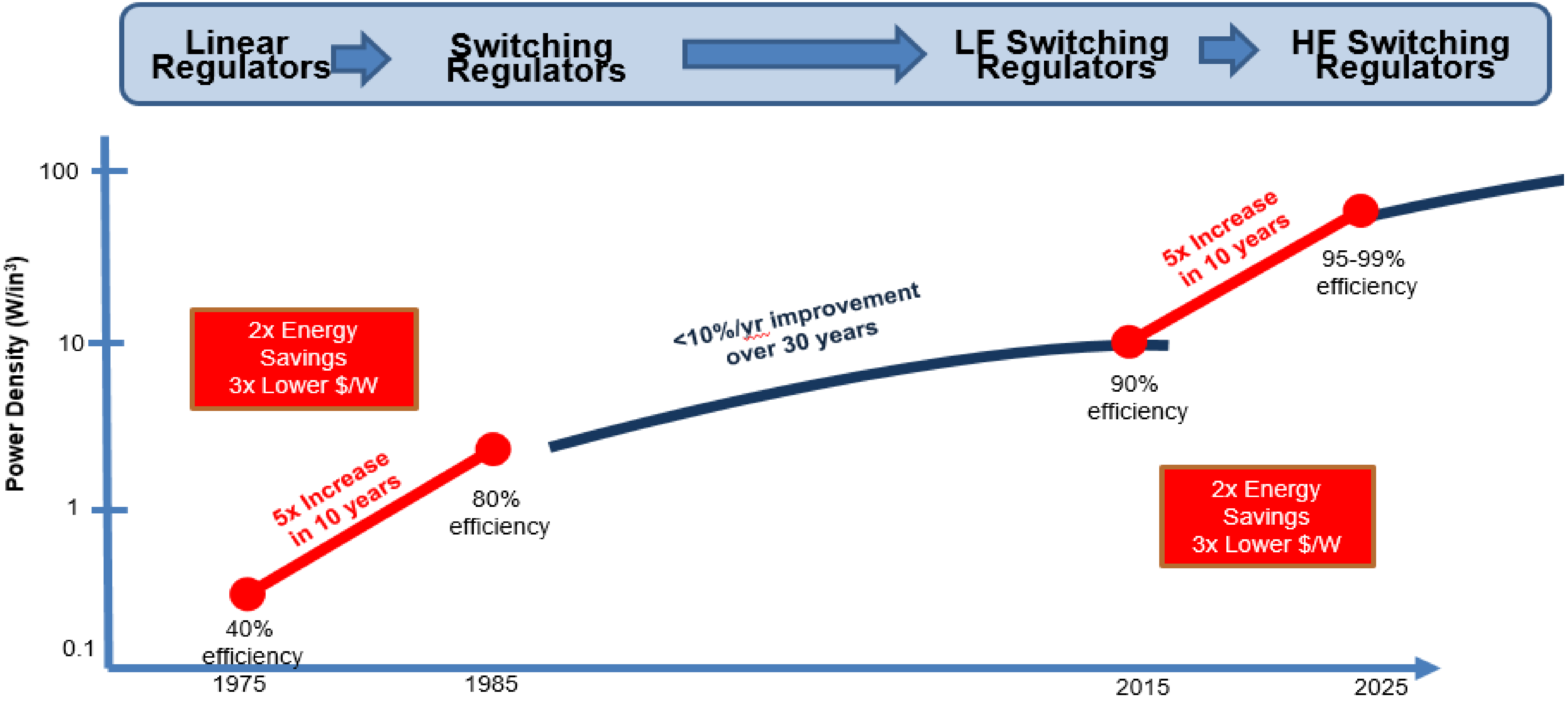
Coupled LLC transformer

Full bridge LLC (1/2 on each card)
(using paralleled NV6117s)

Full bridge SR (80V EPC GaN)
(16 or 24 TBD in final test)

Work in progress, rendered image

GaN Power ICs Accelerate Change in Power Electronics



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GaN Power ICs: The Road Ahead

What's Left to Work on?

- A good P-channel for CMOS
- High density digital
- Memory (volatile, non-volatile, OTP, MTP, etc.)
- ICs rated for temperatures > 150C
- A full expansion of the cell library
- A process design kit

Summary

- GaN Power ICs set new standards for ease-of-use, speed, efficiency, density, & system cost
- Proven technology, ready for commercial use
- Best technology, for 90-305 V_{AC} off-line applications, 25W to 5kW
- GaN Power ICs + high-frequency magnetics + new controllers = A bright future of rapid advancement in the power electronics industry!

Acknowledgements

- The entire team at Navitas
- Advisors in the preparation of the content
  - Prof. Kevin Chen, Hong Kong University of Science and Technology
  - Prof. Dragan Maksimovich, University of Colorado, Boulder
  - Dr. Tetsuzo Ueda and Dr. Yasuhiro Uemoto, both of Panasonic

The 29th International Symposium on Power Semiconductor Devices and ICs
ISPSD 2017
May 28 -June 1, 2017
Sapporo, Japan
Conference site: Royton Sapporo

IEEJ IEEE Electron Devices Society pels NPERC-J

GaN Power IC Technology

Past, Present, and Future

The 29th International Symposium on Power Semiconductor Devices and ICs

Plenary Session

Dan Kinzer, CTO/COO, dan.kinzer@navitassemi.com

May 29, 2017