GaN Power IC Technology
Past, Present, and Future

The 29th International Symposium on Power Semiconductor Devices and ICs
Plenary Session

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May 29, 2017
GaN Power IC Technology

• Why GaN on Silicon?
• GaN IC Development History
• Navitas AllGaN™ Power ICs
• Application examples
• Future directions
• Summary
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Performance Limits of Power Semi Materials

Important material attributes

- High voltage operation
- Electric Field (MV/cm)
- Energy gap (eV)
- Thermal Conductivity (W/cm·°C)
- Electron velocity (x107 cm/s)
- Melting point (x1000 °C)
- High T° applications

Theoretical 1-D $R_{DS(ON)}/BV_{DSS}$ for Vertical Devices

- Si limit
- SiC limit
- GaN limit
- Diamond limit

Si limit

$T = 300$ K

Maximum Voltage (V)

$R_{DS(ON)}$ (mΩ·cm²)

GaN limit
Performance Limits of Power Semi Materials

Important material attributes:
- High voltage operation
- Energy gap (eV)
- Electron velocity (x10^7 cm/s)
- Melting point (x1000 °C)
- Thermal conductivity (W/cm·°C)
- High T° applications

Current Performance:
- Vertical Silicon
- Lateral GaN

GaN 2-D Limit for Lateral Devices:
- (with 400 ohm-sq 2-DEG)
- 2.5 MV/cm
- 3.5 MV/cm
- Almost matches Diamond!

Theoretical 1-D $R_{DS(ON)}/BV_{DSS}$ for Vertical Devices

- Si limit
- SiC limit
- Diamond limit

$T = 300$ K

Maximum Voltage (V)

$R_{DS(ON)}$ (mΩ·cm²)

$BV_{DSS}$
Lateral GaN Advantage for Off-line Applications

- WBG GaN material allows high electric fields so high carrier density can be achieved.
- Two-dimensional electron gas with AlGaN/GaN heteroepitaxy structure gives very high mobility in the channel and drain drift region.
- Lateral device structure achieves extremely low $Q_g$ and $Q_{oss}$ and allows integration.
- Integration on silicon substrates means mature low cost wafer fabrication is available.

![Diagram of Lateral GaN Structure]

- Source
- Drain
- Gate
- Dielectric
- AlGaN barrier
- 2deg
- GaN Buffer
- Transition Layer
- Silicon Substrate
Comparison of Different GaN Technologies

- **Cascode GaN Switch**
  - Relatively easy to control gate
  - Traditional packages
  - Large package inductance
  - Prone to oscillation
  - No dV/dt control
  - Complicated multi-die package

- **E-mode GaN Switch**
  - Extremely low gate charge
  - No reverse recovery loss
  - Easy to package
  - Low package inductance
  - Can control dV/dt
  - Hard to control gate
GaN vs Silicon Output Characteristics

- Switching loss:
  \[ P_{\text{LOSS}} = E_{\text{OSS}}(V_{\text{DS}}) \times F_{\text{SW}} \]
- \( C_{\text{OSS}} \rightarrow \text{Delay (limits } F_{\text{SW}}) \)
- Too slow \( \rightarrow \) partial ZVS \( \rightarrow E_{\text{OSS}} \) loss

- Si \( C_{\text{OSS}} \) is 50x-100x higher than GaN at \( V_{\text{DS}} < 30\text{V} \)
- Si \( P_{\text{LOSS}} \) is 3x higher than GaN at 200V (partial ZVS)
- Big effect at full or light load condition

- Further information: “\( C_{\text{OSS}} \) Hysteresis in Advanced Superjunction MOSFETs”, Harrison, APEC 2016
Hard-Switch $\Rightarrow$ Soft-Switch with **GaN Power IC**

**Primary Switch Power Loss:**

\[
P_{\text{FET}} = P_{\text{COND}} \ast k + P_{\text{DIODE}} + P_{\text{T-ON}} + P_{\text{T-OFF}} + P_{\text{DR}} + P_{\text{QRR}} + P_{\text{QOSS}}
\]

- **k-factor**: $>1$ due to increased circulating current, duty cycle loss
- **$P_{\text{T-On}}$**: $= 0$ (soft-switch)
- **$P_{\text{Qoss}}$**: $\downarrow 10\times$ 2-3× (GaN $C_{\text{OSS}}$ charging/discharging loss negligible up to 2MHz)
- **$P_{\text{DRIVER}}$**: $\downarrow 10\times$ (GaN $P_{\text{DR}}$ negligible up to 2MHz)
- **$P_{\text{QRR}}$**: $= 0$
- **$P_{\text{DIODE}}$**: $\downarrow 3\times$ 2× (synchronous rectification with improved dead-time control)
- **$P_{\text{T-OFF}}$**: $= 0$ Reduced (near-zero drive loop impedance with integration)

>10x frequency increase possible with **higher efficiencies**
# Class Phi-2 DC/AC converter

- 50% less loss than RF Si
- 16x smaller package
- Air-core inductors
- Minimal FET loss
- Negligible gate drive loss

![Class Phi-2 DC/AC converter diagram](image)

<table>
<thead>
<tr>
<th>Technology</th>
<th>V</th>
<th>Pack (mm)</th>
<th>F\textsubscript{SW} (MHz)</th>
<th>Eff. (%)</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Si (ARF521)</td>
<td>500</td>
<td>M174 22x22</td>
<td>27.12</td>
<td>91%</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td>650</td>
<td>QFN 5x6</td>
<td>27.12</td>
<td>96%</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td>650</td>
<td></td>
<td>40.00</td>
<td>93%</td>
<td>115</td>
</tr>
</tbody>
</table>

- 27.12 MHz, φ2 Inverter, V\textsubscript{DS} of GaN
- 20ns/div, 150V/div

![Diagram with waveforms](image)
GaN Power IC Technology

- Why GaN on Silicon?
- **GaN IC Development History**
  - Navitas AllGaN™ Power ICs
  - Application examples
  - Future directions
  - Summary
Early years of GaN Power IC Technology

• Concept of GaN power ICs developed as potential of GaN for power widely explored
• Ideal device has simple digital I/O, and all necessary functions to manage a load, such as gate drive, sensing, protection, & control
• Integrated dMode & eMode small signal HEMT, Schottky, Power HEMT, and power rectifier were proposed and demonstrated
• Threshold shift into positive range used F- implant, with some stability issues

Since then, a variety of circuit blocks and functions have been reported:

- Comparator, with both eMode and dMode input pairs
- Temperature sensors and references
- Integrated controller functions such as sawtooth generator and PWM comparator


Multiple Power Devices on Chip

- One reported 3-phase inverter intended for medium voltage motor driver
- A novel integration of 9 bidirectional switches in AC/AC 3-phase to 3 phase matrix converter
  - Gate drive function is by eighteen rectifier circuits that receive 5 Ghz pulse trains during Intended on periods
- A low voltage assymetric synchronous buck circuit for point-of-load converter
  - An early demonstration of an integrated output buffer stage to provide a gate drive output buffer function

Hybrid Integration: Chip-on-Chip Bonding

- An alternative to full monolithic power IC integration:
- Select GaN transistors from a source wafer to provide high voltage and/or high frequency capability
- Using a designed stamp, pick the devices on an interval that matches the size of the target IC.
- Transfer and release to form the power GaN on CMOS chip on chip

Pushing GaN Power IC Technology >100 MHz

- This monolithic GaN buck converter example is showing operation with near 90% total efficiency up to 100MHz and 45V input.
- At these frequencies, high Q RF compatible air core magnetics and low ESR ceramic capacitors are essential.

<table>
<thead>
<tr>
<th>Switching frequency, $f_s$ [MHz]</th>
<th>20</th>
<th>50</th>
<th>100</th>
<th>200</th>
<th>400</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage [V]</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>20</td>
<td>45</td>
</tr>
<tr>
<td>Maximum output power [W]</td>
<td>16.0</td>
<td>10.1</td>
<td>7.1</td>
<td>3.4</td>
<td>5.0</td>
<td>6.0</td>
</tr>
<tr>
<td>Peak power stage efficiency [%]</td>
<td>95.0</td>
<td>94.2</td>
<td>93.2</td>
<td>86.5</td>
<td>72.5</td>
<td>91.7</td>
</tr>
<tr>
<td>Peak total efficiency [%]</td>
<td>92.5</td>
<td>91.7</td>
<td>89.2</td>
<td>82.0</td>
<td>67.0</td>
<td>90.2</td>
</tr>
<tr>
<td>Inductance (L) [nH]</td>
<td>160</td>
<td>90</td>
<td>47</td>
<td>22</td>
<td>12.5</td>
<td>9.0</td>
</tr>
<tr>
<td>Duty cycle (D) [%]</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>75</td>
<td>50</td>
<td>50</td>
</tr>
</tbody>
</table>

Recent Cell Library Development and Application

- A cell library includes current sources, comparators, bias and logic circuitry, a PTAT generator, and a reference.
- All of this is integrated in the example to provide a high voltage GaN single transistor Power IC with thermal protection.

Dilip Risbud, Kenneth Pedrotti, “Analog and digital cell library in High Voltage GaN-on-Si Schottky Power Semiconductor Technology,” WiPDA, Nov. 7-9, 2016 Fayetteville, Ar, USA.
A Demonstration of Half Bridge Integration

- In order to suppress current collapse, the chip substrate is connected to a passive network formed by the $R_{DIV}$ divider and the chip capacitance that causes it to closely follow the switch node.

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Navitas AllGaN™ Power ICs

Fastest, most efficient GaN Power FETs

>20x faster than silicon
>5x faster than cascoded GaN
Proprietary design

iDrive First & Fastest
Integrated GaN Gate Drivers

>3x faster than any other gate driver
Proprietary design
30+ patents granted/applied

World’s First
AllGaN™ Power IC

Up to 40MHz switching, 5x higher density & 20% lower system cost
Multiple Discretes $\rightarrow$ Monolithic Integration

- **Normally-ON (dMode)**
  - Co-pack Cascode FET
  - Discrete, External Driver
  - Multiple Chips, Two Packages

- **Normally-OFF (eMode)**
  - Co-pack Cascode FET & Driver IC
  - Charge Pump Negative Rail
  - Two Die, One Package

- **Fast, Easy, Low Cost**
Removing Speed Limits:
Navitas GaN Power IC

- **Monolithic** integration
- 10X lower drive loss than silicon
- Driver impedance matched to power device
- Short prop delay (10ns)
- Zero inductance turn-off loop
- Digital input (hysteretic)
- Rail-rail drive output
- Reduces layout sensitivity

QFN 5x6mm
Speed & Integration → Eliminate Turn-off Losses

**External drivers**
- Just 1-2 nH of gate loop inductance can cause unintended turn-on
- Gate resistors reduce spikes but create additional losses

**Integrated GaN drivers (iDrive™)**
- Eliminate the problem
- Negligible turn-off losses
GaN Power IC – Fast & Efficient

- 500 V Switching
- No overshoot / spike
- No oscillations
- ‘S-curve’ transitions
- Zero Loss Turn-on
- Zero Loss Turn-off
- Sync Rectification
- High frequency
- Small, low cost magnetics

![Graph showing GaN Power IC performance characteristics](image-url)
Monolithic integration of GaN FET, GaN Driver, GaN Logic

- 650 V eMode power device
- 10x lower drive loss than silicon (<35 mW at 1 MHz)
- Driver impedance matched to power device
- Very fast (prop delay including turn-on/off 10ns)
- Zero inductance turn-off loop
- High dV/dt immunity (200 V/ns)
  - Regulated gate voltage
  - Controllable turn-on dV/dt
- Digital input

GaN Power IC – Voltage Slew Rate Control

- dV/dt controllable from 180 V/ns to 10 V/ns for EMI optimization
**Reliability Benefits of GaN Power IC**

- **Sensitive eMode gate node protected from system noise and spikes**
- **Built-in regulator precisely controls gate voltage applied to eMode gate**
- **ESD protection integrated into all pins** (≥1000 V HBM, >1000 V CDM)
- **V_{MAX} on V_{CC} & V_{PWM} pins have 30 V rating**
- **Eliminates parasitic inductance, turn-off losses, and false turn-on of eMode gate**
- **All benefits while delivering the performance advantage of Navitas’ GaN Power ICs!**
Taking GaN Beyond JEDEC & Industry Norms

• GaNSPEC DWG
  • GaN Standards for Power Electronic Conversion Devices Working Group

• Broad industry cooperation

• Defining new standards and guidelines for GaN quality & reliability
  • Test methods
  • Reliability & qualification procedures
  • Datasheet parameters

APEC 2017 Industry Presentation
High-Frequency Half-Bridge Integration

Disparate technologies:
Hybrid isolator, discrete driver, discrete power, bootstrap diode

High Loss
1) Driver loss, $R_G$ loss
2) Bootstrap diode $Q_{rr}$, $V_f$
3) Pulsed high current level shifter power

Low Loss
1) No gate driver loop parasitics, matched driver-FET capability, negligible loss vs frequency
2) Zero $Q_{rr}$, low $V_{DSON}$ in synchronous charging
3) Extremely fast, low-power level shifter, multi-MHz operation, short propagation delay
AllGaN™ Half-Bridge GaN Power IC

- Integrated 650V 10A Power Circuit
  - 2x GaN FETs & 2x GaN drivers
  - Gate voltage regulation
  - Level-shift circuit, bootstrap charging
  - UVLO, ESD, shoot-through protection

600V 2 MHz

6 x 8 mm QFN

30
3x Lower Drive and Level Shift Loss at 1 MHz

FET-specific loss (e.g. $I^2R$) common across all options, not included.
GaN gate charge loss nearly negligible, common across all options.

Loss (W)

- **SOIC, R2113**
- **Capacitive-coupled, UCC21521**
- **Capacitive-coupled, S8801088-B-1S**
- **Inductive-Coupled, ADuM1234**
- **Inductive-Coupled, ADuM3223**
- **Inductive-Coupled, BM60210PV-C**
- **Inductive-Coupled, 2ED020106**

Loss categories explained:
- **Loss #1: Level-Shifter**
- **Loss #2: FET QG**
- **Loss #3: Quiescent**
- **Loss #4: RG**
- **Loss #5: Bootstrap**

GaN, NV62xx
5x Smaller Footprint than Best Single GaN

Digital Isolator
2x Single GaN Power ICs
Bootstrap diode
Passives

Half Bridge
GaN Power ICs
5X smaller than alternatives
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Power Electronics: *Speed & Efficiency are Key*

- **Speed** enables *small size, low-cost* and *faster charging*
- **Efficiency** enables *energy savings*
- With Silicon or Discrete GaN power devices, you can get one *or* the other
- With GaN power ICs, you get *both at the same time* with unequaled Speed & Efficiency

![Graph showing efficiency vs. speed (frequency)](image)

- **Up to 5x Energy Savings**
- **100x faster**
- Shrink size, weight & cost
66% Higher Power with Half-Bridge GaN Power IC

Original 15 W AC/DC charger case

Original 15 W, Si-based QR Flyback
~100 kHz, <90% efficient

Upgraded 25 W Active Clamp Flyback
Half-Bridge GaN Power IC
~400 kHz, >94% efficient
25W Cool Thermals (12.5V, 2A)

25°C ambient
Full load
90 V_{AC} input
No heatsinking

Transformer 62°C
SR FET + SR IC 62°C
ACF IC 63°C
GaN Power IC 63°C
AC Rectifier 65°C

No case Cased

Peak: 49.7°C
Average: 45.8°C
Peak: 45°C
Average: 43.3°C
Peak: 46.6°C
Average: 45.1°C
Peak: 47.2°C
Average: 41.6°C

25°C ambient
Full load
90 V_{AC} input
No heatsinking
45W, 65W 24W/in³ ACF

45W = 59.1 x 33.5 x 15.7 mm = 24 W/in³ (uncased)
2x NV6115 (160mΩ)

65W = 66.7 x 33.5 x 15.7 mm = 30 W/in³ (uncased)
1x NV6115 (160mΩ) + 1x NV6117 (110mΩ)

65W Efficiency vs. AC line
(25°C ambient, no airflow, full load)

65W Thermal Performance
(90VAC, 25°C ambient, no airflow, full load)
150W AC-19V, ~300 kHz, 21 W/in³

- 94% average per DoE Level VI

Conducted EMI

Quasi-Peak

Average

Output Power (W)
Heatsink (PFC Boost Switch)

PFC choke (Hitachi ML91S)

3x paralleled input current-limiting relays

2x DM choke (in series)

AC input

2x + 2x X-caps

CM choke (no EMI test yet)

48 V Output

Coupled Res Inductor

Coupled LLC transformer

Full bridge LLC (1/2 on each card) (using paralleled NV6117s)

Full bridge SR (80V EPC GaN) (16 or 24 TBD in final test)

Isolated power supply for SR

1 MHz, 3.2 kW 65W/in³ AllGaN™ AC/DC
GaN Power ICs Accelerate Change in Power Electronics

- Linear Regulators
- Switching Regulators
- LF Switching Regulators
- HF Switching Regulators

- 2x Energy Savings
- 3x Lower $/W

- 5x Increase in 10 years
- 80% efficiency
- 40% efficiency

- <10% improvement over 30 years
- 90% efficiency
- 95-99% efficiency

- 2x Energy Savings
- 3x Lower $/W

- 5x Increase in 10 years

- 100
- 10
- 1
- 0.1

- 1975
- 1985
- 2015
- 2025
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GaN Power ICs: The Road Ahead
What’s Left to Work on?

• A good P-channel for CMOS
• High density digital
• Memory (volatile, non-volatile, OTP, MTP, etc.)
• ICs rated for temperatures > 150C
• A full expansion of the cell library
• A process design kit
Summary

• GaN Power ICs set new standards for ease-of-use, speed, efficiency, density, & system cost
• Proven technology, ready for commercial use
• Best technology, for 90-305 V\textsubscript{AC} off-line applications, 25W to 5kW
• GaN Power ICs + high-frequency magnetics + new controllers = A bright future of rapid advancement in the power electronics industry!
Acknowledgements

• The entire team at Navitas

• Advisors in the preparation of the content
  • Prof. Kevin Chen, Hong Kong University of Science and Technology
  • Prof. Dragan Maksimovich, University of Colorado, Boulder
  • Dr. Tetsuzo Ueda and Dr. Yasuhiro Uemoto, both of Panasonic
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