Power Technology Roadmap 2017

GaN Power ICs and the High Frequency Eco-System

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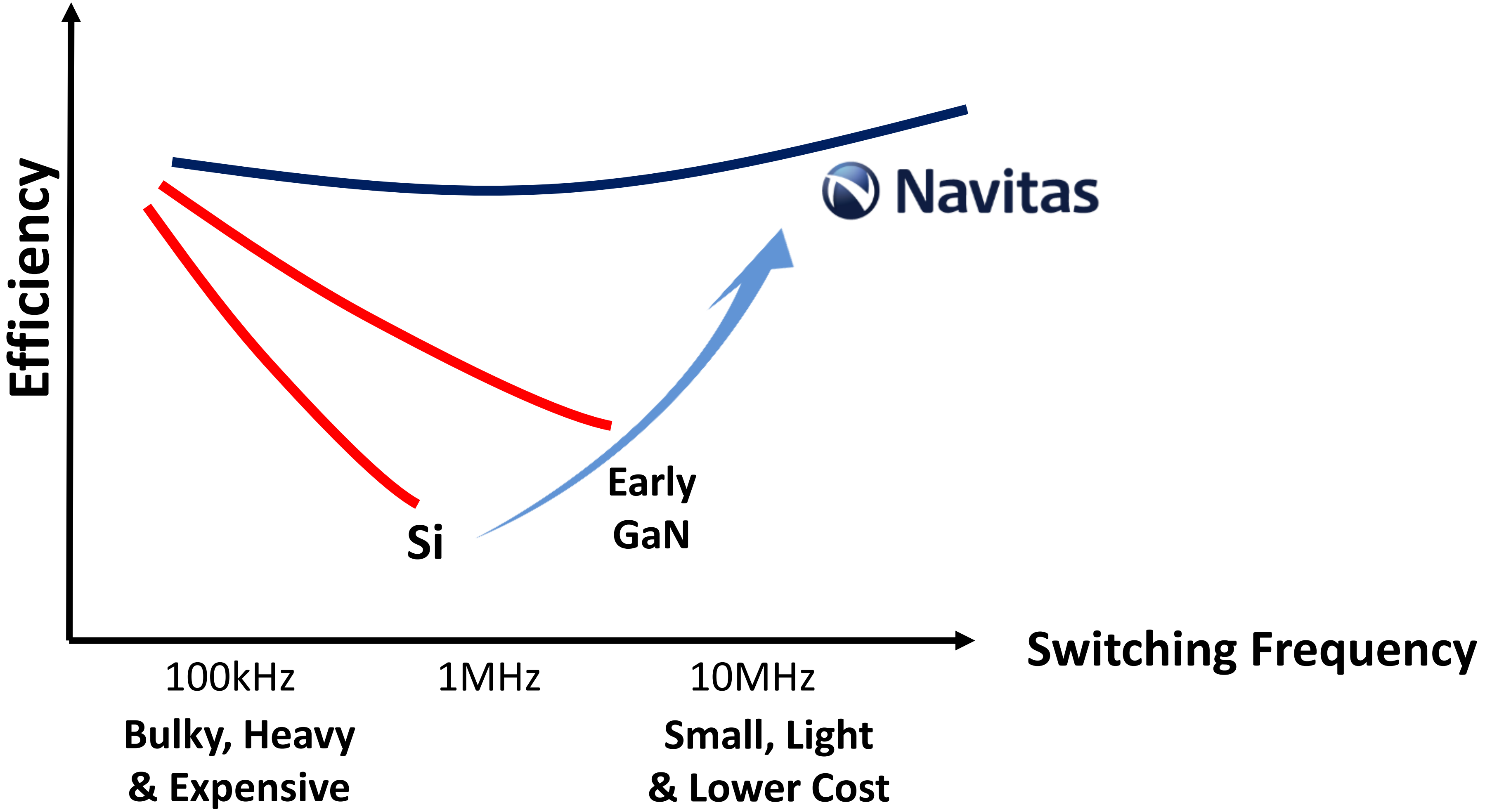
Frequency → Density → Efficiency



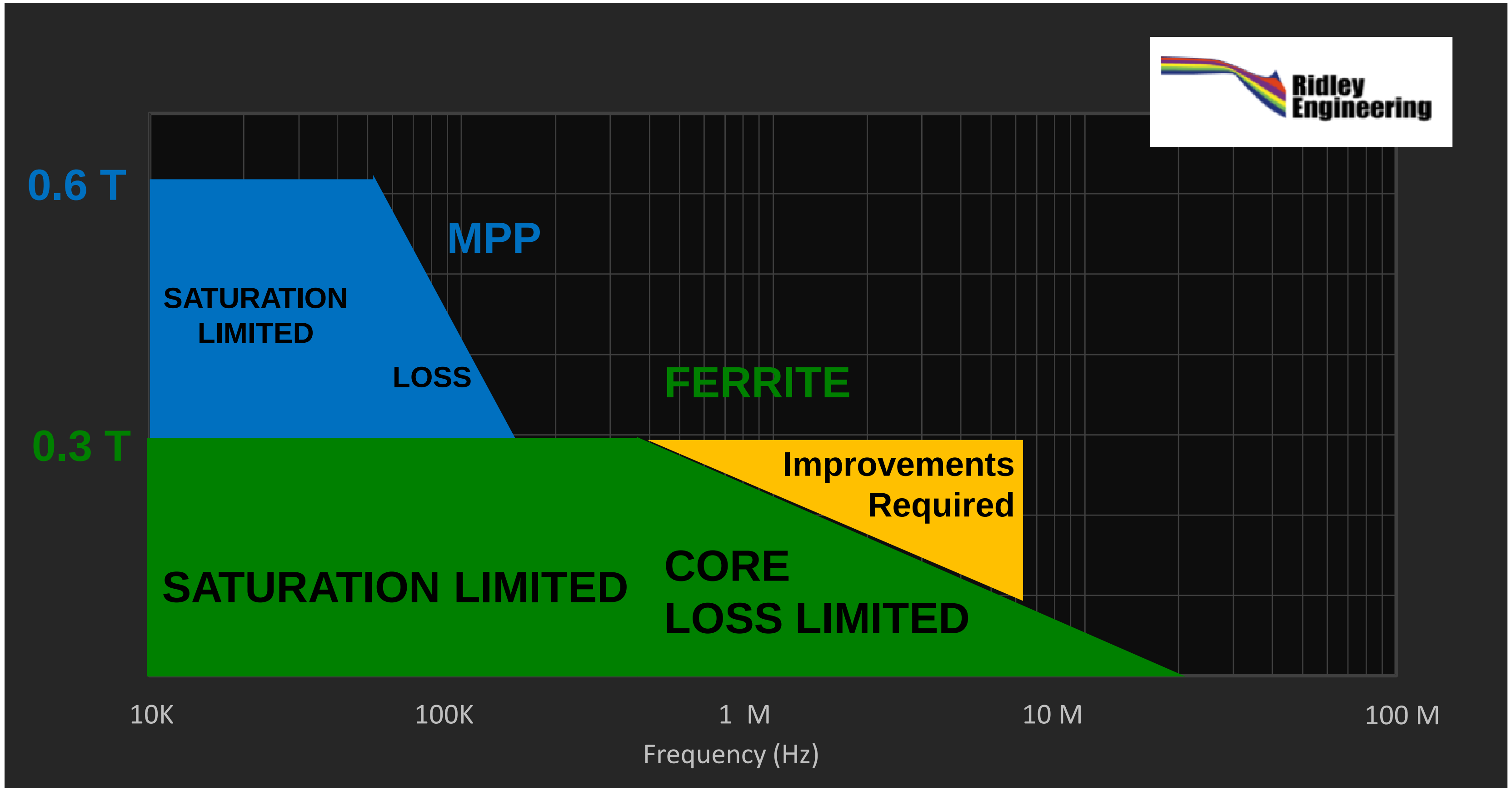
Looking for an Eco-System!

https://askabiologist.asu.edu/sites/default/files/image/article/2009/ecosystems_header.jpg

Magnetics:

Can Magnetics Rise to the Speed Challenge?

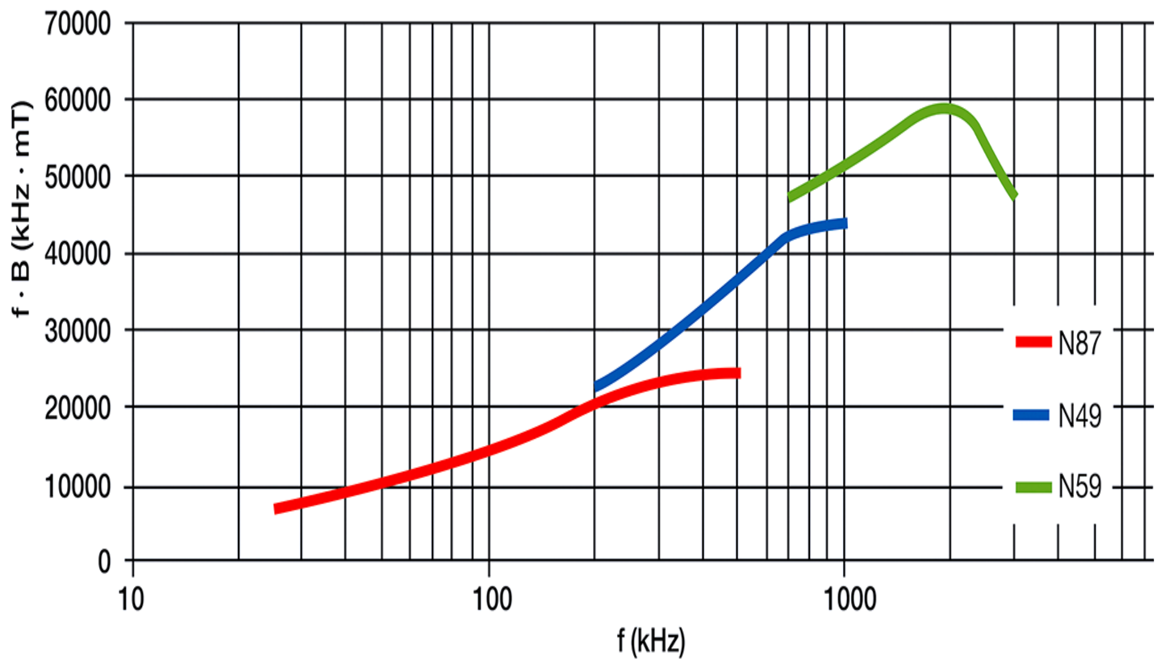
- Boundaries vary with material, DC/AC current mix, power, etc.
- Majority of mass production applications run 65kHz – 150kHz
- 5x frequency increase is within today's capability

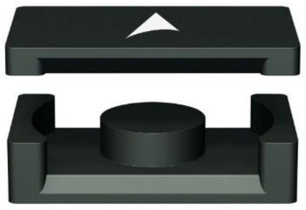


Magnetics:

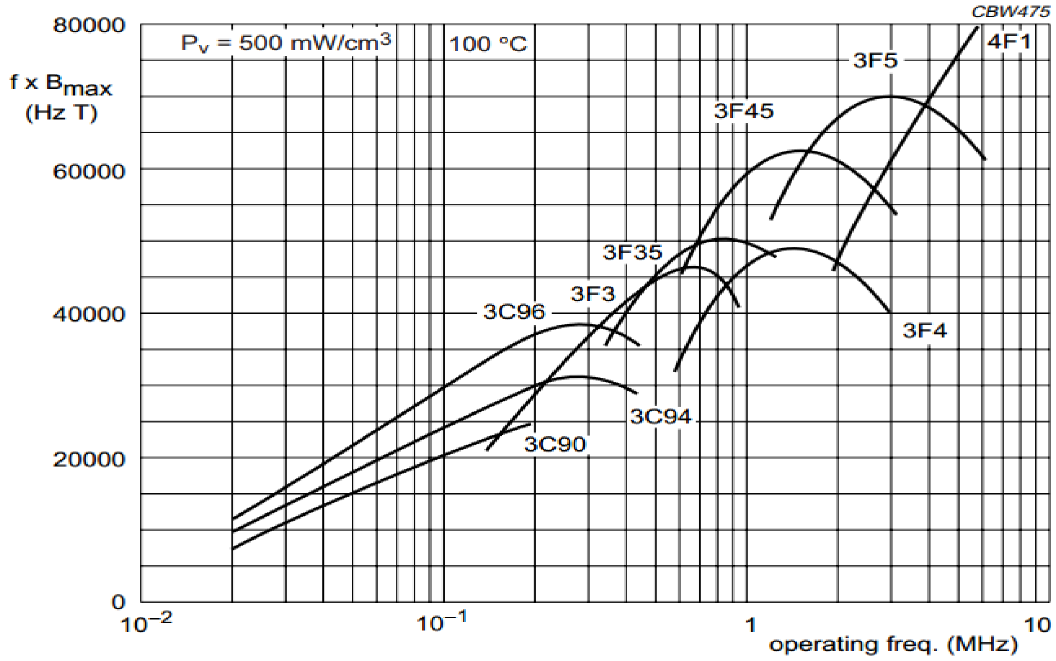
High Frequency Magnetics 'GaN Optimized'

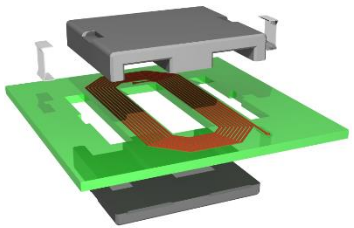
N59 optimized for 2MHz



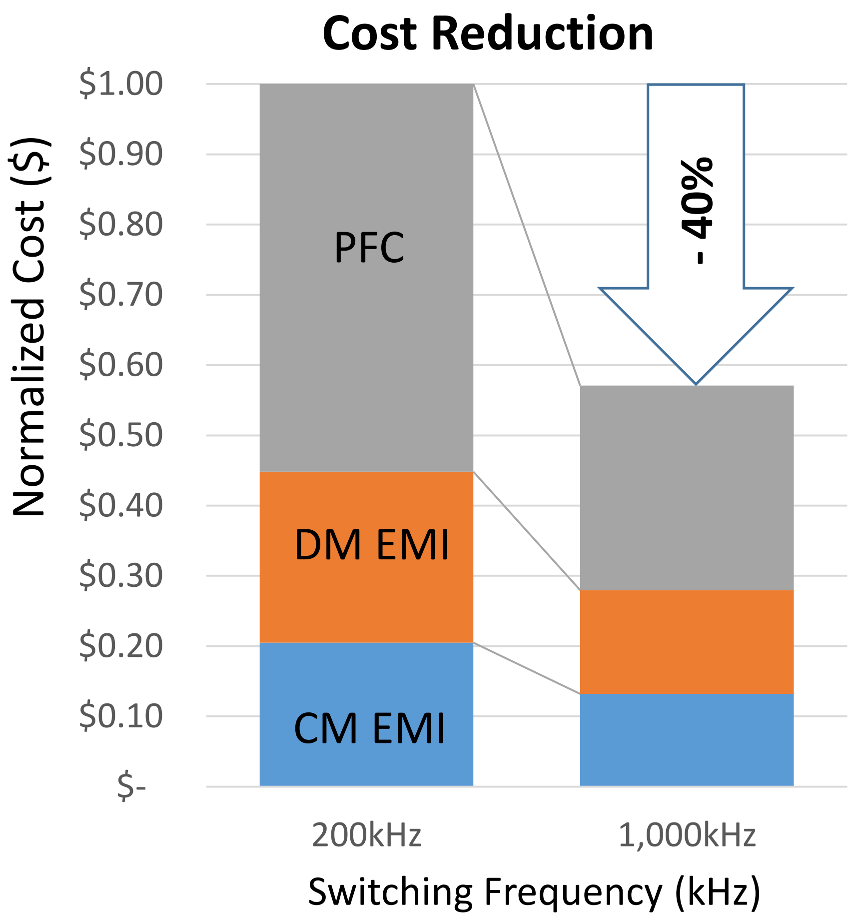


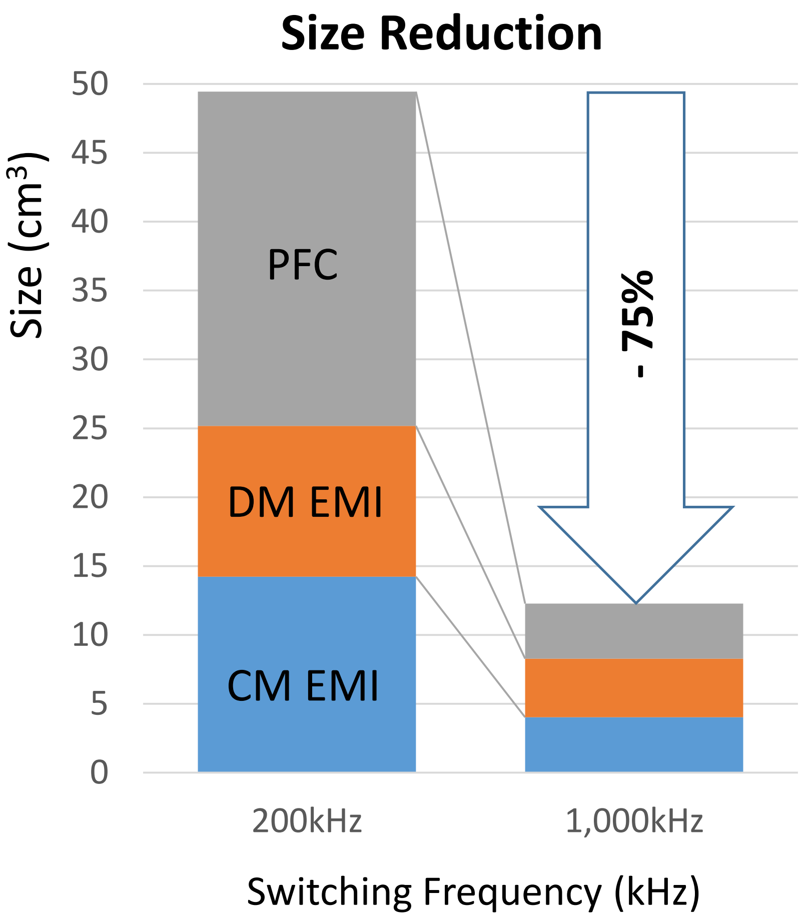
3F & 4F up to 10MHz





Magnetics:
Higher Frequency = Smaller, Cheaper

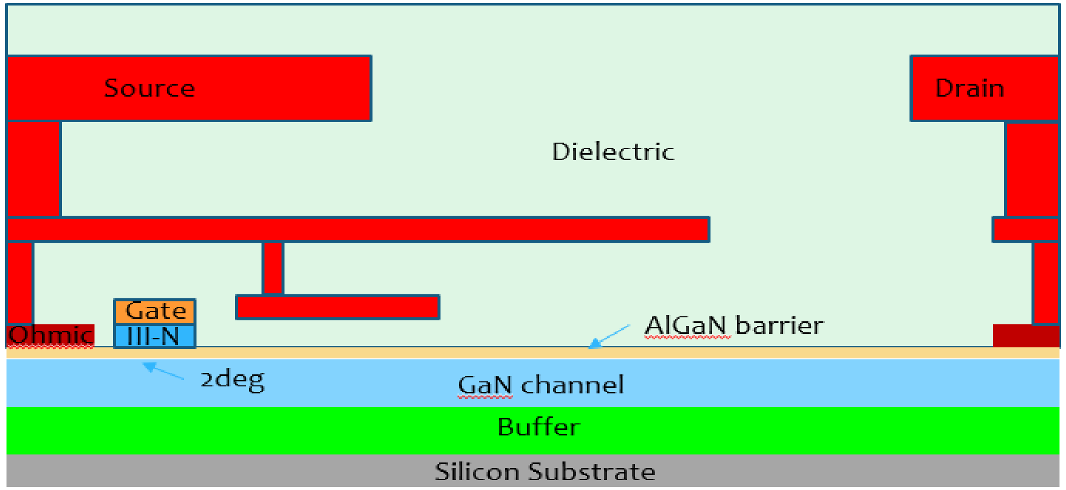


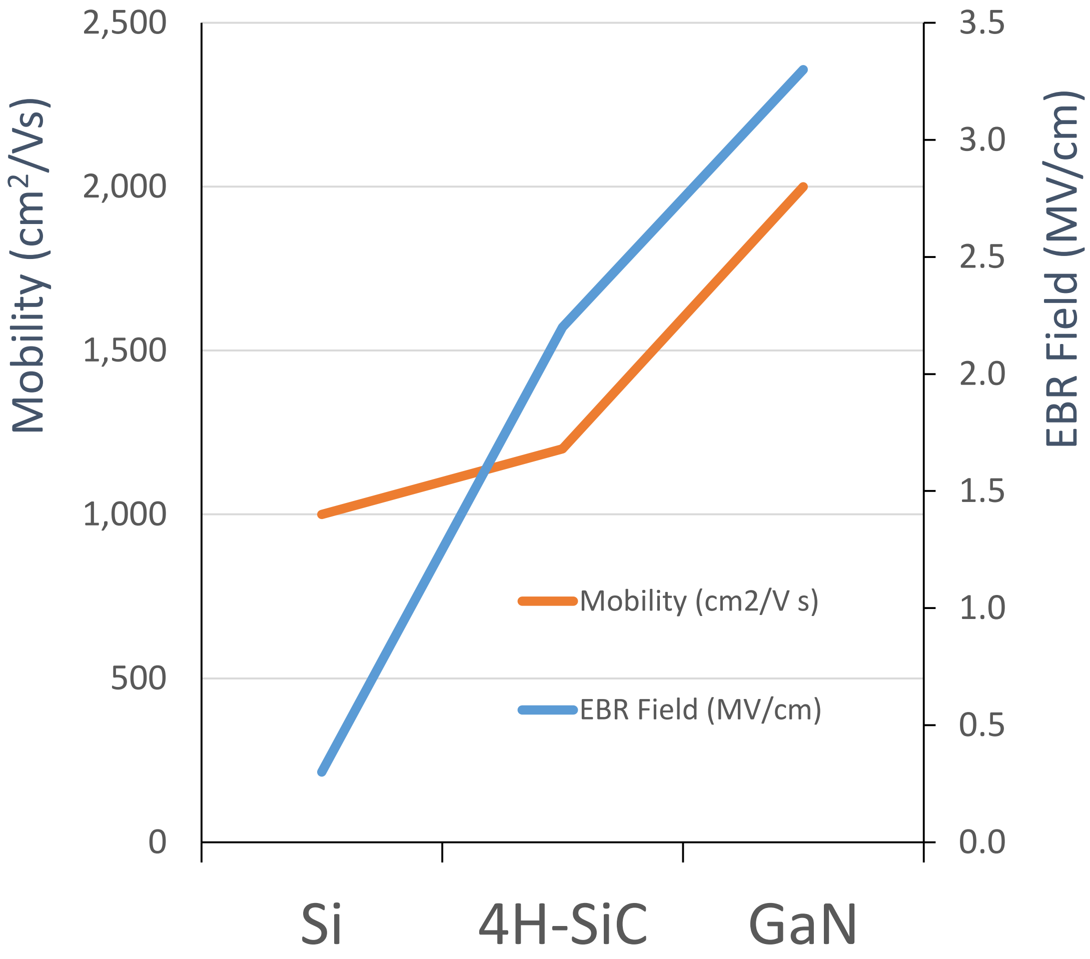


Switch:

Physics Drives Switch Performance

- WBG GaN material allows high electric fields so high carrier density can be achieved
- Two-dimensional electron gas with AlGaN/GaN heteroepitaxy structure gives very high mobility in the channel and drain drift region
- Lateral device structure achieves extremely low Q_g and Q_{OSS} and allows integration



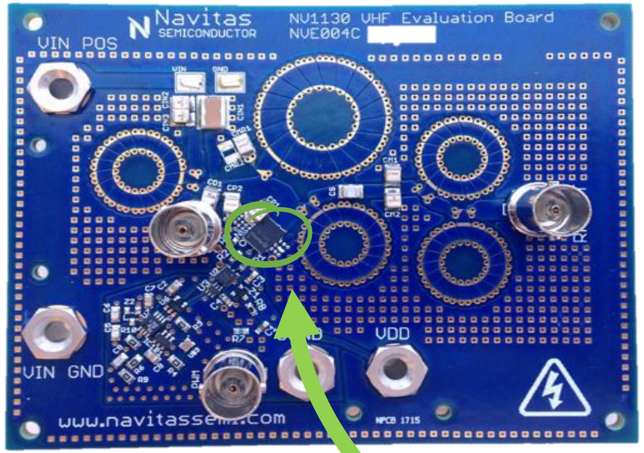


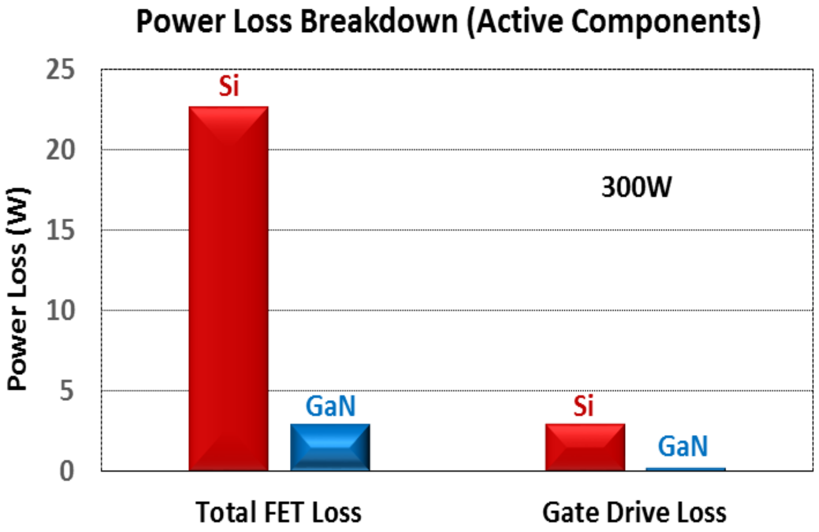
Switch:

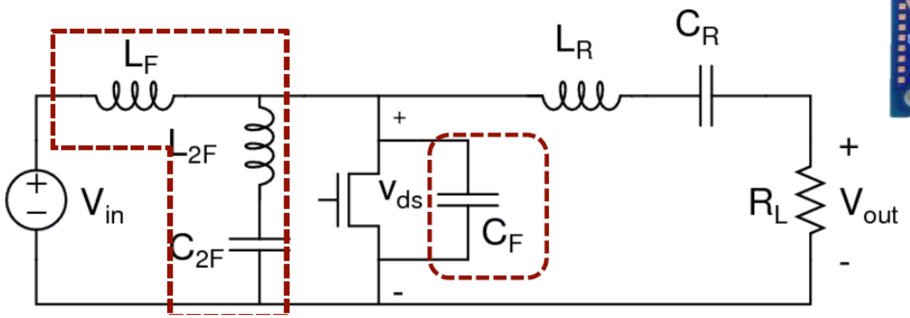
650V eMode GaN at 27MHz & 40MHz

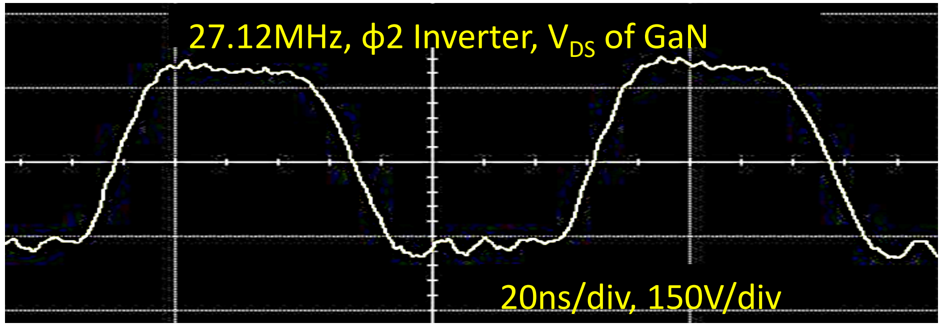
Class Phi-2 DC/AC converter: Stanford / Navitas demo

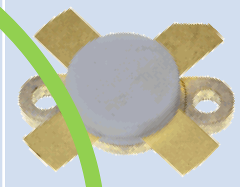
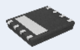
- 50% less loss than RF Si
- 16x smaller package
- Air-core inductors
- Minimal FET loss
- Negligible gate drive loss







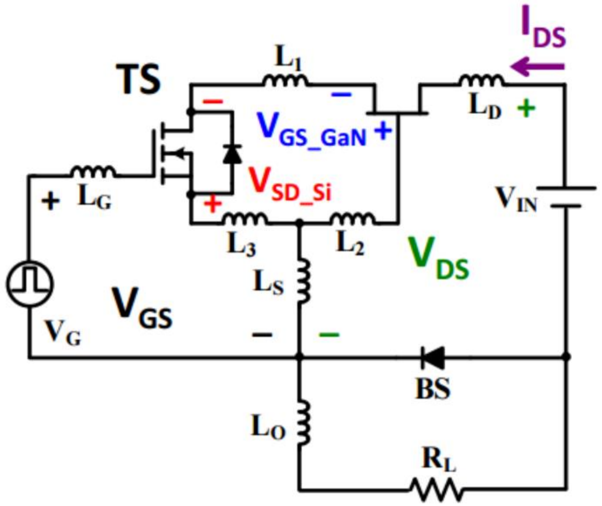


Technology	V	Pack (mm)		F_{SW} (MHz)	Eff. (%)	Power (W)
RF Si (ARF521) Microsemi POWER PRODUCTS GROUP	500	M174 22x22		27.12	91%	150
eMode GaN Navitas	650	QFN 5x6		27.12	96%	150
				40.00	93%	115

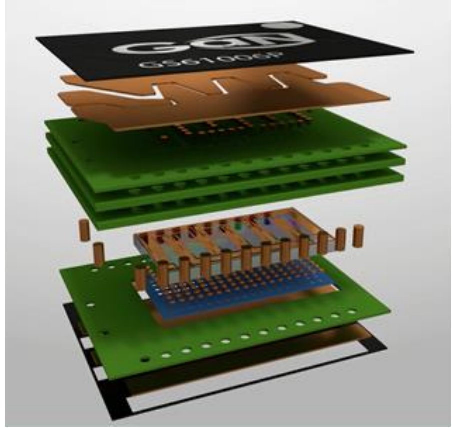
Package / Drive:

Early GaN

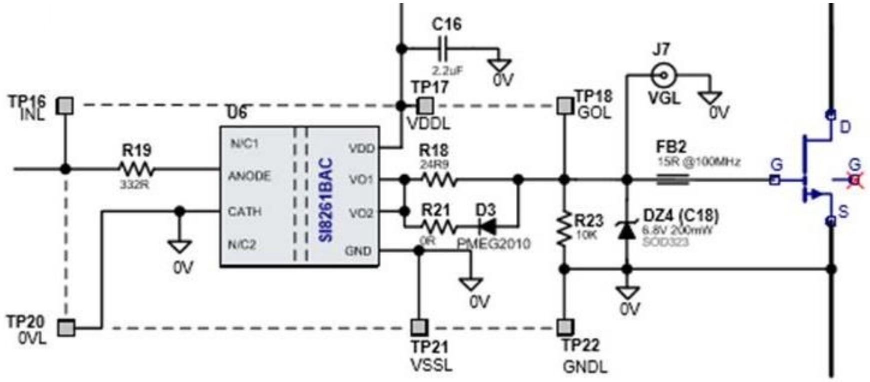
Cascoded dMode Parasitics



Complex
Embedded eMode



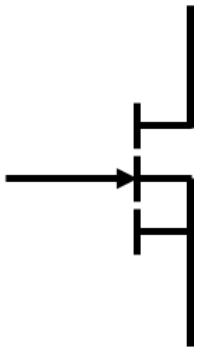
Complex eMode discrete drive



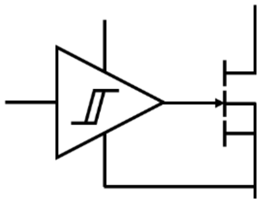
From GS66508T-EVBHB 650V GaN E-HEMT Half Bridge Evaluation Board

Creating the World's First AllGaN™ Power ICs

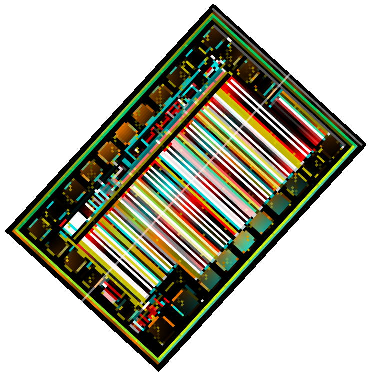
Fastest, most efficient GaN Power FETs



First & Fastest Integrated GaN Gate Driver



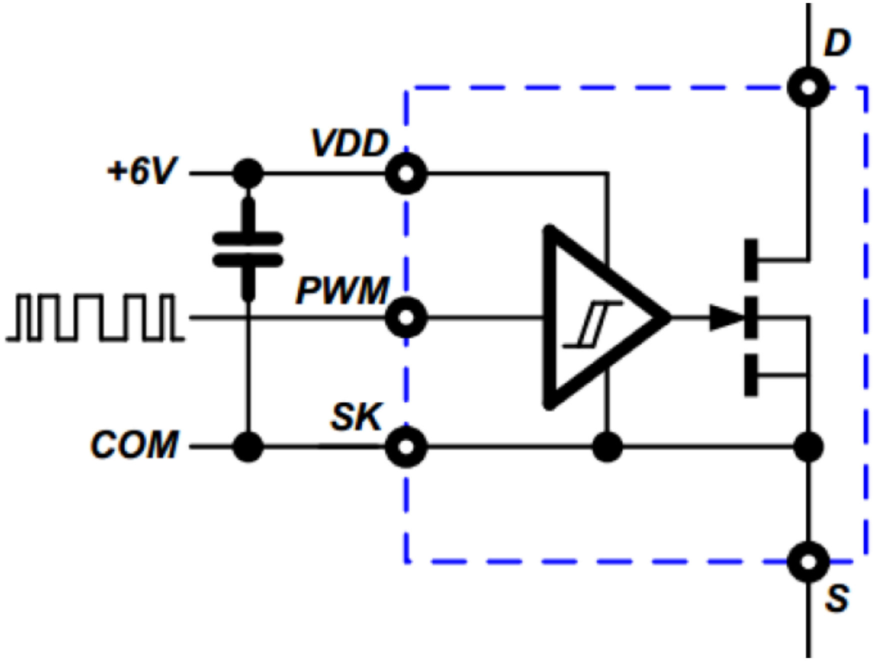
World's First AllGaN™ Power IC

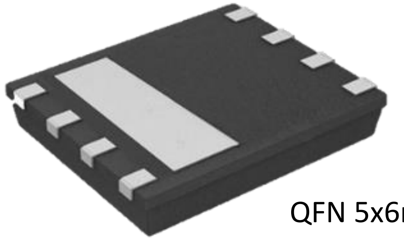


Up to 40MHz switching, 4x higher density & 20% lower system cost

Navitas GaN Power IC

- **Monolithic** integration
- 20x lower drive loss than silicon
- Driver impedance matched to power device
- Shorter prop delay than silicon (10ns)
- Zero inductance turn-off loop
- Digital input (hysteretic)
- Rail-rail drive output
- Layout insensitive



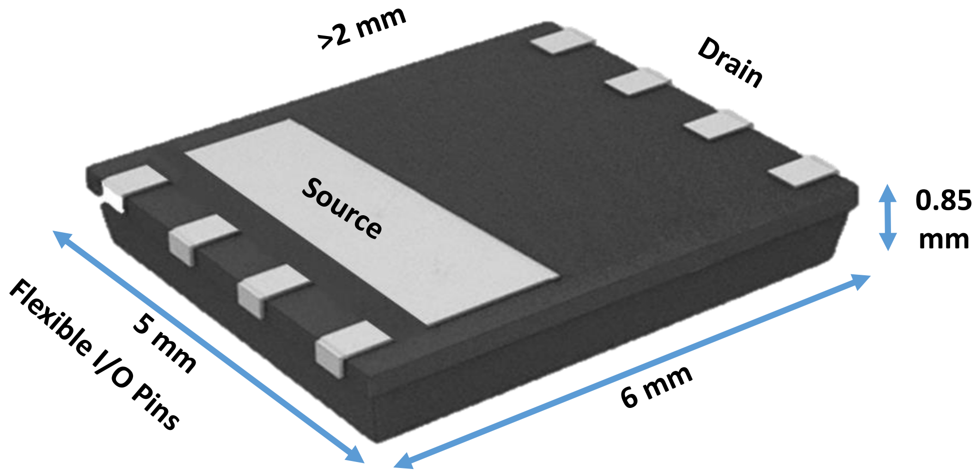


QFN 5x6mm

Package:

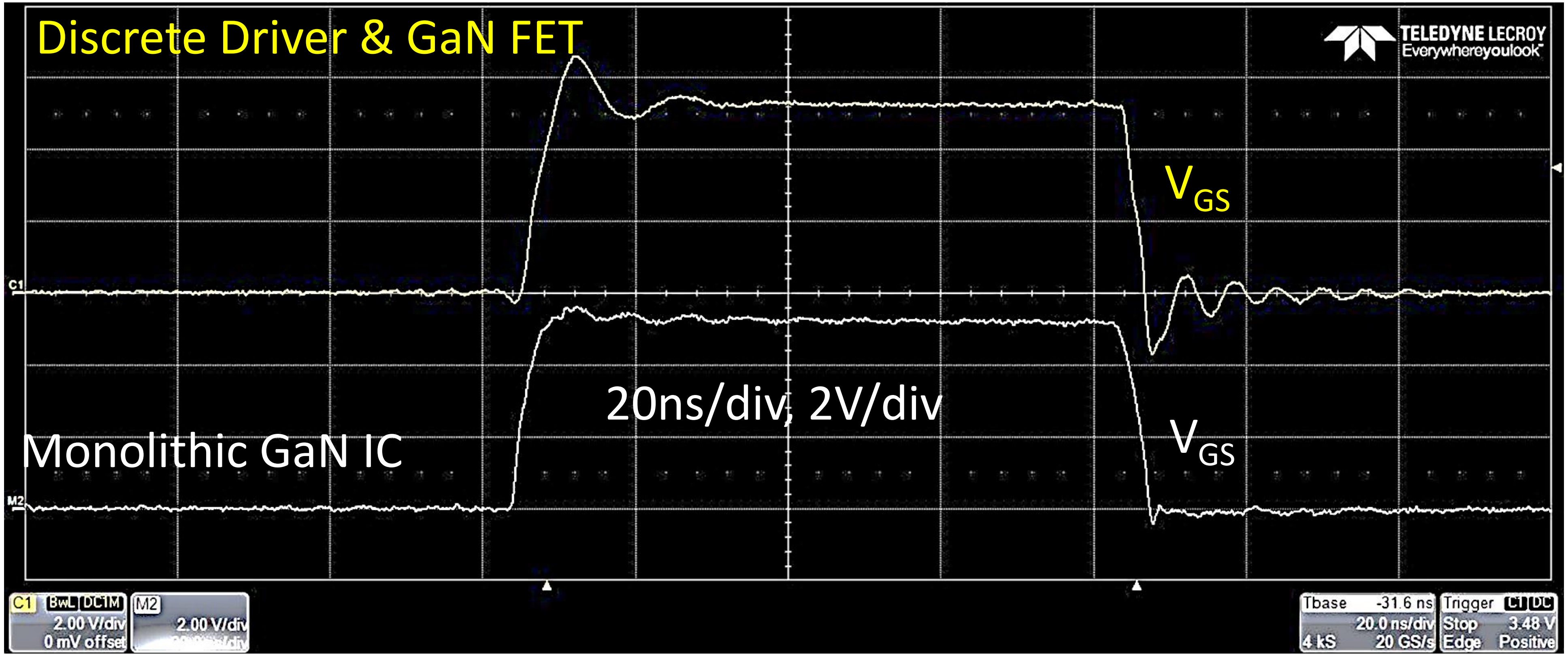
Fast, Low Cost, Industry-Standard QFN

- Leadframe-based 5x6mm power package outline
- Low profile, small footprint <u>with</u> HV clearance
- Kelvin source connection for gate drive return
- Low inductance power connections (~0.2nH)
- Low thermal resistance (<2^{o}C/W)
- I/O pins enough for drive functions
- High volume, reliable, low cost



Crisp & Efficient Gate Control

- Eliminates gate overshoot and undershoot
- Zero inductance on chip insures no turn-off loss



Topology:

Hard-Switch

Primary Switch Power Loss:

$$P_{FET} = P_{COND} \qquad + P_{DIODE} + P_{T\text{-}ON} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

Topology:

Hard-Switch → Soft-Switch

Primary Switch Power Loss:

$$P_{FET} = P_{COND} * k \quad + P_{DIODE} + \cancel{P_{T\text{-}ON}} + P_{T\text{-}OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

- k-factor >1 due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓2-3x (silicon devices can have high C_{OSS} charging/discharging losses)

Topology:

Hard-Switch → Soft-Switch with eMode GaN

Primary Switch Power Loss:

Minimized Reduced

$$P_{FET} = P_{COND} * k + P_{DIODE} + \cancel{P_{T\text{-}ON}} + P_{T\text{-}OFF} + \cancel{P_{DR}} + \cancel{P_{QRR}} + \cancel{P_{QOSS}}$$

- k-factor >1 due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓10x ~~2-3x~~ (GaN C_{OSS} charging/discharging loss negligible up to 2MHz)
- P_{DRIVER} ↓10x (GaN P_{DR} negligible up to 2MHz)
- P_{QRR} = 0
- P_{DIODE} ↓2x (reverse conduction loss reduced by synchronous rectification)
- $P_{T\text{-}OFF}$ = Reduced (limited by I-V crossover loss due to drive loop impedance)

Topology, Switch, Drive:

Hard-Switch → Soft-Switch with GaN Power IC

Primary Switch Power Loss:

Minimized Minimized

$$P_{FET} = P_{COND} * k + P_{DIODE} + \cancel{P_{T\text{-}ON}} + \cancel{P_{T\text{-}OFF}} + \cancel{P_{DR}} + \cancel{P_{QRR}} + \cancel{P_{QOSS}}$$

- k-factor >1 due to increased circulating current, duty cycle loss
- $P_{T\text{-}On}$ = 0 (soft-switch)
- P_{Qoss} ↓10x ~~2-3x~~ (GaN C_{OSS} charging/discharging loss negligible up to 2MHz)
- P_{DRIVER} ↓10x (GaN P_{DR} negligible up to 2MHz)
- P_{QRR} = 0
- P_{DIODE} ↓3x ~~2x~~ (synchronous rectification with improved dead-time control)
- $P_{T\text{-}OFF}$ = 0 ~~Reduced~~ (near-zero drive loop impedance with integration)

>10x frequency increase possible with higher efficiencies

Control ICs:

MHz Controllers … with more, faster to come

PFC (BCM):
- L6562 (1MHz)
- NCP1608 (1MHz)
- UCC28061 (500kHz)

DC-DC (LLC):
- NCP1395 (1.2MHz)
- FAN7688 (500kHz) (+SR)
- ICE2HS01G (1MHz)

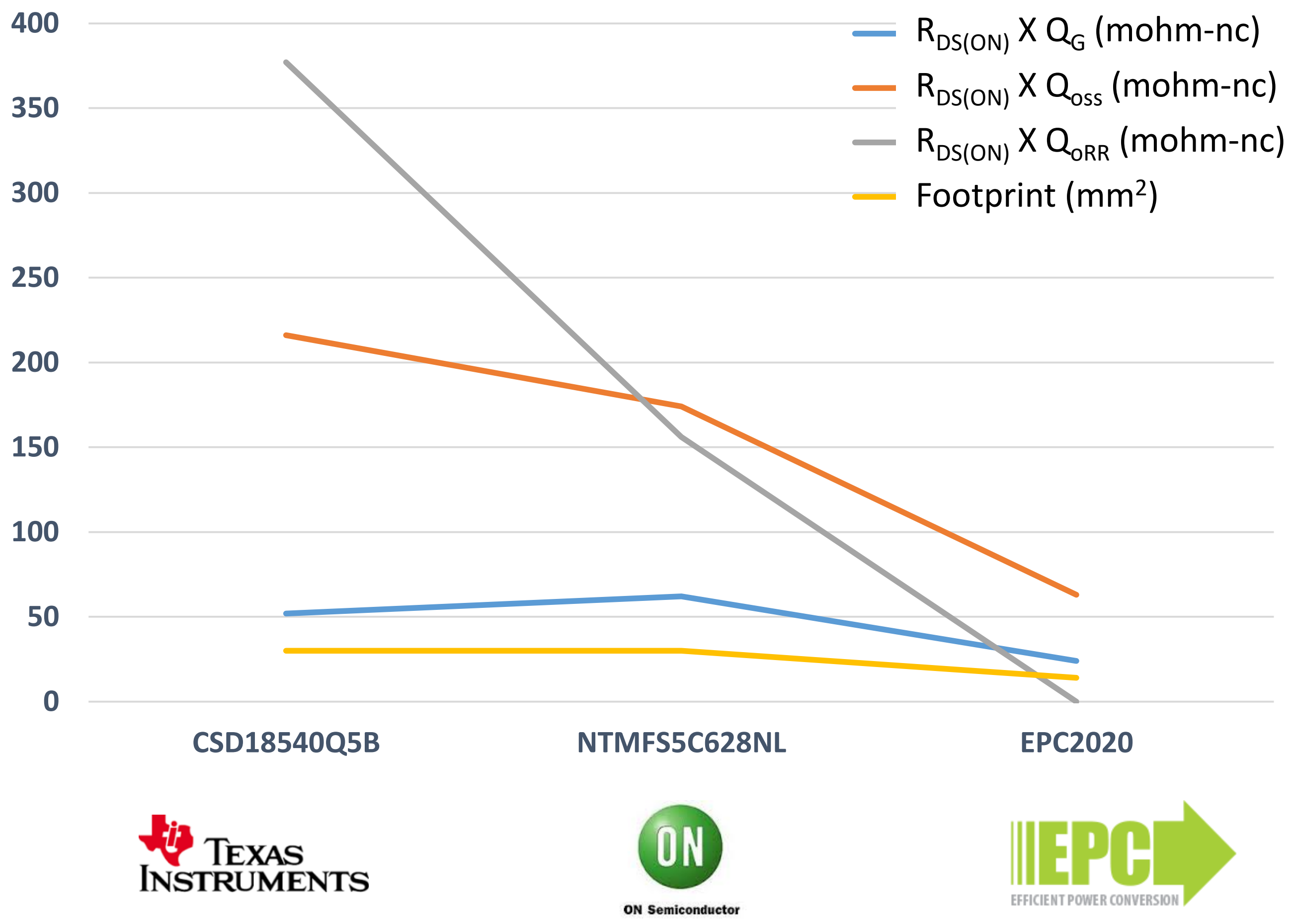
DC-DC (Sync Rectifier):
- NCP4305 (1MHz)
- UCC24610 (600kHz)

PWM:
- NCP1252 (500kHz)
- NCP1565 (1.5MHz)
- UCC28C44 (1MHz)
- UCC25705 (4MHz)

DSP
- UCD3138 (2MHz)
- dsPIC33xx (5MHz)
- ADP1055 (1MHz)

SR FETs: Better with GaN

- All relevant FsOM favor GaN at 60V
  - $R_{DS(ON)}$ x Q_G reflects drive losses
  - $R_{DS(ON)}$ x Q_{OSS} reflects turn-off losses with non-resonant rectification
  - $R_{DS(ON)}$ x Q_{RR} reflects stored minority carrier turn-off losses (minimized with dead-time control)
- Si in QFN 5x6mm, GaN is Chip-Scale BGA

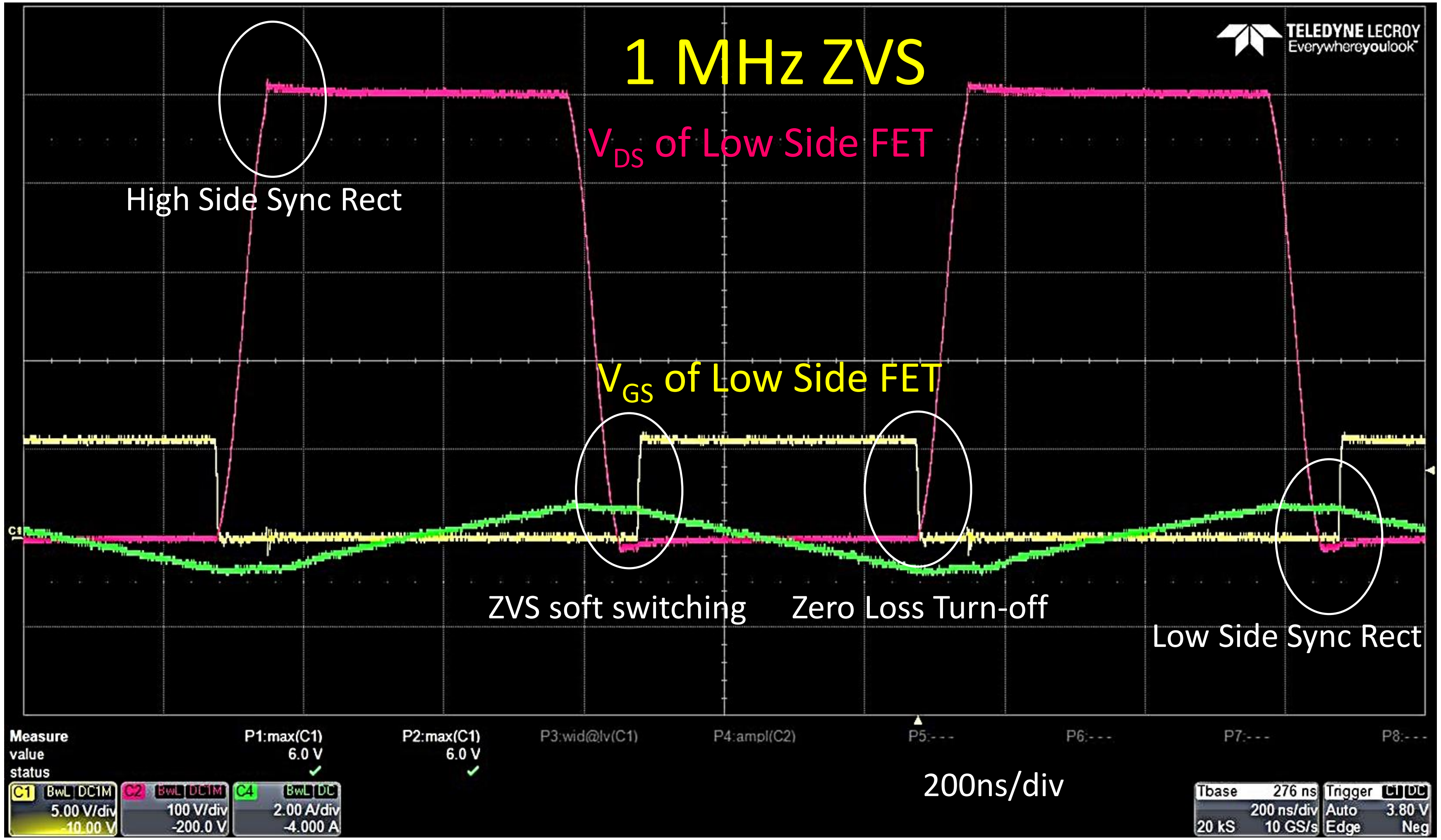


Note: Datasheet typicals at 4.5/5V gate drive and capacitance curves

Magnetics (EMI):

Smooth, clean, controlled waveforms

- 500V Switching
- No overshoot / spike
- No oscillations
- 'S-curve' transitions
- ZVS Turn-on
- Zero loss turn-off
- Sync rectification
- High frequency
- Small, low cost filter



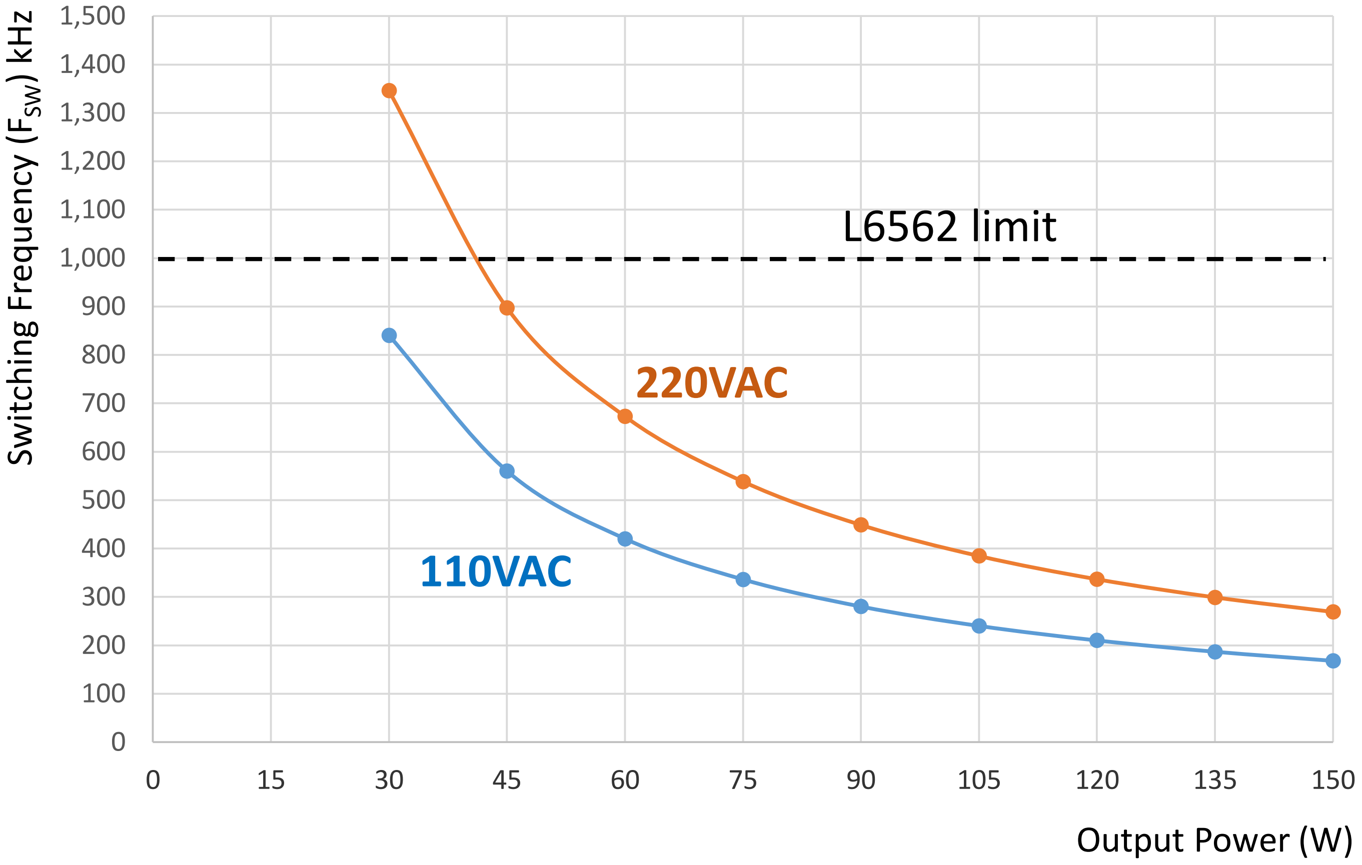
Topology:

Critical Conduction Mode (CrCM) PFC

- CrCM PFC enables ZVS / QR operation
  - Also known as Boundary Conduction Mode (BCM)
  - Ideal for high frequency
  - Uses slower, lower cost diode than in Continuous Conduction Mode (CCM)
  - Peak current ‘OK’ up to ~300W per phase (can interleave for higher power)
- Operating frequency varies with:
  - AC input voltage, output power, AC line cycle
- ‘Nominal’ frequency specified as:
  - $220V_{AC}$, full load, peak of the AC line

PFC Frequency vs. Power

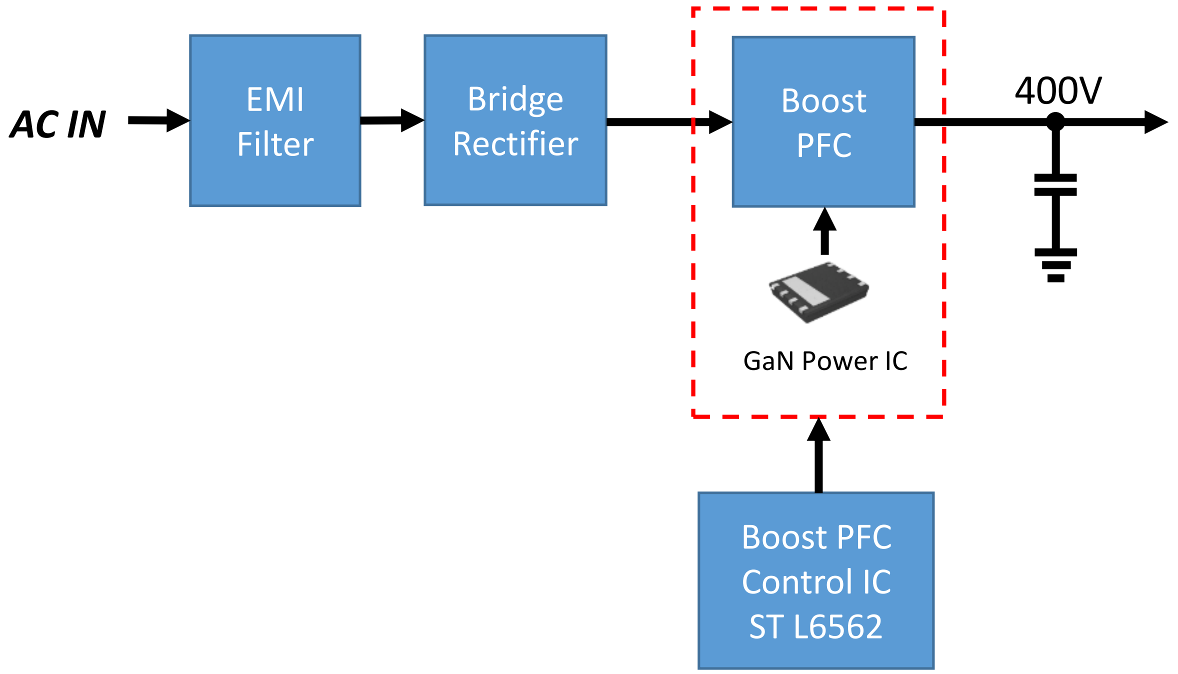
- Calculated CrCM example to show frequency trend
- 150W PFC Boost
  - Assume L6562 controller
  - Nominal frequency = 270kHz
    ($220V_{AC}$, full load, peak of the AC ine)
  - Maximum frequency = 1MHz
    (controller limit)

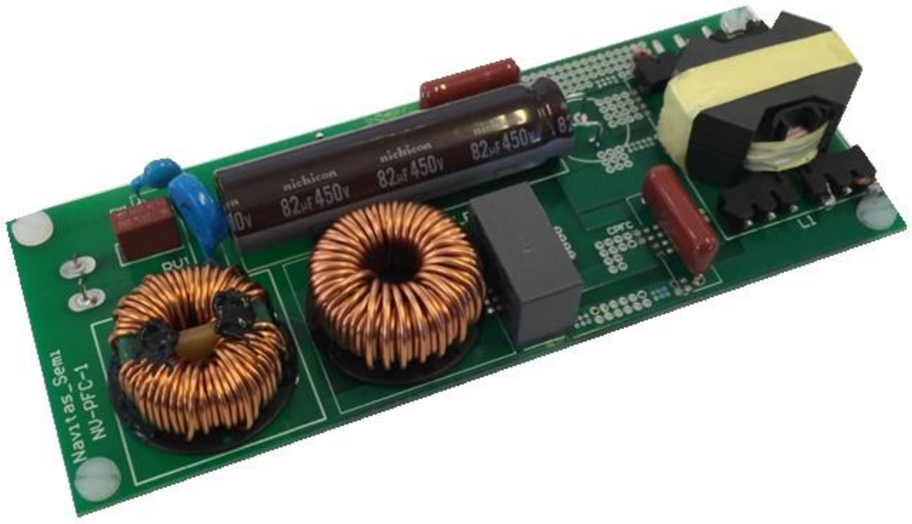


150W CrCM Boost PFC

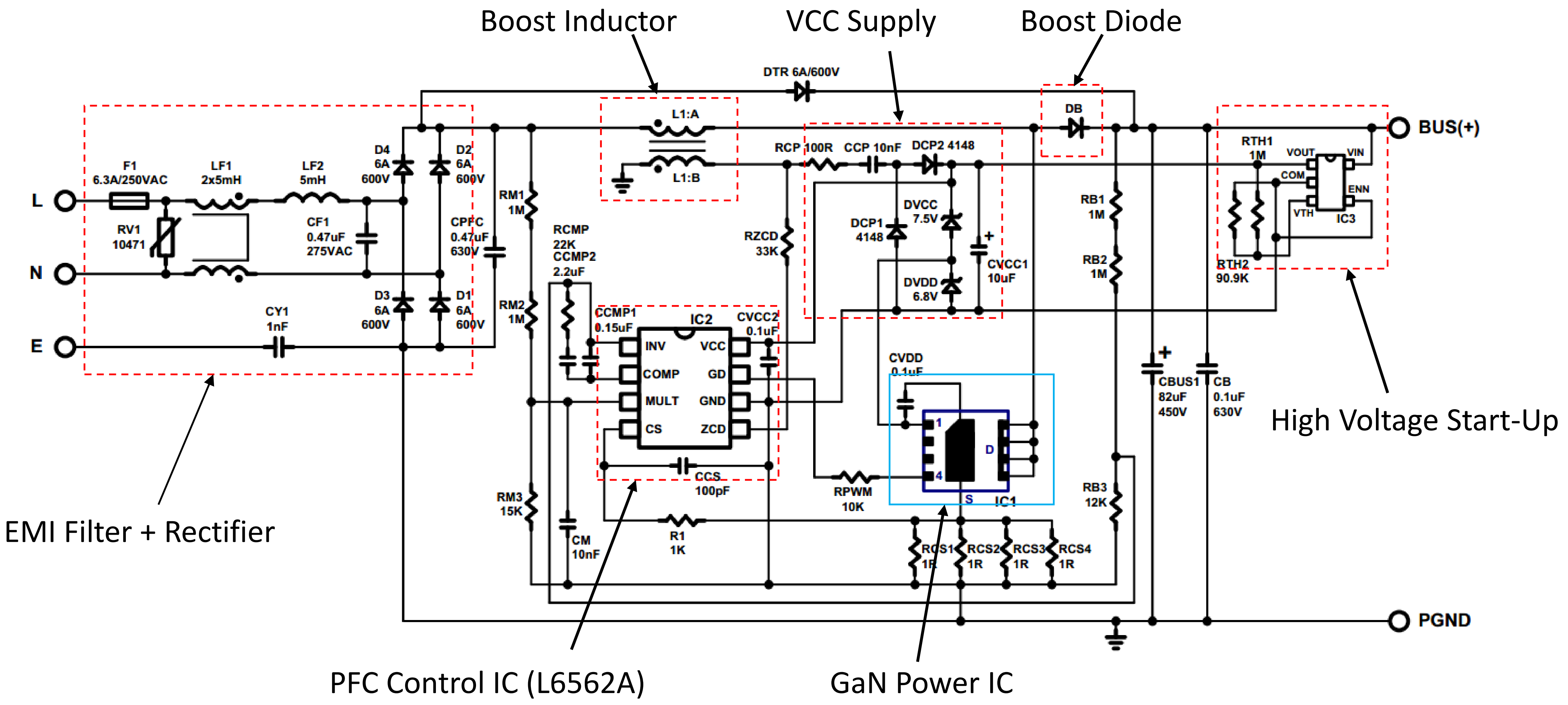
- Input : Universal AC (85-265V_{AC}, 47-63Hz)
- Output : 400V, 0.27A (150W)
- Frequency* : 120V = 167-230kHz
  : 220V = 230-500kHz
  : 265V = 1MHz
- **limited by control IC (L6562A)*

- Efficiency : >98% peak, >97.1% average (25%, 50%, 75%, 100% load)
- Power Factor : >0.995
- Demo Size : 100 x 50 x 20mm *"No heatsink" design*
- Construction : 2-layer PCB, SMT powertrain on bottom side





150W PFC:
Schematic



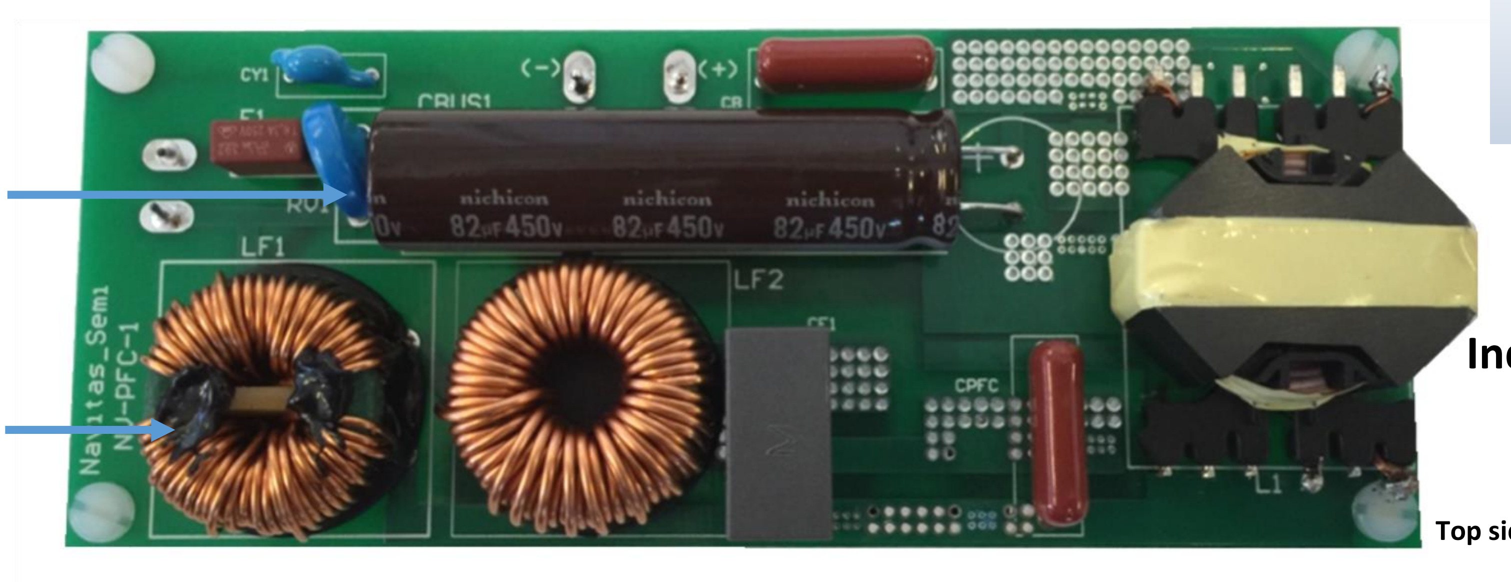
150W PFC:

Layout

- All active semiconductors on bottom-side
  - Low profile
  - 'No-heatsink' design
- 100 x 50 x 20mm

Bulk Cap

EMI Filter



PFC Inductor

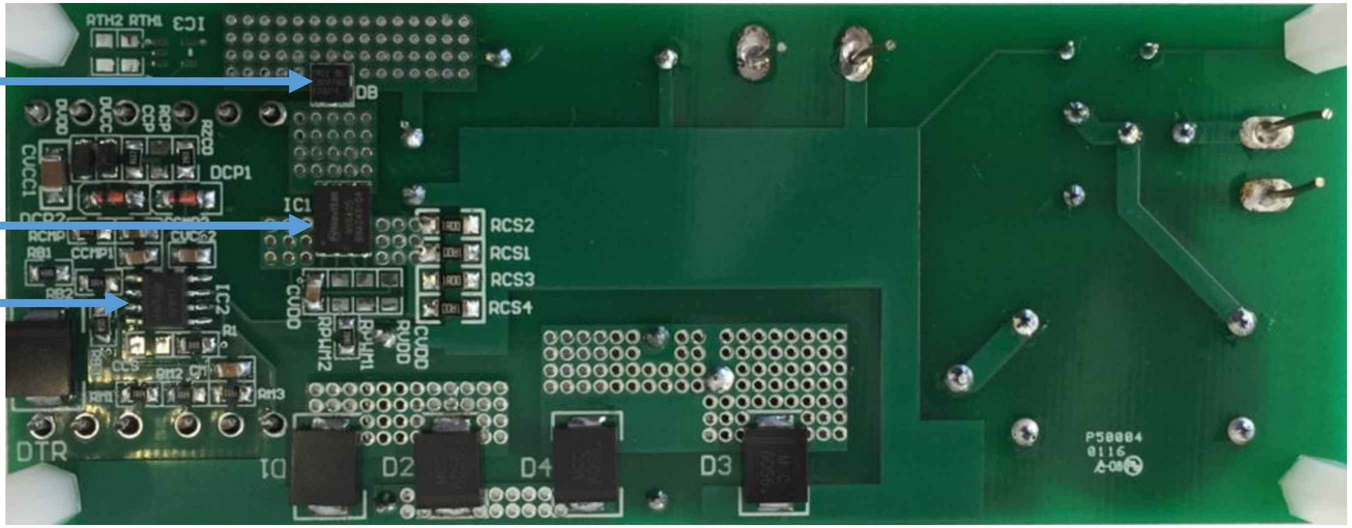
Top side

Bottom side

PFC Boost Diode

GaN Power IC

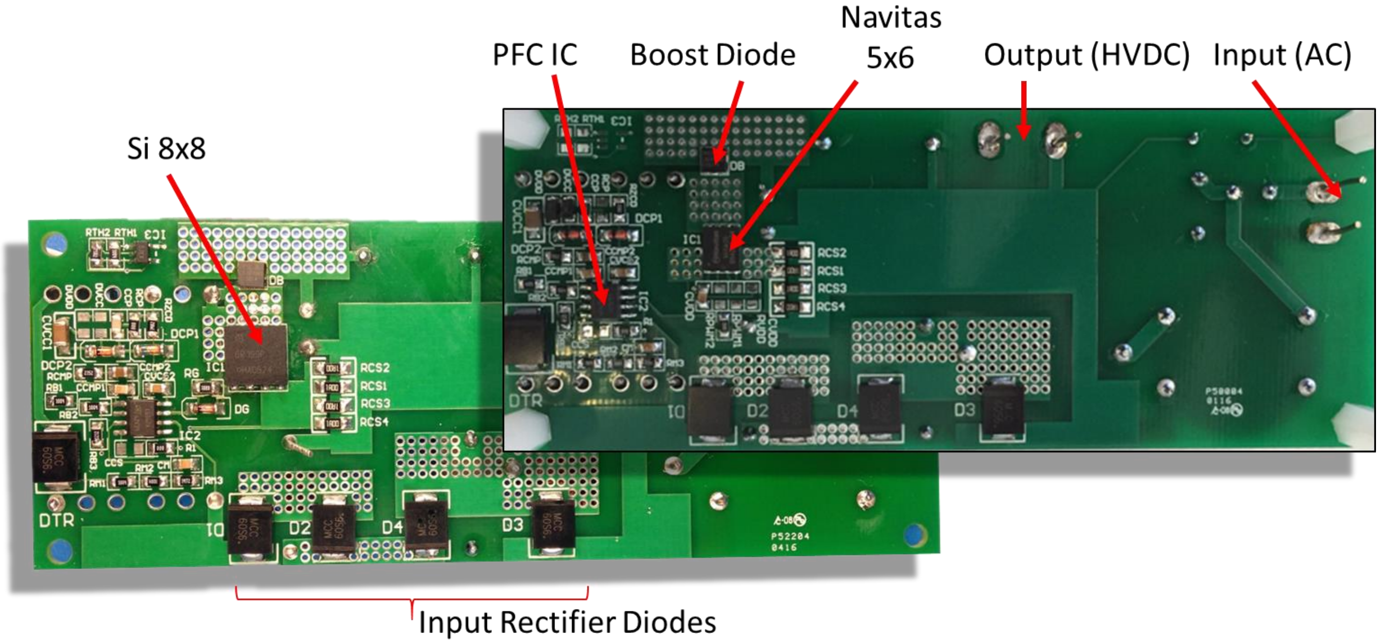
L6562A PFC Control IC



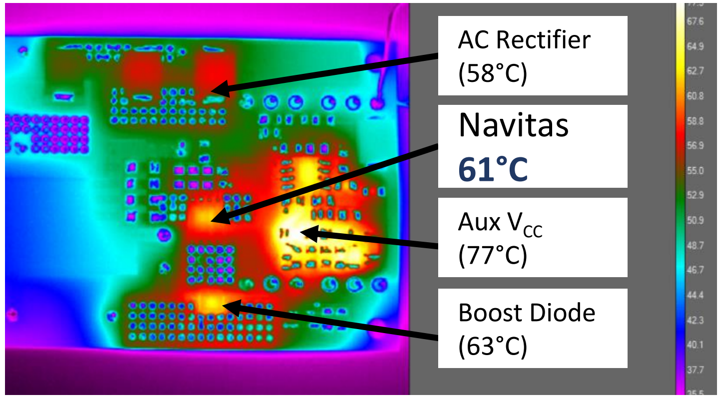
AC Bridge Rectifier

150W PFC:
SuperJunction Si vs. GaN Power IC

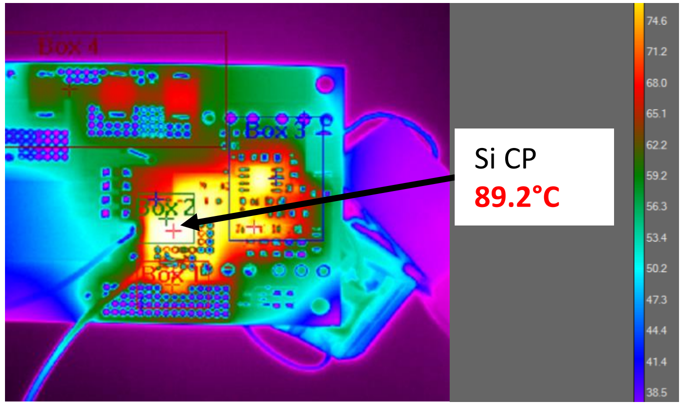
	Pack	$R_{DS(ON)}$ mΩ	Q_G nC	$C_{OSS}(er)$ pF	$C_{OSS}(tr)$ pF	$R*Q_G$ mΩ.nC	$R*C_{OSS}(tr)$ mΩ.pF	$R*C_{OSS}(er)$ mΩ.pF
Navitas	5x6	160	2.5	30	50	400	8,000	4,800
IPL65R199CP	8x8	180	32	69	180	5,760	32,400	12,400
IPL60R130C7	8x8	115	35	53	579	4,025	66,600	6,100
GaN Benefits	**>50%**	**n/a**	**>10x**	**>2x**	**>10x**	**>10x**	**>7x**	**>2.5x**



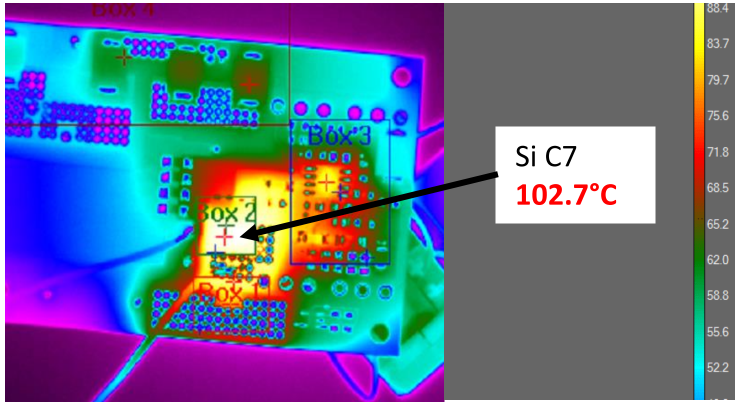
Full Load FET Temperature



$220V_{AC}$, 150W



$220V_{AC}$, 150W



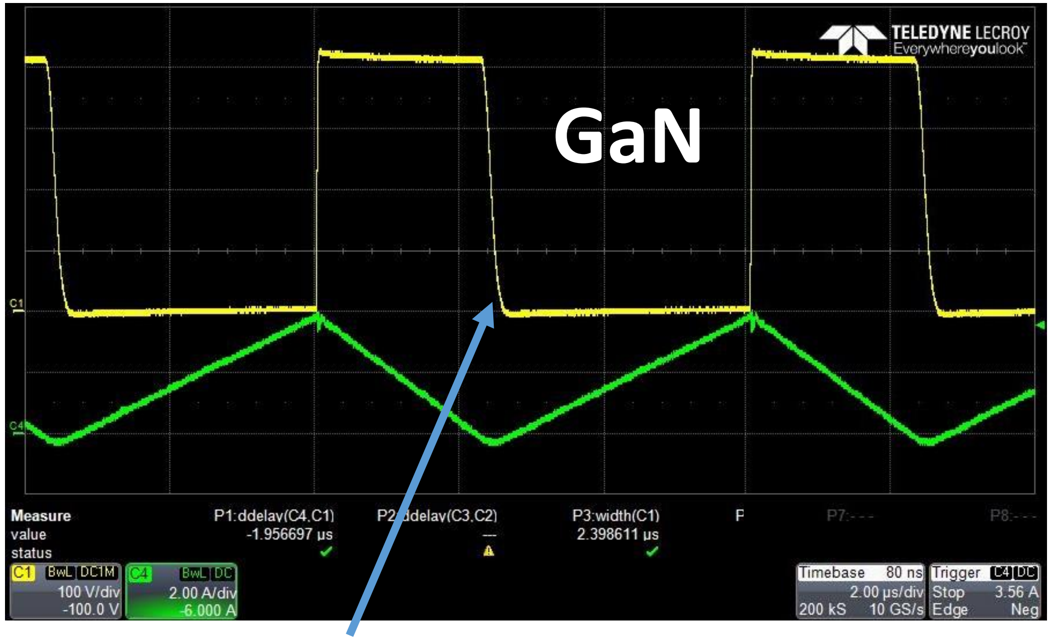
$180V_{AC}$, 150W

- GaN running cool (61°C)
  - Efficiency up 1% vs. Si CP
  - Loss 20-35% lower
  - Power Factor >99.5%

- CP Si running >90°C
- C7 Si too hot to run at $220V_{AC}$

Silicon's High C_{OSS} Creates Partial ZVS

120V_{AC}, Si CP partial hard-switching (~200kHz)

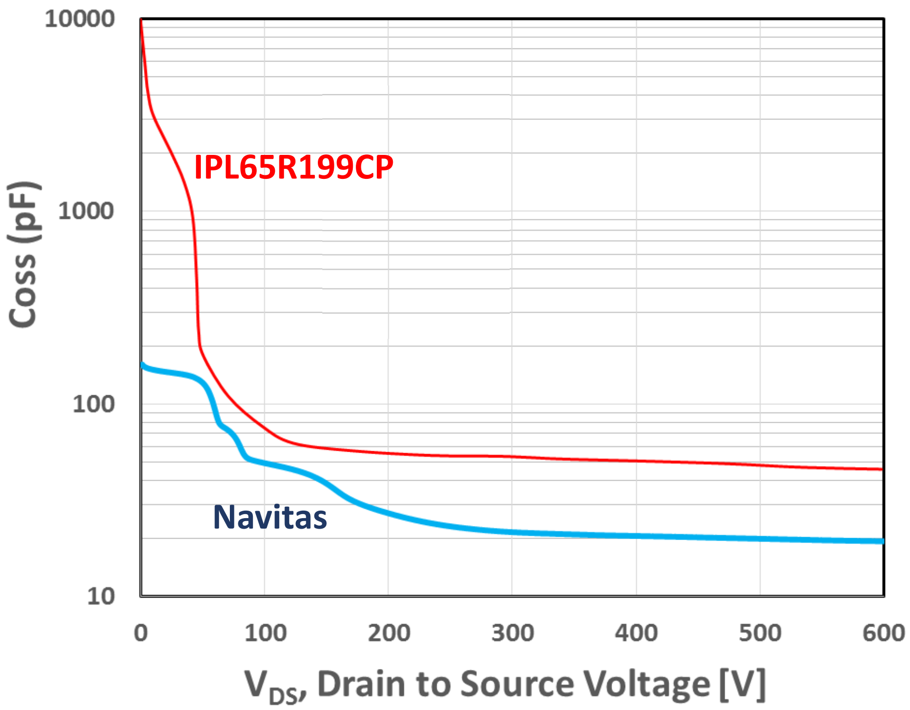


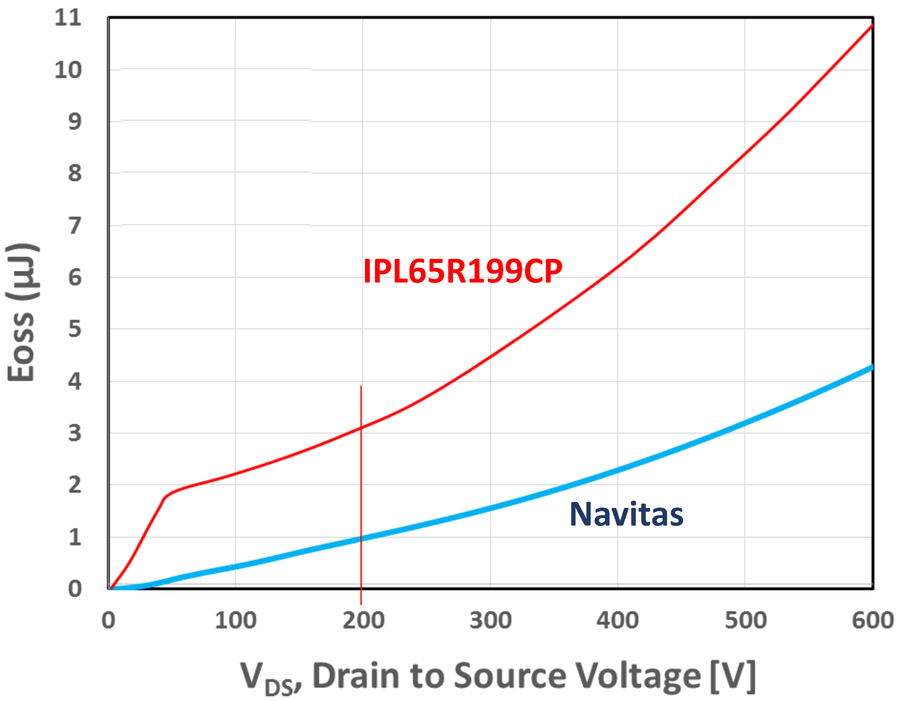
120V_{AC}, GaN clean ZVS waveforms (~200kHz)

- High loss due to large stored charge while hard-switching
- Si C_{OSS} is 50x-100x worse than GaN at V_{DS} < 30V

- Turn-off losses low due to integrated drive
- Near loss-less ZVS turn-on transition
- Minimize deadtime for low reverse conduction loss
- No voltage spikes / overshoot

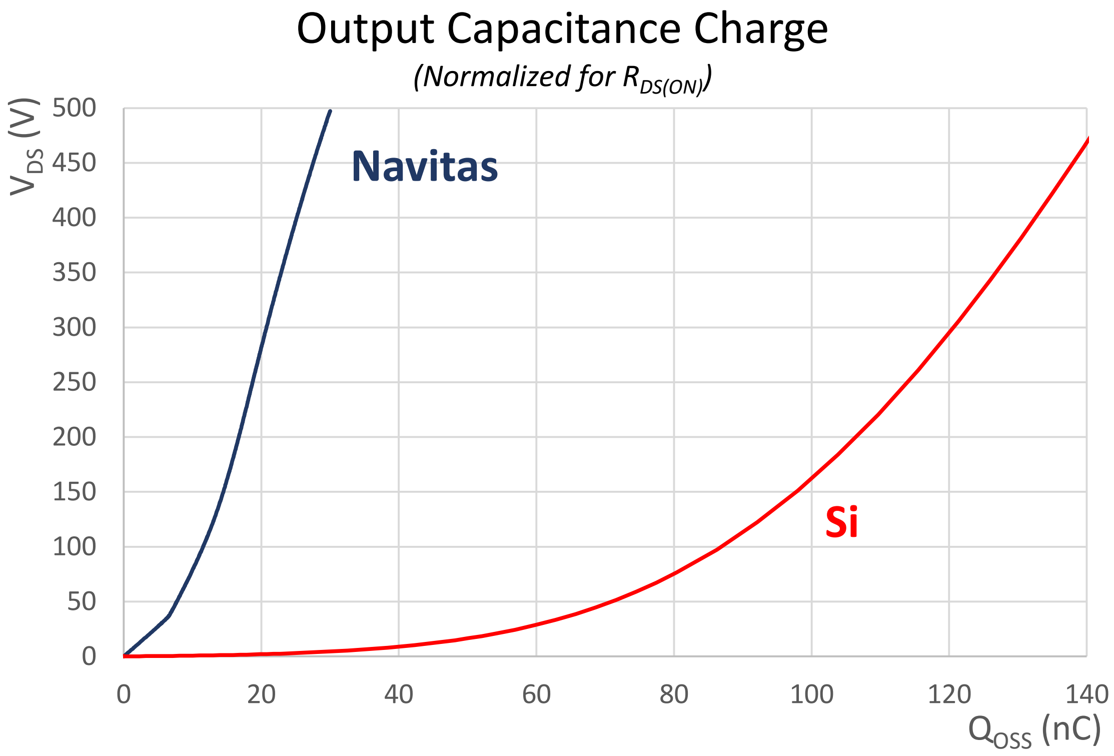
Critical Parameters: C_{OSS} , E_{OSS}

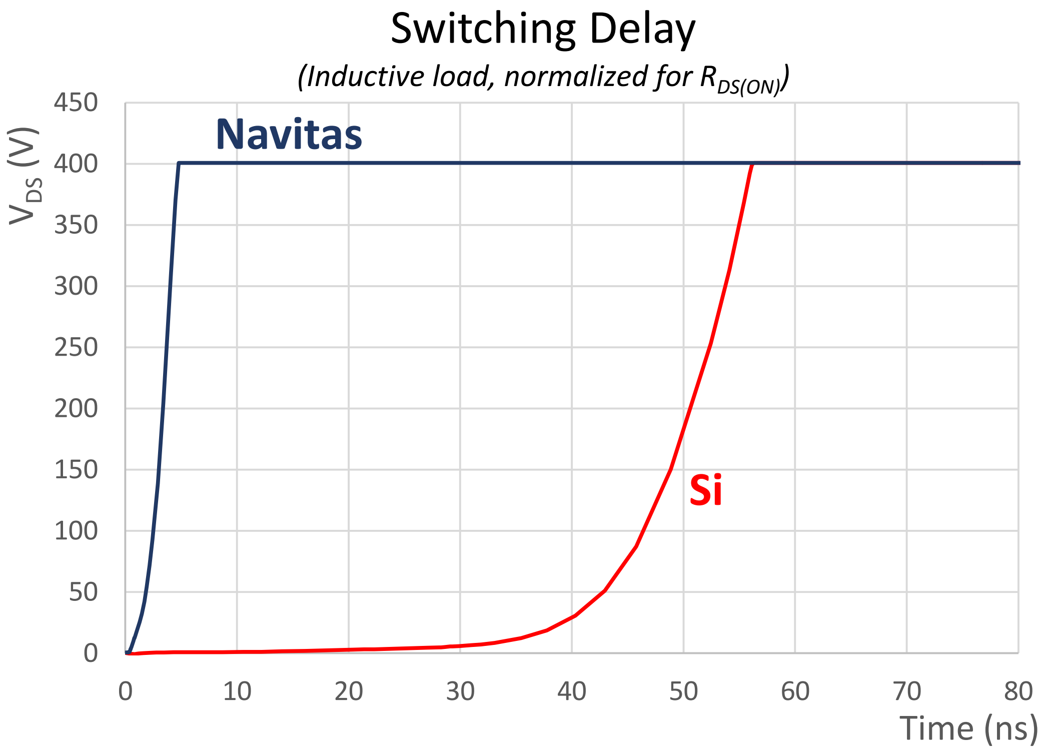




- Q_{OSS} charge affects ZVS transition time and E_{OSS} under partial ZVS condition
- Switching loss: $P_{LOSS} = E_{OSS} (V_{DS}) * F_{SW}$
  - Si has 3x higher loss than GaN at 200V (partial ZVS) - big effect at full or light load condition
  - CrCM boost has inherent partial ZVS at high line – so 265VAC and light load is worst case
- For more information: “C_{OSS} Hysteresis in Advanced Superjunction MOSFETs“, Harrison, APEC 2016

Long Si ZVS Transition Time = Trapped Energy





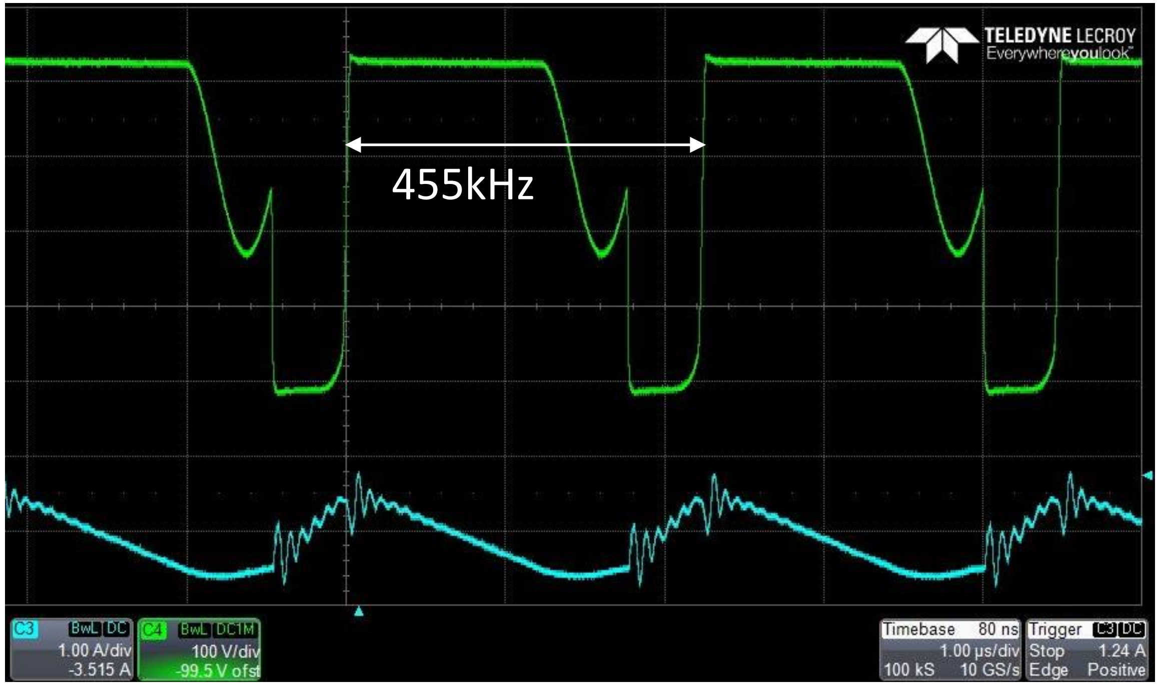
- Q_{OSS} directly proportional to transition time, which limits max frequency
- If too slow, goes into partial ZVS condition, creates **E_{OSS} loss**

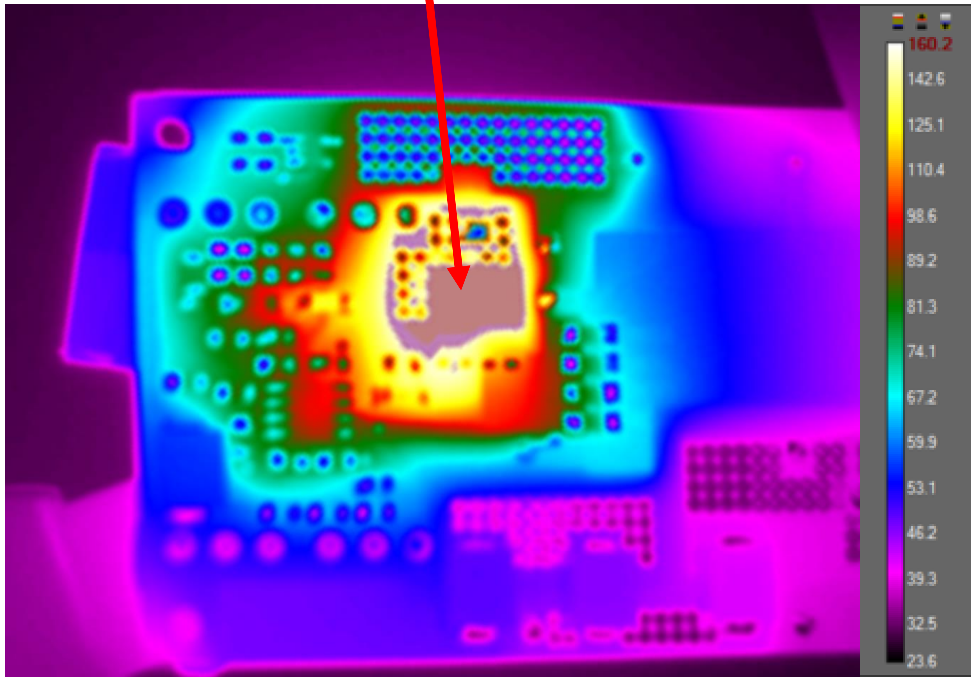
Light Load = High Frequency = High Loss for Si

Switching loss: P_{LOSS} $= E_{OSS}(V_{DS})$ *frequency (at 20W)

= 3.5uJ * 455kHz

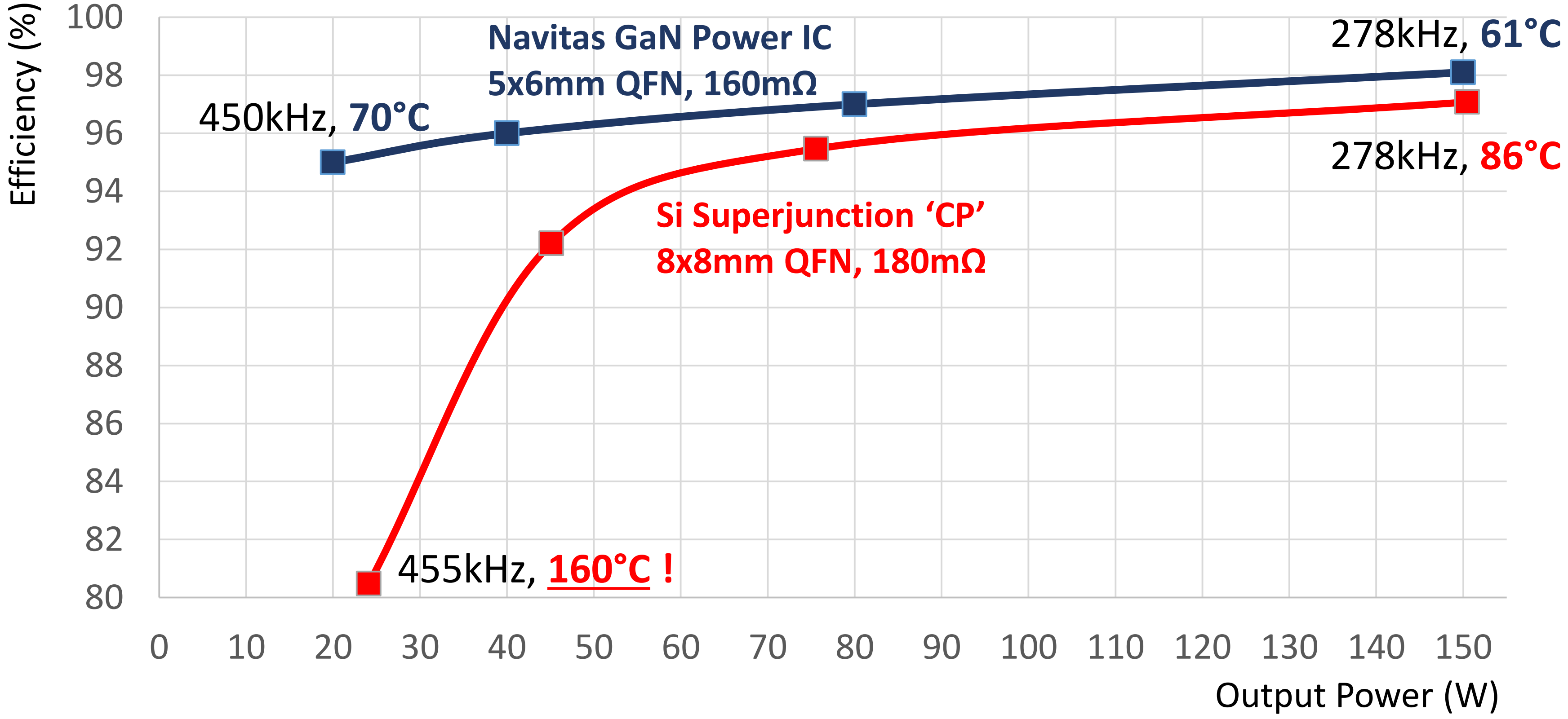
= 1.59W → = 160°C !





Light-Load = High Frequency

Hot Si, Cool GaN

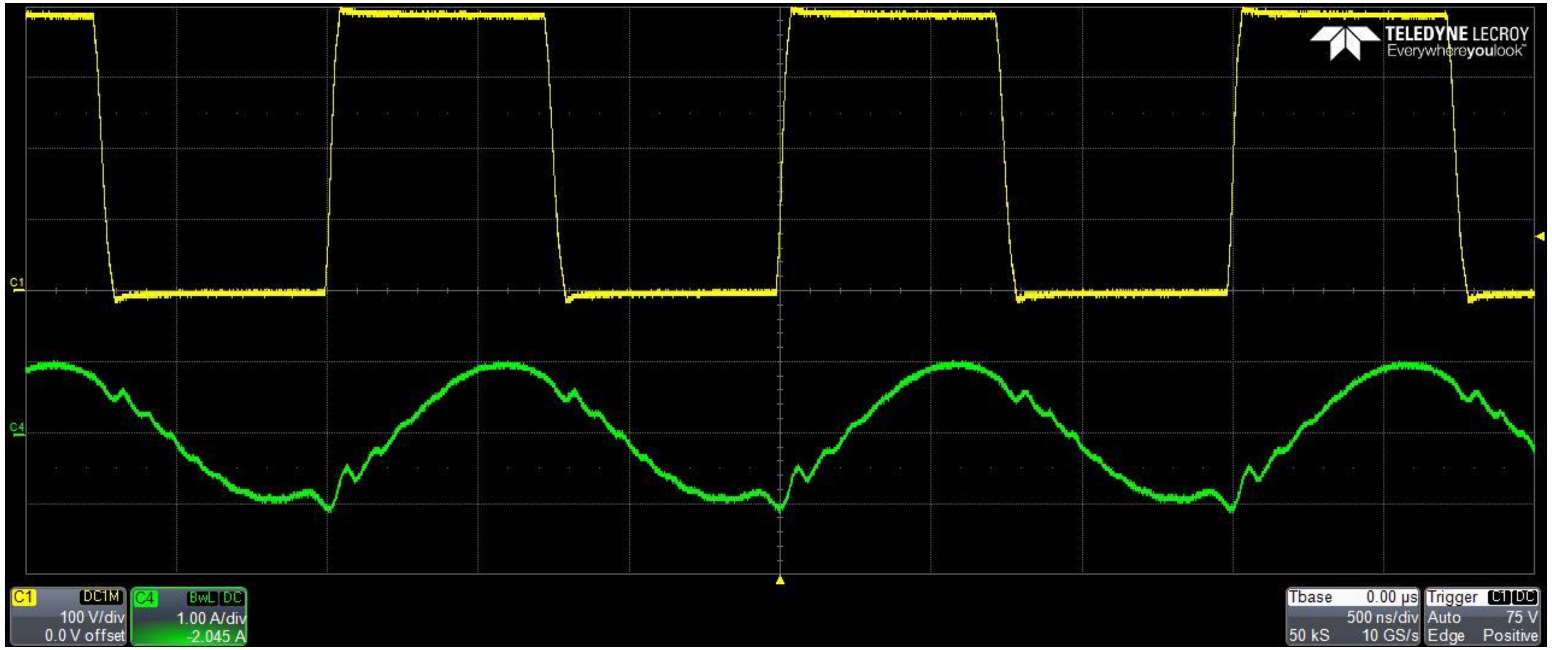


Topology:

LLC at 650kHz (400-12V)

V_{SW} (100V/div)

I_L (1A/div)

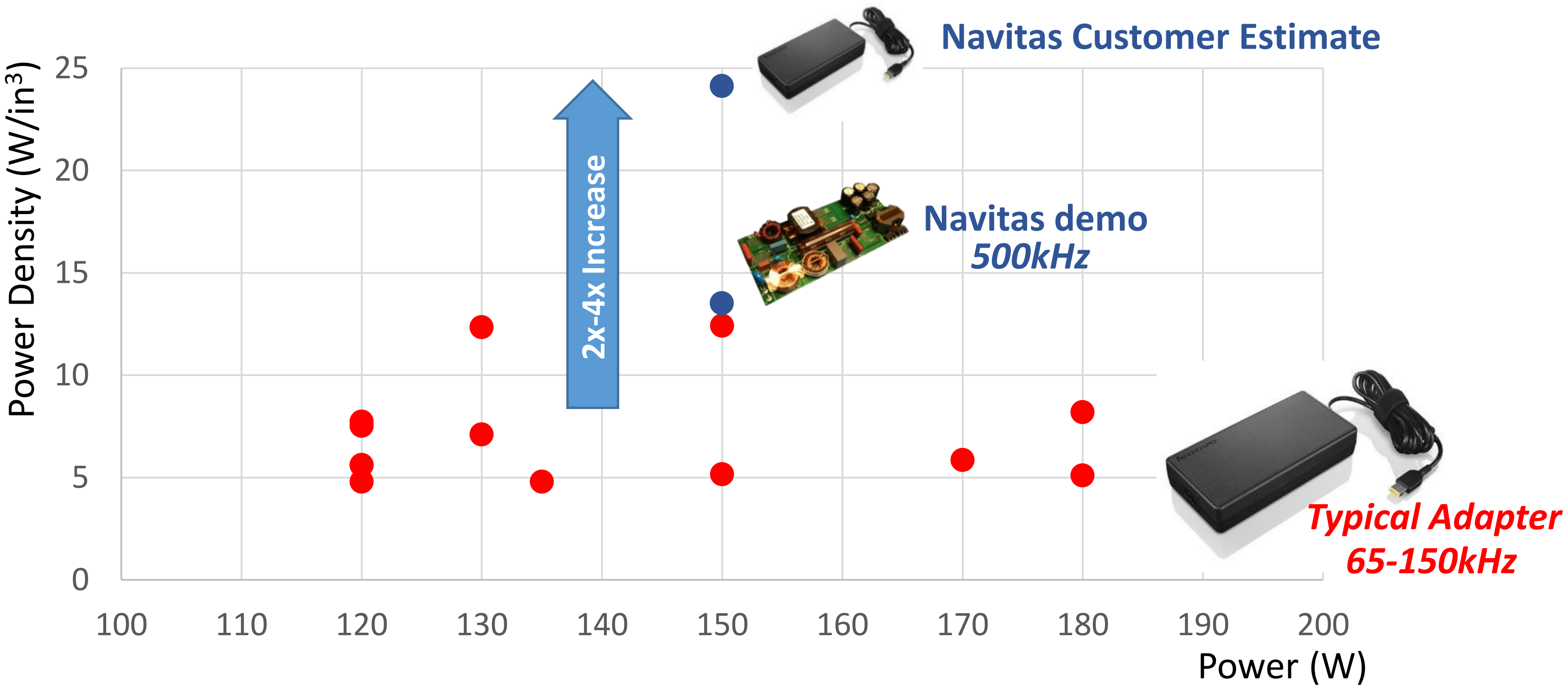


Normal Operation, 50% duty cycle, Full ZVS

Topology: PFC+LLC

Frequency drives 2x-4x Power Density

- Typical adapters (65-150kHz) = 5-12W/in^3
- Navitas demo (500kHz) = 13.5W/in^3
- Navitas customer estimate = 20-25W/in^3



Gamer Laptops (100-150W)

All-in-One PCs (150-200W)

38"-52" TVs (100-200W)

I found my Eco-System!