GaN Power ICs and the High Frequency Eco-System

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Frequency ➔ Density ➔ Efficiency

Switching Frequency

Efficiency

100kHz 1MHz 10MHz

Bulky, Heavy & Expensive

Si

Early GaN

Small, Light & Lower Cost

Navitas
Looking for an Eco-System!

Control
Switch
Package
Magnetics
Topologies
Layout
Drive

Magnetics:
Can Magnetics Rise to the Speed Challenge?

- Boundaries vary with material, DC/AC current mix, power, etc.
- Majority of mass production applications run 65kHz – 150kHz
- 5x frequency increase is within today’s capability
Magnetics:

High Frequency Magnetics ‘GaN Optimized’

N59 optimized for 2MHz

3F & 4F up to 10MHz
Magnetics:
Higher Frequency = Smaller, Cheaper

Cost Reduction

<table>
<thead>
<tr>
<th>Frequency (kHz)</th>
<th>CM EMI</th>
<th>DM EMI</th>
<th>PFC</th>
<th>Cost Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>200kHz</td>
<td>$0.10</td>
<td>$0.20</td>
<td>$0.50</td>
<td></td>
</tr>
<tr>
<td>1,000kHz</td>
<td>$0.10</td>
<td>$0.20</td>
<td>$0.30</td>
<td>-40%</td>
</tr>
</tbody>
</table>

Size Reduction

<table>
<thead>
<tr>
<th>Frequency (kHz)</th>
<th>CM EMI</th>
<th>DM EMI</th>
<th>PFC</th>
<th>Size Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>200kHz</td>
<td>50 cm³</td>
<td>35 cm³</td>
<td>20 cm³</td>
<td></td>
</tr>
<tr>
<td>1,000kHz</td>
<td>5 cm³</td>
<td>10 cm³</td>
<td>15 cm³</td>
<td>-75%</td>
</tr>
</tbody>
</table>
Switch: Physics Drives Switch Performance

- WBG GaN material allows high electric fields so high carrier density can be achieved
- Two-dimensional electron gas with AlGaN/GaN heteroepitaxy structure gives very high mobility in the channel and drain drift region
- Lateral device structure achieves extremely low $Q_g$ and $Q_{OSS}$ and allows integration
Switch:

650V eMode GaN at 27MHz & 40MHz

Class Phi-2 DC/AC converter: Stanford / Navitas demo

- 50% less loss than RF Si
- 16x smaller package
- Air-core inductors
- Minimal FET loss
- Negligible gate drive loss

<table>
<thead>
<tr>
<th>Technology</th>
<th>V</th>
<th>Pack (mm)</th>
<th>$F_{SW}$ (MHz)</th>
<th>Eff. (%)</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Si (ARF521)</td>
<td>500</td>
<td>M174 22x22</td>
<td>27.12</td>
<td>91%</td>
<td>150</td>
</tr>
<tr>
<td>eMode GaN</td>
<td>650</td>
<td>QFN 5x6</td>
<td>27.12</td>
<td>96%</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>40.00</td>
<td>93%</td>
<td>115</td>
</tr>
</tbody>
</table>

Power Loss Breakdown (Active Components)

- Si: 300W
- GaN

• 50% less loss than RF Si
• 16x smaller package
• Air-core inductors
• Minimal FET loss
• Negligible gate drive loss

27.12MHz, φ2 Inverter, $V_{DS}$ of GaN

20ns/div, 150V/div
Package / Drive:

Early GaN

Cascoded dMode Parasitics

Complex
Embedded eMode

Complex eMode discrete drive

From GS66508T-EVBHB 650V GaN E-HEMT Half Bridge Evaluation Board
Switch, Drive:
Creating the World’s First AllGaN™ Power ICs

Fastest, most efficient GaN Power FETs

First & Fastest Integrated GaN Gate Driver

World’s First AllGaN™ Power IC

Up to 40MHz switching, 4x higher density & 20% lower system cost
Switch, Drive: Navitas GaN Power IC

- **Monolithic** integration
- 20x lower drive loss than silicon
- Driver impedance matched to power device
- Shorter prop delay than silicon (10ns)
- Zero inductance turn-off loop
- Digital input (hysteretic)
- Rail-rail drive output
- Layout insensitive
Package:

Fast, Low Cost, Industry-Standard QFN

• Leadframe-based 5x6mm power package outline
• Low profile, small footprint with HV clearance
• Kelvin source connection for gate drive return
• Low inductance power connections (~0.2nH)
• Low thermal resistance (<2°C/W)
• I/O pins enough for drive functions
• High volume, reliable, low cost
Monolithic Drive:
Crisp & Efficient Gate Control

• Eliminates gate overshoot and undershoot
• Zero inductance on chip insures no turn-off loss
Topology:

Hard-Switch

Primary Switch Power Loss:

\[ P_{\text{FET}} = P_{\text{COND}} + P_{\text{DIODE}} + P_{\text{T-ON}} + P_{\text{T-OFF}} + P_{\text{DR}} + P_{\text{QRR}} + P_{\text{QOSS}} \]
Topology:

Hard-Switch $\rightarrow$ Soft-Switch

**Primary Switch Power Loss:**

\[ P_{\text{FET}} = P_{\text{COND}} \times k + P_{\text{DIODE}} + P_{\text{T-ON}} + P_{\text{T-OFF}} + P_{\text{DR}} + P_{\text{QRR}} + P_{\text{QOSS}} \]

- k-factor $> 1$ due to increased circulating current, duty cycle loss
- $P_{\text{T-ON}} = 0$ (soft-switch)
- $P_{\text{QOSS}} \downarrow 2-3x$ (silicon devices can have high $C_{\text{OSS}}$ charging/discharging losses)
Topology:

Hard-Switch → Soft-Switch with eMode GaN

**Primary Switch Power Loss:**

\[
P_{\text{FET}} = P_{\text{COND}} \cdot k + P_{\text{DIODE}} + P_{\text{T-ON}} + P_{\text{T-OFF}} + P_{\text{DR}} + P_{\text{QRR}} + P_{\text{QOSS}}
\]

- **k-factor** >1 due to increased circulating current, duty cycle loss
- **\( P_{\text{T-On}} \)** = 0 (soft-switch)
- **\( P_{\text{Qoss}} \)** ↓10x 2-3x (GaN \( C_{\text{OSS}} \) charging/discharging loss negligible up to 2MHz)
- **\( P_{\text{DRIVER}} \)** ↓10x (GaN \( P_{\text{DR}} \) negligible up to 2MHz)
- **\( P_{\text{QRR}} \)** = 0
- **\( P_{\text{DIODE}} \)** ↓2x (reverse conduction loss reduced by synchronous rectification)
- **\( P_{\text{T-OFF}} \)** = Reduced (limited by I-V crossover loss due to drive loop impedance)
Topology, Switch, Drive:

Hard-Switch $\rightarrow$ Soft-Switch with GaN Power IC

Primary Switch Power Loss:

$$P_{FET} = P_{COND} \ast k + P_{DIODE} + P_{T-ON} + P_{T-OFF} + P_{DR} + P_{QRR} + P_{QOSS}$$

- $k$-factor $>1$ due to increased circulating current, duty cycle loss
- $P_{T-On} = 0$ (soft-switch)
- $P_{Qoss}$ ↓10x 2-3x (GaN $C_{OSS}$ charging/discharging loss negligible up to 2MHz)
- $P_{DRIVER}$ ↓10x (GaN $P_{DR}$ negligible up to 2MHz)
- $P_{QRR} = 0$
- $P_{DIODE}$ ↓3x 2x (synchronous rectification with improved dead-time control)
- $P_{T-OFF} = 0$ Reduced (near-zero drive loop impedance with integration)

$>10x$ frequency increase possible with higher efficiencies
Control ICs:

MHz Controllers ... with more, faster to come

PFC (BCM):
- L6562 (1MHz)
- NCP1608 (1MHz)
- UCC28061 (500kHz)

DC-DC (LLC):
- NCP1395 (1.2MHz)
- FAN7688 (500kHz) (+SR)
- ICE2HS01G (1MHz)

DC-DC (Sync Rectifier):
- NCP4305 (1MHz)
- UCC24610 (600kHz)

PWM:
- NCP1252 (500kHz)
- NCP1565 (1.5MHz)
- UCC28C44 (1MHz)
- UCC25705 (4MHz)

DSP:
- UCD3138 (2MHz)
- dsPIC33xx (5MHz)
- ADP1055 (1MHz)
Switch:

SR FETs: Better with GaN

• All relevant FsOM favor GaN at 60V
  • $R_{\text{DS(ON)}} \times Q_G$ reflects drive losses
  • $R_{\text{DS(ON)}} \times Q_{\text{OSS}}$ reflects turn-off losses with non-resonant rectification
  • $R_{\text{DS(ON)}} \times Q_{\text{RR}}$ reflects stored minority carrier turn-off losses (minimized with dead-time control)

• Si in QFN 5x6mm, GaN is Chip-Scale BGA

Note: Datasheet typicals at 4.5/5V gate drive and capacitance curves
Magnetics (EMI):
Smooth, clean, controlled waveforms

- 500V Switching
- No overshoot / spike
- No oscillations
- ‘S-curve’ transitions
- ZVS Turn-on
- Zero loss turn-off
- Sync rectification
- High frequency
- Small, low cost filter
Critical Conduction Mode (CrCM) PFC

- CrCM PFC enables ZVS / QR operation
  - Also known as Boundary Conduction Mode (BCM)
  - Ideal for high frequency
  - Uses slower, lower cost diode than in Continuous Conduction Mode (CCM)
  - Peak current ‘OK’ up to ~300W per phase (can interleave for higher power)

- Operating frequency varies with:
  - AC input voltage, output power, AC line cycle

- ‘Nominal’ frequency specified as:
  - $220V_{AC}$, full load, peak of the AC line
PFC Frequency vs. Power

- Calculated CrCM example to show frequency trend
- 150W PFC Boost
  - Assume L6562 controller
  - Nominal frequency = 270kHz (220V_{AC}, full load, peak of the AC line)
  - Maximum frequency = 1MHz (controller limit)
150W CrCM Boost PFC

- **Input**: Universal AC (85-265V<sub>AC</sub>, 47-63Hz)
- **Output**: 400V, 0.27A (150W)
- **Frequency***: 120V = 167-230kHz
  - 220V = 230-500kHz
  - 265V = 1MHz
- **Efficiency**: >98% peak, >97.1% average (25%, 50%, 75%, 100% load)
- **Power Factor**: >0.995
- **Demo Size**: 100 x 50 x 20mm “No heatsink” design
- **Construction**: 2-layer PCB, SMT powertrain on bottom side

*limited by control IC (L6562A)
150W PFC: Schematic

- EMI Filter + Rectifier
- PFC Control IC (L6562A)
- GaN Power IC
- Boost Inductor
- VCC Supply
- Boost Diode
- High Voltage Start-Up
150W PFC: Layout

- All active semiconductors on bottom-side
  - Low profile
  - ‘No-heatsink’ design
- 100 x 50 x 20mm

- PFC Boost Diode
- GaN Power IC
- L6562A PFC Control IC
- AC Bridge Rectifier
- Bulk Cap
- EMI Filter
## 150W PFC: SuperJunction Si vs. GaN Power IC

<table>
<thead>
<tr>
<th>Pack</th>
<th>Pack</th>
<th>$R_{DS(ON)}$ mΩ</th>
<th>$Q_G$ nC</th>
<th>$C_{OSS(er)}$ pF</th>
<th>$C_{OSS(tr)}$ pF</th>
<th>$R*Q_G$ mΩ.nC</th>
<th>$R*C_{OSS(tr)}$ mΩ.pF</th>
<th>$R*C_{OSS(er)}$ mΩ.pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Navitas</td>
<td>5x6</td>
<td>160</td>
<td>2.5</td>
<td>30</td>
<td>50</td>
<td>400</td>
<td>8,000</td>
<td>4,800</td>
</tr>
<tr>
<td>IPL65R199CP</td>
<td>8x8</td>
<td>180</td>
<td>32</td>
<td>69</td>
<td>180</td>
<td>5,760</td>
<td>32,400</td>
<td>12,400</td>
</tr>
<tr>
<td>IPL60R130C7</td>
<td>8x8</td>
<td>115</td>
<td>35</td>
<td>53</td>
<td>579</td>
<td>4,025</td>
<td>66,600</td>
<td>6,100</td>
</tr>
<tr>
<td>GaN Benefits</td>
<td>&gt;50%</td>
<td>n/a</td>
<td>&gt;10x</td>
<td>&gt;2x</td>
<td>&gt;10x</td>
<td>&gt;10x</td>
<td>&gt;7x</td>
<td>&gt;2.5x</td>
</tr>
</tbody>
</table>

**GaN Benefits**
- >50% power efficiency improvement
- >10x gate drive efficiency improvement
- >2x turn-on and turn-off losses improvement
- >10x output capacitance reduction
- >10x reverse recovery time reduction
- >7x forward voltage drop reduction
Full Load FET Temperature

- GaN running cool (61°C)
  - Efficiency up 1% vs. Si CP
  - Loss 20-35% lower
  - Power Factor >99.5%

- CP Si running >90°C
- C7 Si too hot to run at 220V_{AC}
Silicon’s High $C_{OSS}$ Creates Partial ZVS

- High loss due to large stored charge while hard-switching
- Si $C_{OSS}$ is 50x-100x worse than GaN at $V_{DS} < 30V$

120V$_{AC}$, Si CP partial hard-switching (~200kHz)

120V$_{AC}$, GaN clean ZVS waveforms (~200kHz)

- Turn-off losses low due to integrated drive
- Near loss-less ZVS turn-on transition
- Minimize deadtime for low reverse conduction loss
- No voltage spikes / overshoot
Critical Parameters: $C_{OSS}$, $E_{OSS}$

- $Q_{OSS}$ charge affects ZVS transition time and $E_{OSS}$ under partial ZVS condition
- **Switching loss:** $P_{LOSS} = E_{OSS} \cdot (V_{DS}) \cdot F_{SW}$
  - Si has 3x higher loss than GaN at 200V (partial ZVS) - big effect at full or light load condition
  - CrCM boost has inherent partial ZVS at high line – so 265VAC and light load is worst case
- For more information: “$C_{OSS}$ Hysteresis in Advanced Superjunction MOSFETs”, Harrison, APEC 2016
Long Si ZVS Transition Time = Trapped Energy

- \( Q_{OSS} \) directly proportional to transition time, which limits max frequency
- If too slow, goes into partial ZVS condition, creates \( E_{OSS} \) loss
Light Load = High Frequency = High Loss for Si

Switching loss: $P_{\text{LOSS}} = E_{\text{OSS}} (V_{DS}) \times \text{frequency (at 20W)}$

= 3.5\text{μJ} \times 455\text{kHz}$

= 1.59\text{W}$

= 160°C!
Light-Load = High Frequency

Hot Si, Cool GaN

- **Navitas GaN Power IC**: 450kHz, 70°C
  - 5x6mm QFN, 160mΩ
- **Si Superjunction ‘CP’**: 455kHz, 160°C
  - 8x8mm QFN, 180mΩ
- **Navitas GaN Power IC**: 278kHz, 61°C
  - 8x8mm QFN, 180mΩ
- **Navitas GaN Power IC**: 278kHz, 86°C
  - 8x8mm QFN, 180mΩ
Topology:
LLC at 650kHz (400-12V)

$V_{SW} \ (100V/div)$

$I_L \ (1A/div)$

Normal Operation, 50% duty cycle, Full ZVS
Topology: PFC+LLC

**Frequency drives 2x-4x Power Density**

- Typical adapters (65-150kHz) = 5-12W/in³
- Navitas demo (500kHz) = 13.5W/in³
- Navitas customer estimate = 20-25W/in³

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**Graph:**
- **X-axis:** Power (W)
- **Y-axis:** Power Density (W/in³)
- **Legend:**
  - Typical Adapter 65-150kHz
  - Navitas demo 500kHz
  - Navitas Customer Estimate

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**Applications:**
- Gamer Laptops (100-150W)
- All-in-One PCs (150-200W)
- 38”-52” TVs (100-200W)
I found my Eco-System!