



# GaN Power ICs: Device Integration Delivers Application Performance

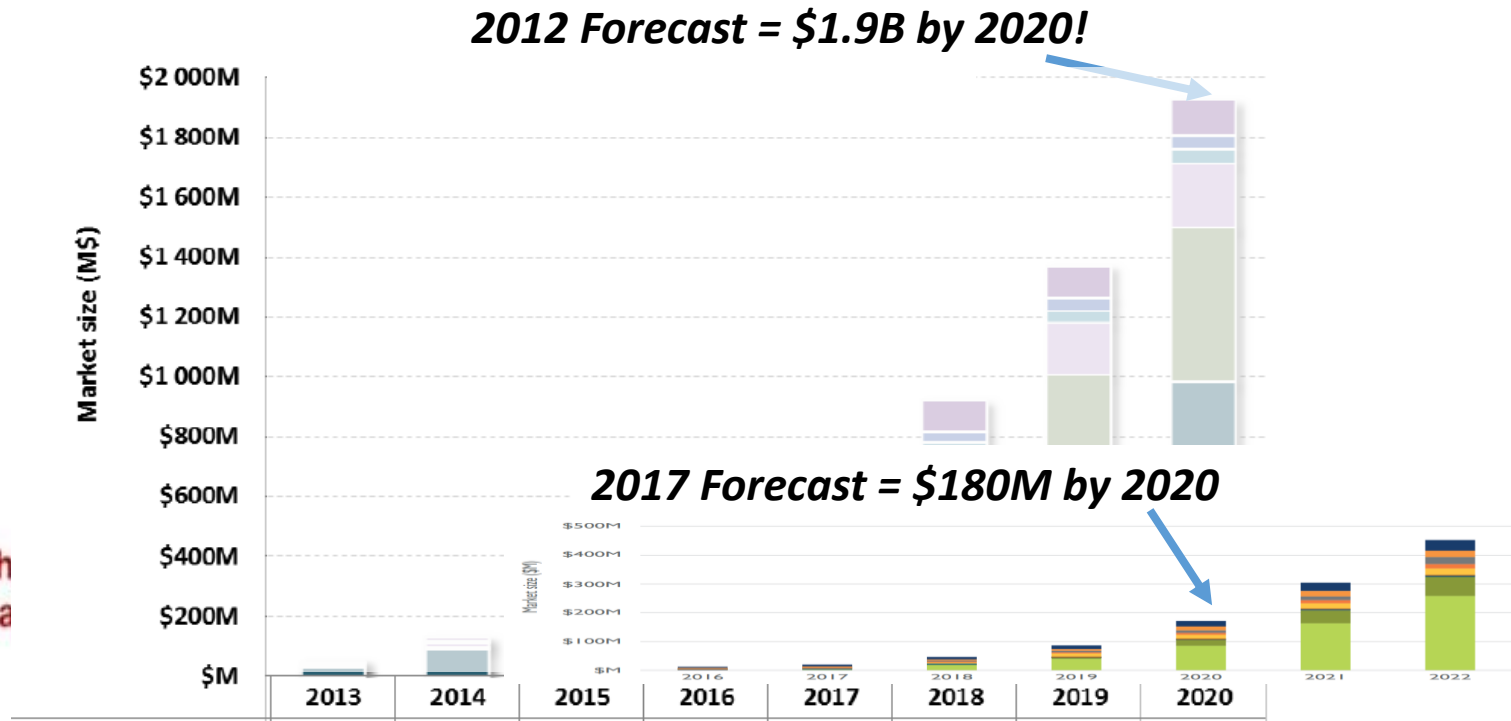
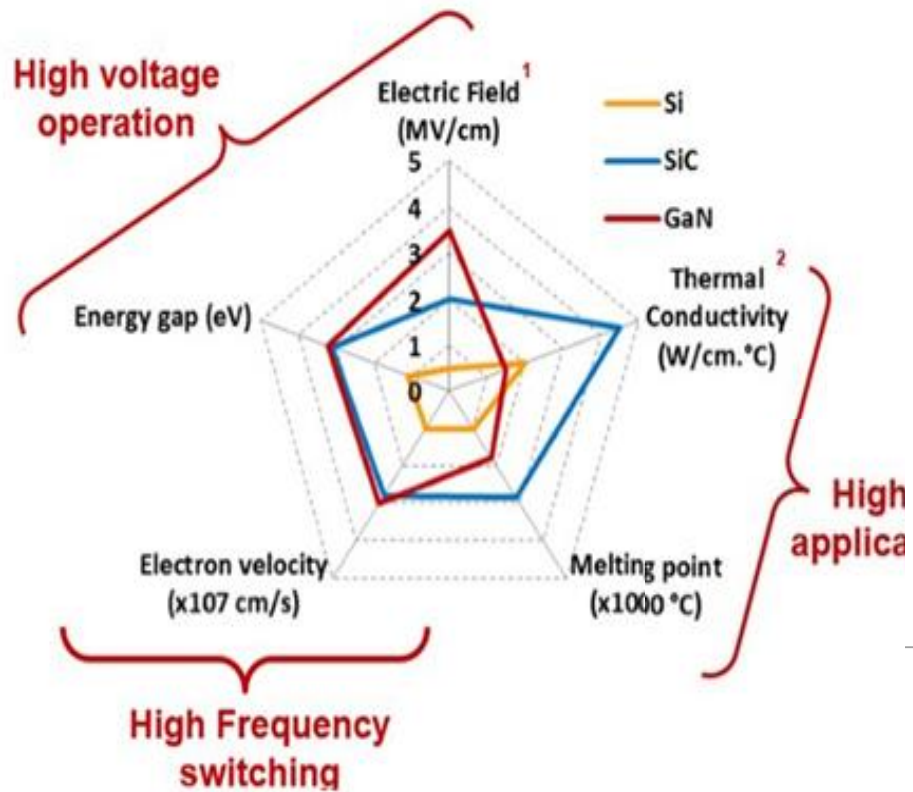
5th IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)

Albuquerque, NM, USA. November 1<sup>st</sup> 2017

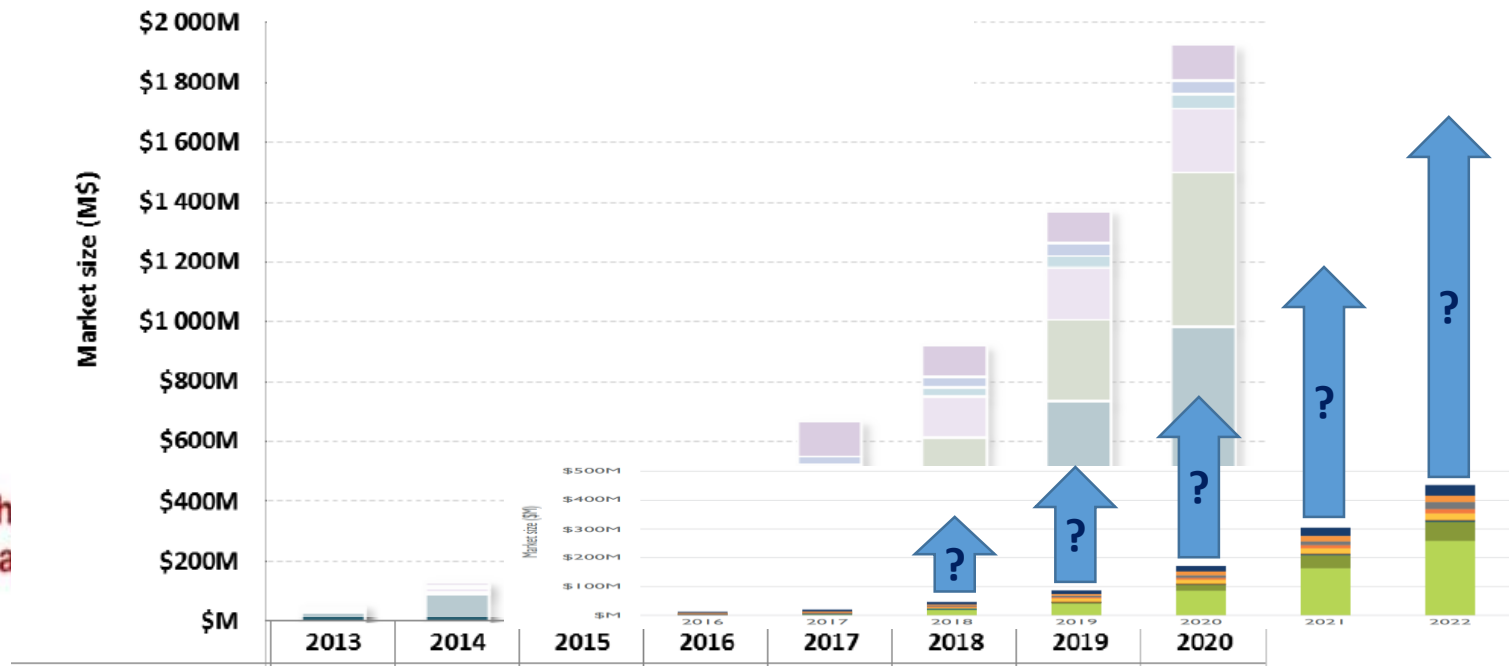
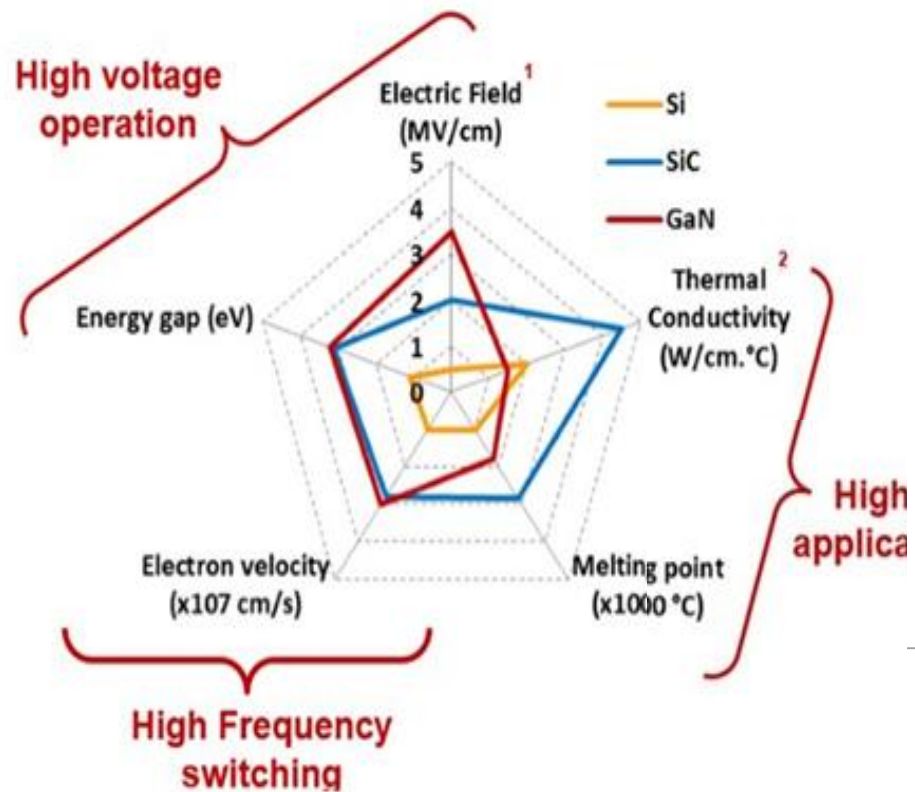
Dr. Nick Fichtenbaum, Co-Founder & VP Engineering

[Nick.Fichtenbaum@navitassemi.com](mailto:Nick.Fichtenbaum@navitassemi.com)

# Fast GaN, Slow Adoption?

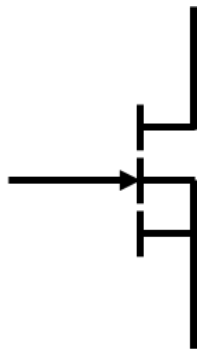


# Faster with AlGaN™ Integration!



# World's First AllGaN™ Power ICs

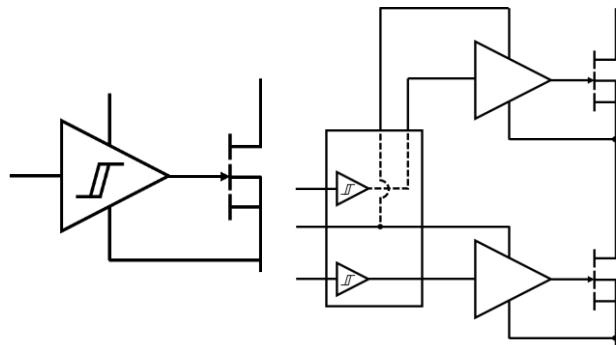
**Fastest, most efficient  
GaN Power FETs**



**>20x faster than silicon  
>5x faster than cascoded GaN  
Proprietary design**



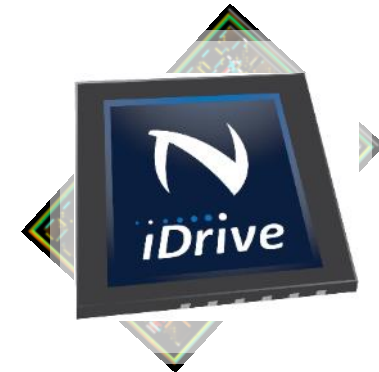
***iDrive* First & Fastest  
Integrated GaN Gate Drivers**



**>3x faster than any other gate driver  
Proprietary design  
30+ patents granted/applied**



**World's First  
AllGaN™ Power IC**

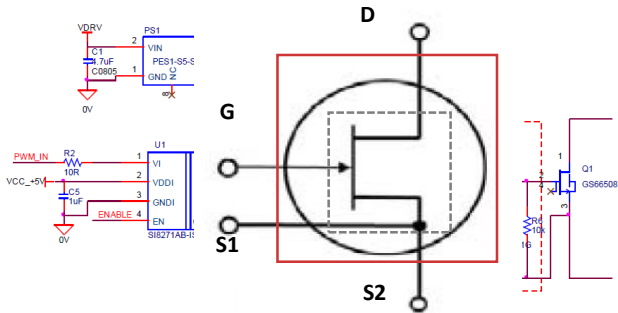


**Up to 40MHz switching, 5x higher density & 20% lower system cost**

# The Drive for Better Drivers

- Low  $V_{TH}$
- Low  $R \times Q$
- Low  $V_{GS\_Max}$

## Discrete FET + Discrete Driver

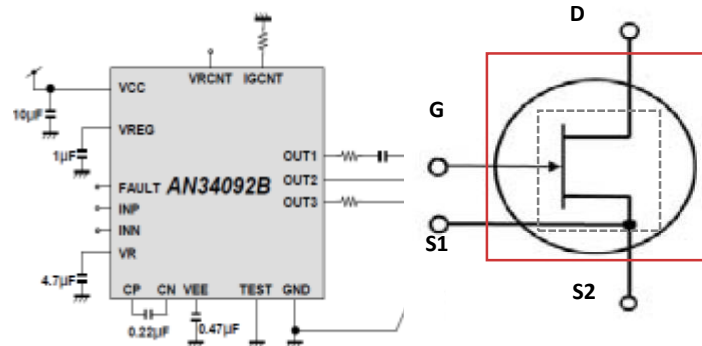


| Gate Drive Challenges           | Discrete FET + Discrete Driver | Discrete FET + Custom driver | GaN Power IC |
|---------------------------------|--------------------------------|------------------------------|--------------|
| Eliminate Gate Oscillations     | ✓                              |                              |              |
| Eliminate dV/dt Induced Turn-on | ✓                              |                              |              |
| Regulate Gate Drive Voltage     | ✓                              |                              |              |
| Gate Overvoltage Protection     | ✓                              |                              |              |
| Reduce Design Complexity        | ✗                              |                              |              |
| Manage Noise Sensitivity        | ✗                              |                              |              |
| Fast Turn-on/off Speed          | ✗                              |                              |              |
| Gate ESD Protection             | ✗                              |                              |              |
| Layout Insensitive              | ✗                              |                              |              |
| Lowest PCB Area                 | ✗                              |                              |              |
| Lowest Cost                     | ✗                              |                              |              |
| Remove Negative Drive           | ✗                              |                              |              |
| Fast Start-up                   | ✓                              |                              |              |
| Eliminate Standby Loss          | ✓                              |                              |              |

# The Drive for Better Drivers

- Low  $V_{TH}$
- Low  $R \times Q$
- Low  $V_{GS\_Max}$

## Discrete FET + Custom Driver

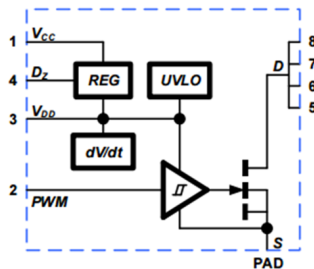


| Gate Drive Challenges           | Discrete FET + Discrete Driver | Discrete FET + Custom driver | GaN Power IC |
|---------------------------------|--------------------------------|------------------------------|--------------|
| Eliminate Gate Oscillations     | ✓                              | ✓                            |              |
| Eliminate dV/dt Induced Turn-on | ✓                              | ✓                            |              |
| Regulate Gate Drive Voltage     | ✓                              | ✓                            |              |
| Gate Overvoltage Protection     | ✓                              | ✓                            |              |
| Reduce Design Complexity        | ✗                              | ✓                            |              |
| Manage Noise Sensitivity        | ✗                              | ✓                            |              |
| Fast Turn-on/off Speed          | ✗                              | ✓                            |              |
| Gate ESD Protection             | ✗                              | ✗                            |              |
| Layout Insensitive              | ✗                              | ✗                            |              |
| Lowest PCB Area                 | ✗                              | ✗                            |              |
| Lowest Cost                     | ✗                              | ✗                            |              |
| Remove Negative Drive           | ✗                              | ✗                            |              |
| Fast Start-up                   | ✓                              | ✗                            |              |
| Eliminate Standby Loss          | ✓                              | ✗                            |              |

# The Drive for Better Drivers

- Low  $V_{TH}$
- Low  $R \times Q$
- Low  $V_{GS\_Max}$

## GaN Power IC



**No compromises**

| Gate Drive Challenges           | Discrete FET + Discrete Driver | Discrete FET + Custom driver | GaN Power IC |
|---------------------------------|--------------------------------|------------------------------|--------------|
| Eliminate Gate Oscillations     | ✓                              | ✓                            | ✓            |
| Eliminate dV/dt Induced Turn-on | ✓                              | ✓                            | ✓            |
| Regulate Gate Drive Voltage     | ✓                              | ✓                            | ✓            |
| Gate Overvoltage Protection     | ✓                              | ✓                            | ✓            |
| Reduce Design Complexity        | ✗                              | ✓                            | ✓            |
| Manage Noise Sensitivity        | ✗                              | ✓                            | ✓            |
| Fast Turn-on/off Speed          | ✗                              | ✓                            | ✓            |
| Gate ESD Protection             | ✗                              | ✗                            | ✓            |
| Layout Insensitive              | ✗                              | ✗                            | ✓            |
| Lowest PCB Area                 | ✗                              | ✗                            | ✓            |
| Lowest Cost                     | ✗                              | ✗                            | ✓            |
| Remove Negative Drive           | ✗                              | ✗                            | ✓            |
| Fast Start-up                   | ✓                              | ✗                            | ✓            |
| Eliminate Standby Loss          | ✓                              | ✗                            | ✓            |

# Clean, Controlled FET Gate

- **Discrete driver**

- Gate loop inductance creates overshoot (even with good layout)
- Reliability concern

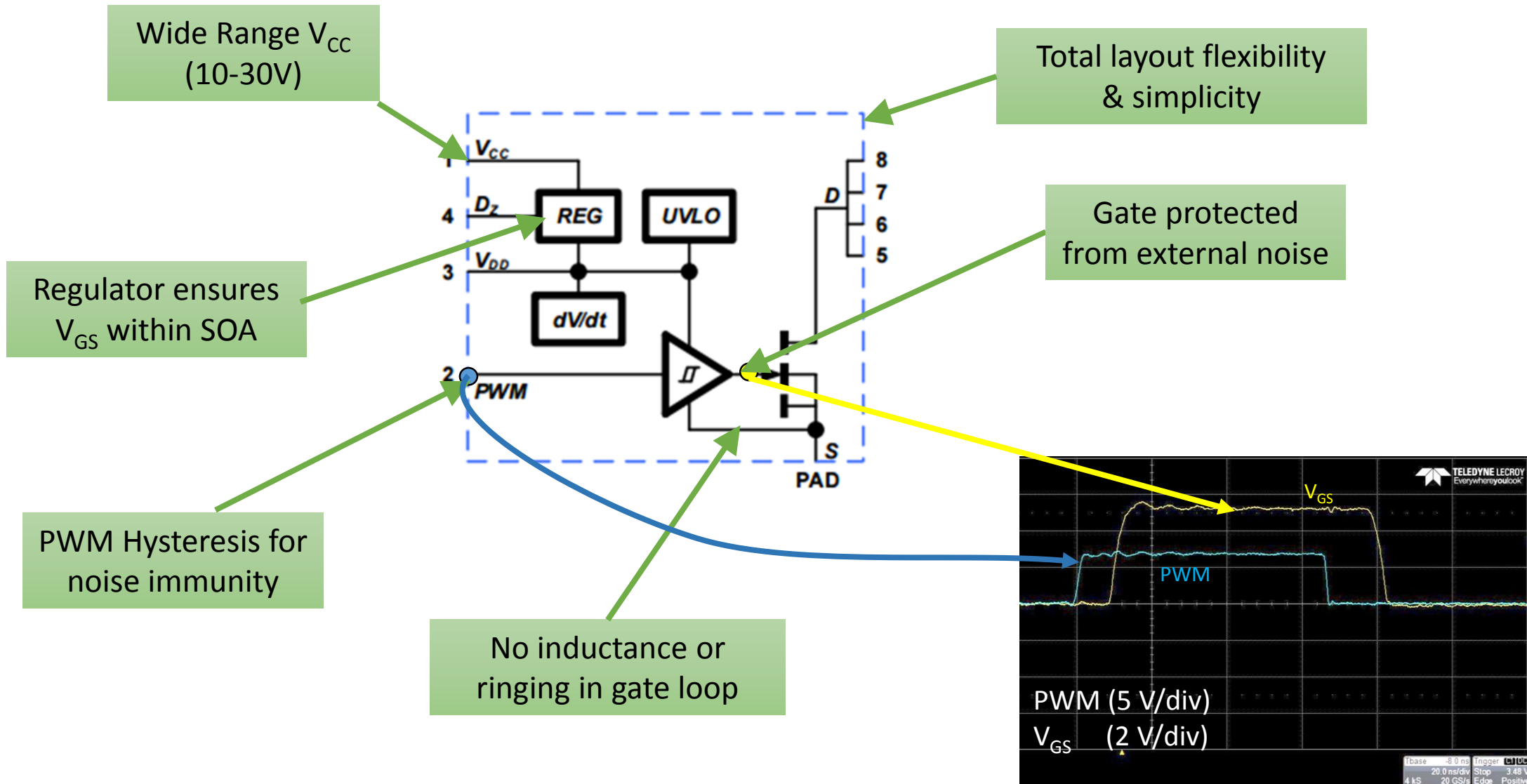
- **iDrive™ GaN Power IC**

- No gate loop parasitic
- Clean and fast gate signal

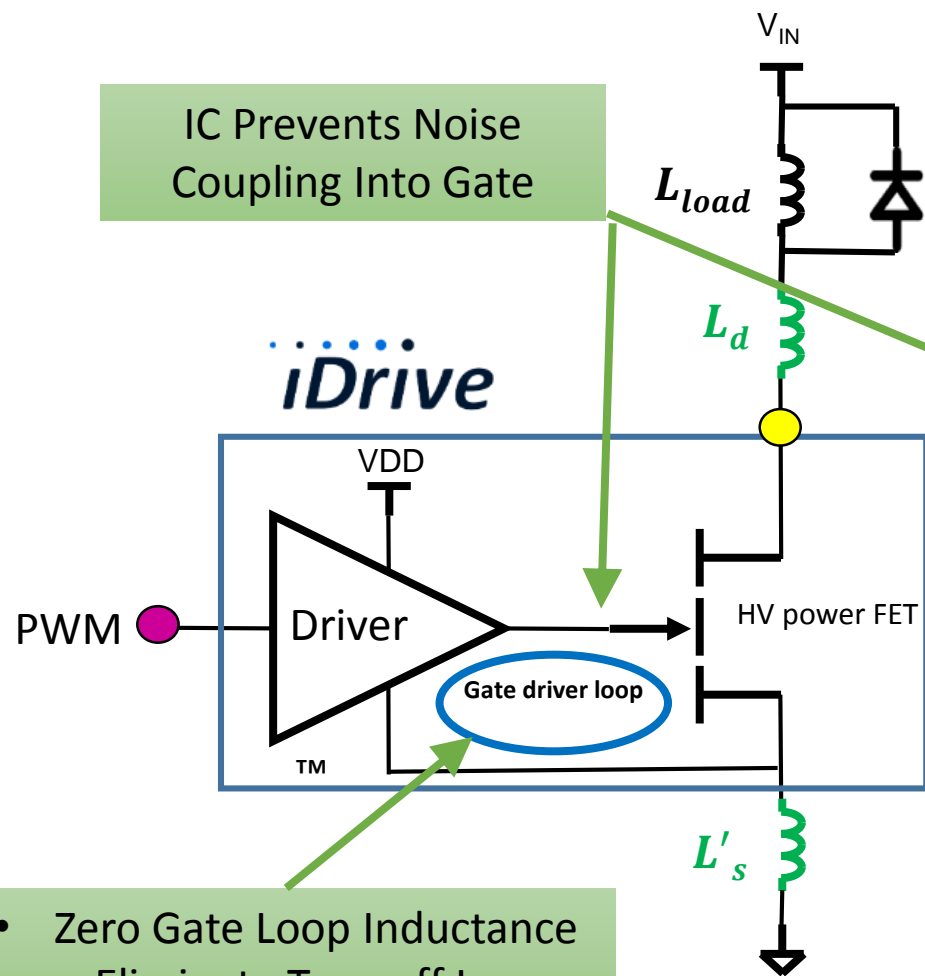




# Integrated Drive → Simple & Robust

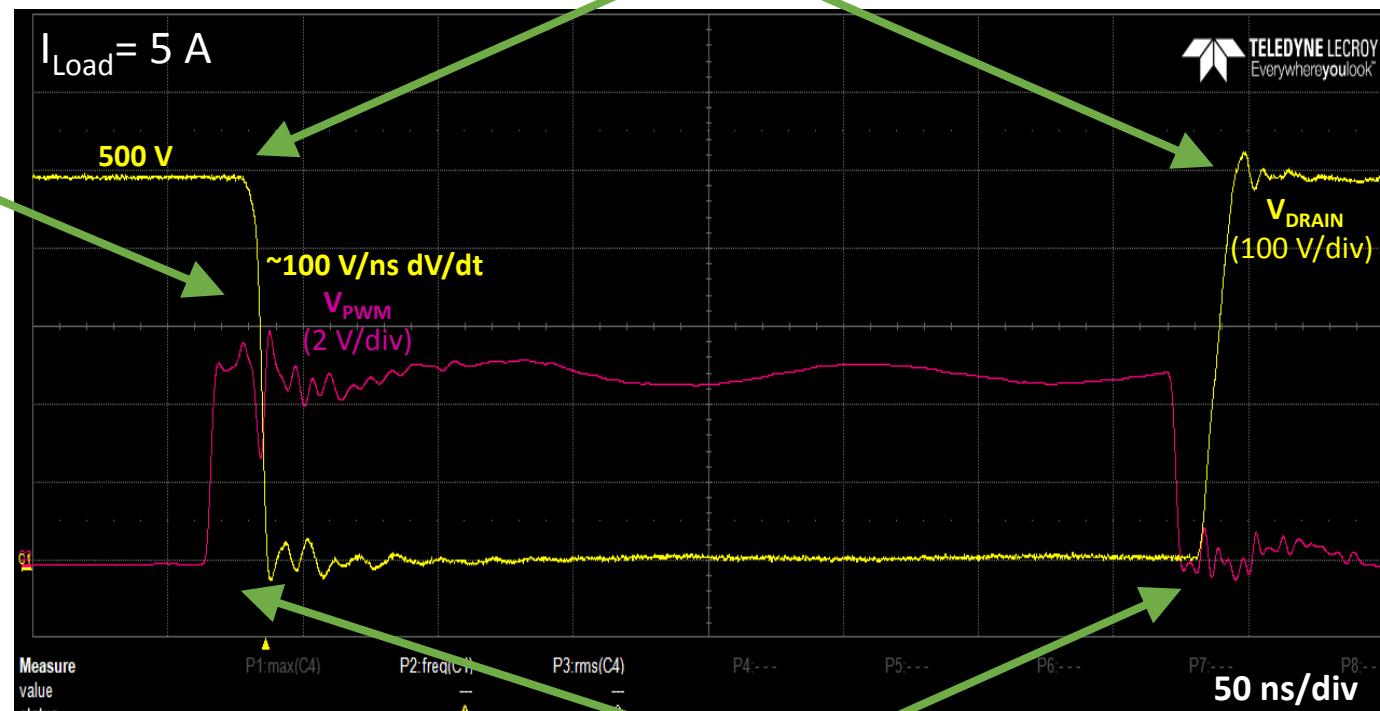


# Fast & Clean Hard Switching



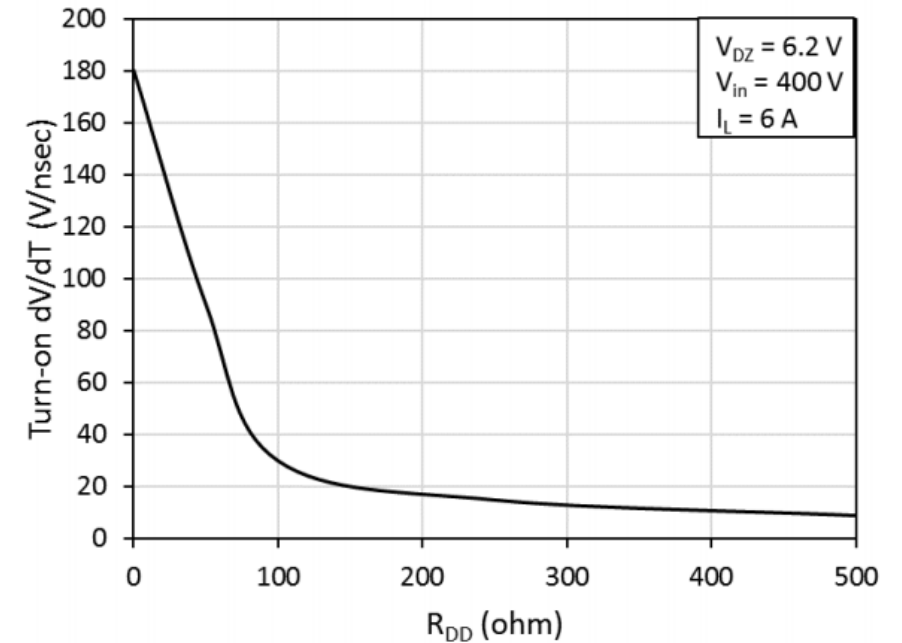
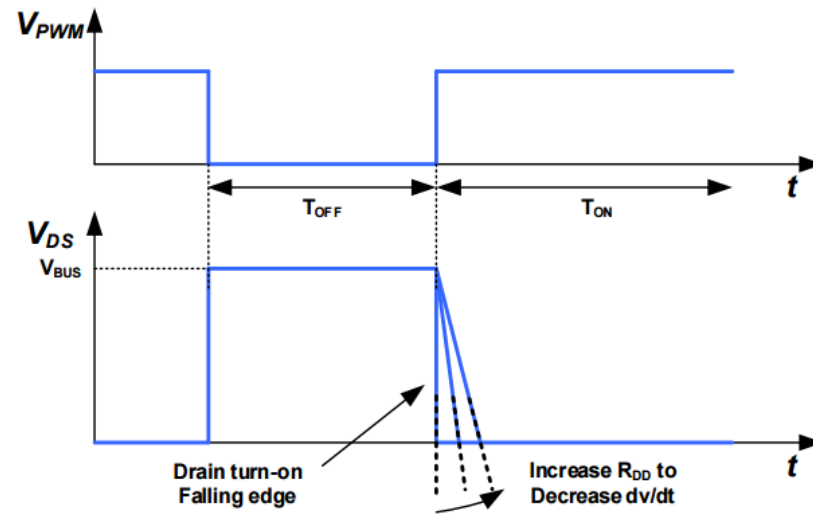
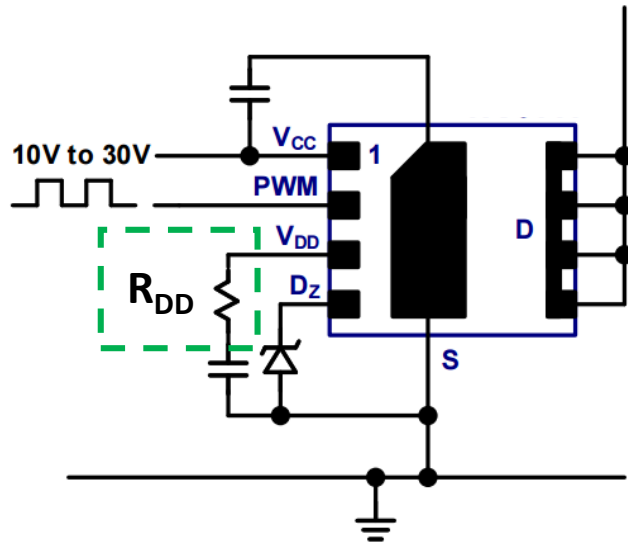
- Zero Gate Loop Inductance
- Eliminate Turn-off Loss

Clean HV Hard Switching



Prop Delay 10-20 ns

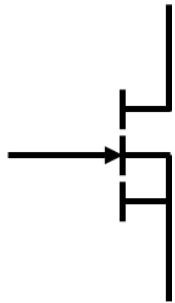
# Voltage Slew-Rate Control ... Easy EMI Tuning



$dv/dt$  controllable from 180 V/ns to 10 V/ns

# ESD Protection?

## Discrete GaN

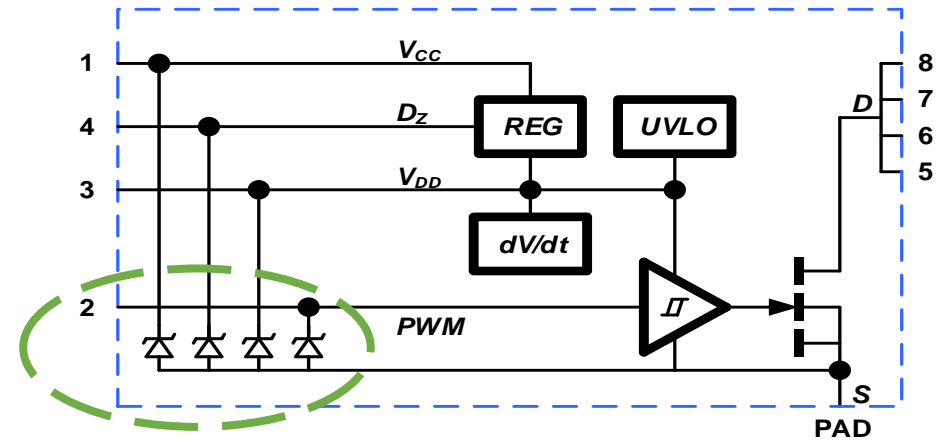


Low  $C_{ISS}$  → Fast switch, but...

**HBM < 250 V (typical)**

VS.

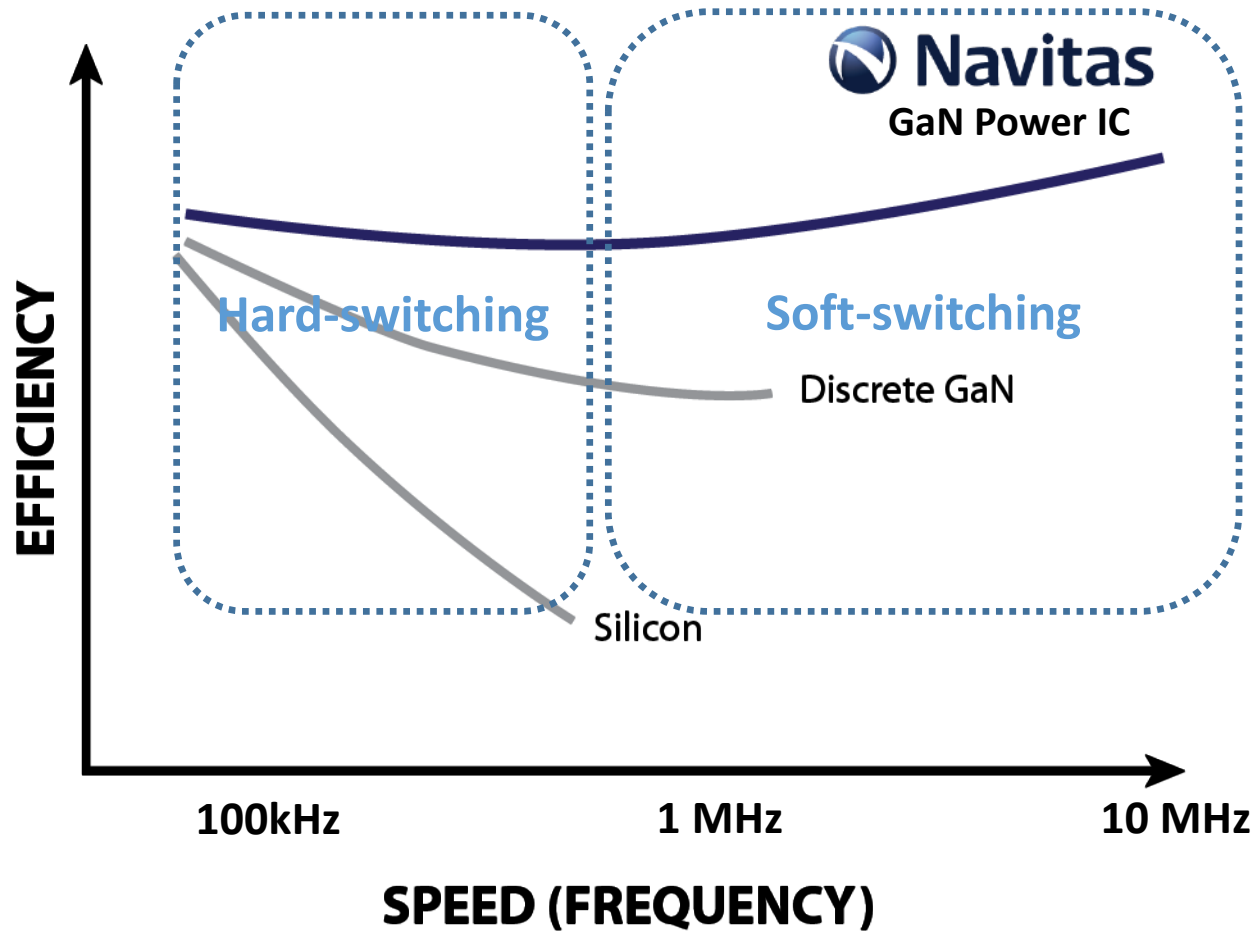
## GaN Power IC



Integrated ESD Protection

**HBM, CDM > 1,000 V**

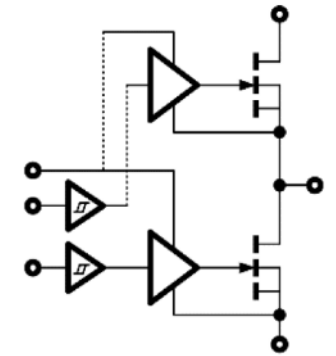
# Using Integration to Improve Power Density



## Half-Bridge Building Block



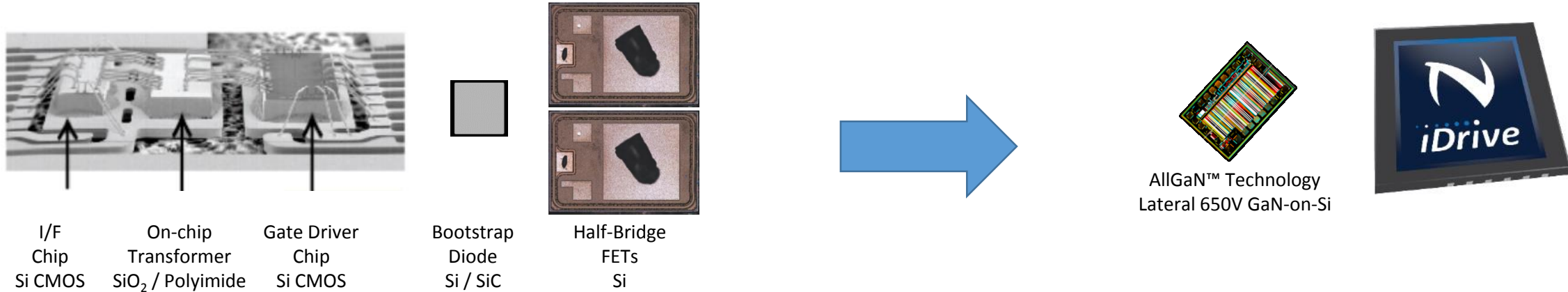
PQFN 6x8 mm



Simplified Schematic

*Soft-switching → allows simultaneous increase in frequency and efficiency uniquely enabled by GaN power ICs.*

# High-Frequency Half-Bridge Integration

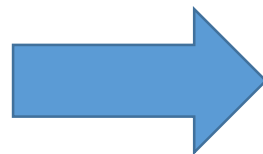


**Disparate Technologies**  
Hybrid isolator, discrete driver, discrete power, bootstrap diode

**Monolithic Platform**  
Lateral GaN-on-Si, Half-Bridge GaN Power IC

## High Power Loss

- Driver loss,  $R_G$  loss
- Bootstrap diode  $Q_{RR}$ ,  $V_F$
- Pulsed high current level shifter power (?)



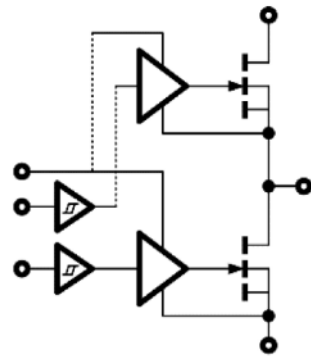
## Low Power Loss

- No gate driver loop parasitics, matched driver-FET capability, negligible loss vs frequency
- Zero  $Q_{RR}$ , low  $V_{DS}$  in synchronous charging
- Extremely fast, low-power level-shifter, multi-MHz operation, short propagation delay

# Simple, Powerful, Efficient, Cost-Effective

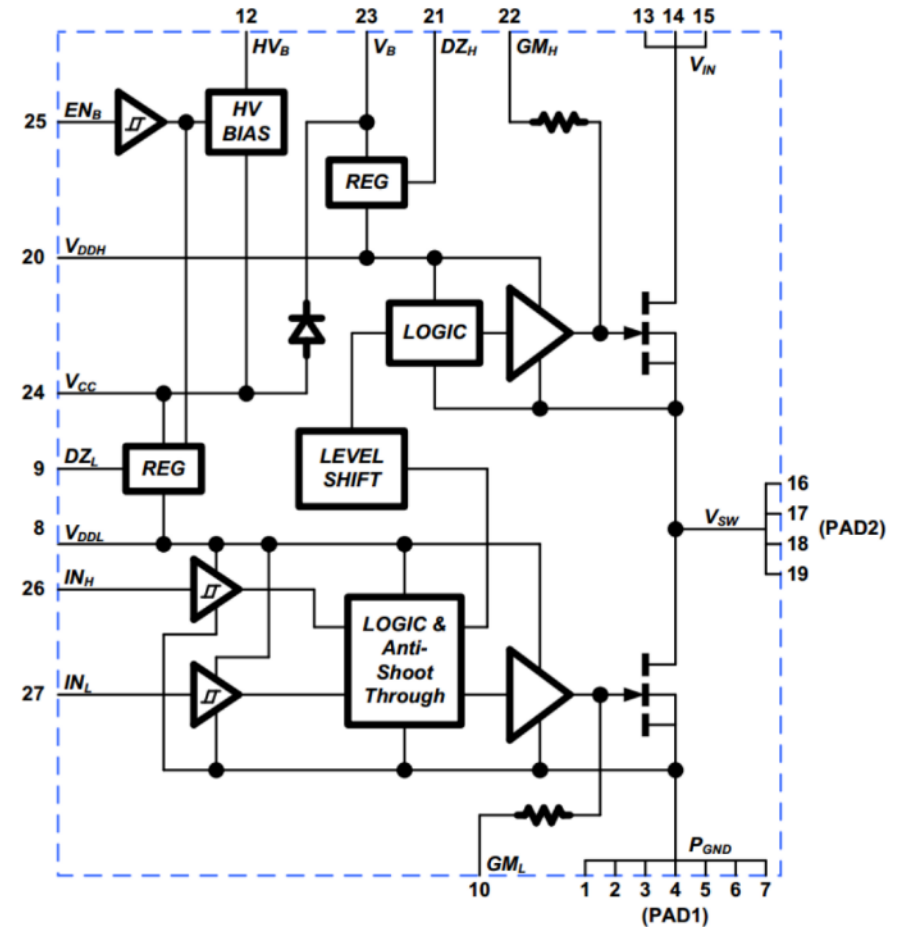


PQFN 6x8 mm



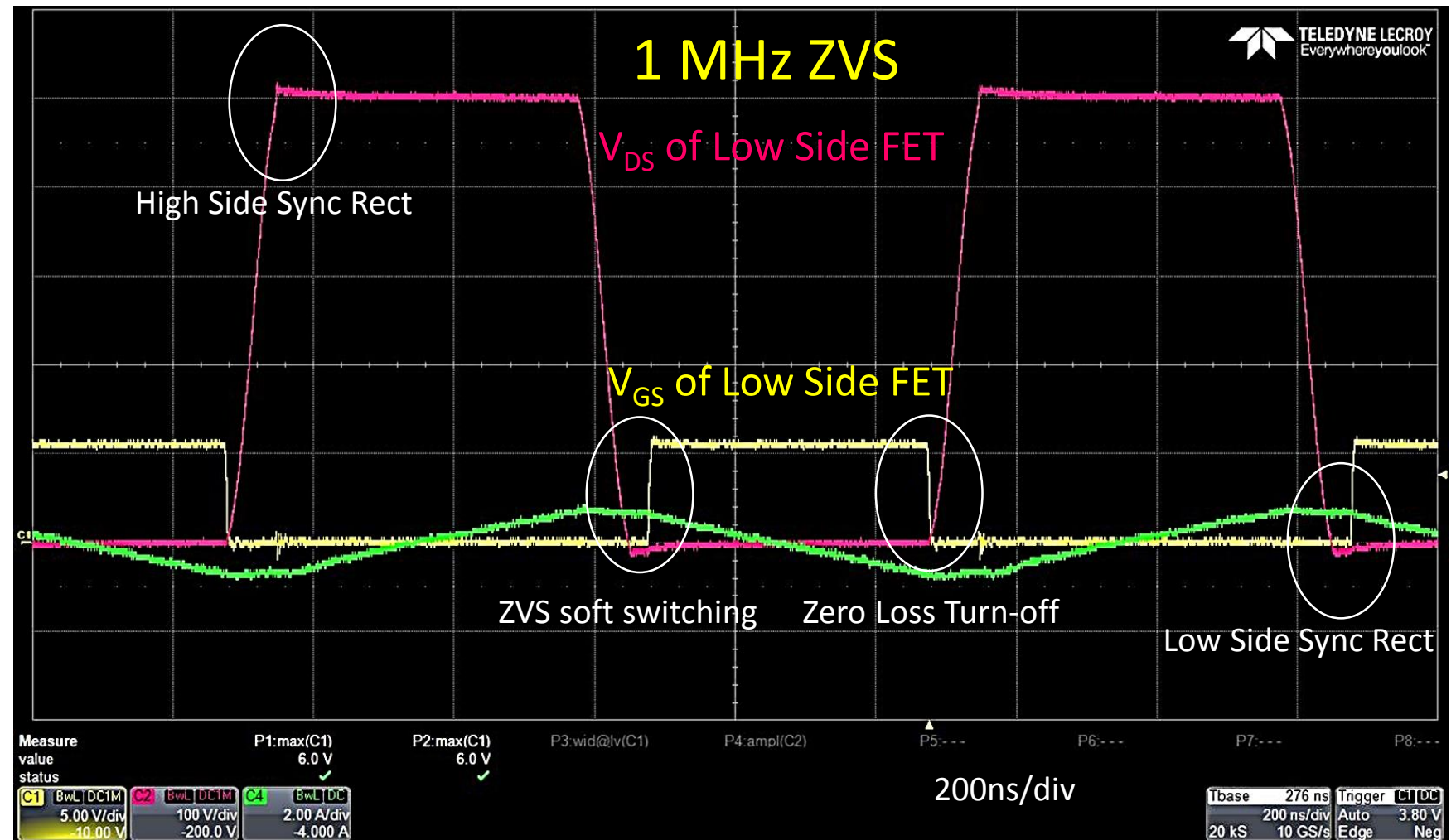
Simplified Schematic

- Internal level-shift & bootstrap circuits
- Monolithic integration
- Single component
- Ground-referenced control
- Active Clamp Flyback, Half-Bridge, LLC, etc.



# GaN Power IC – *Fast & Efficient*

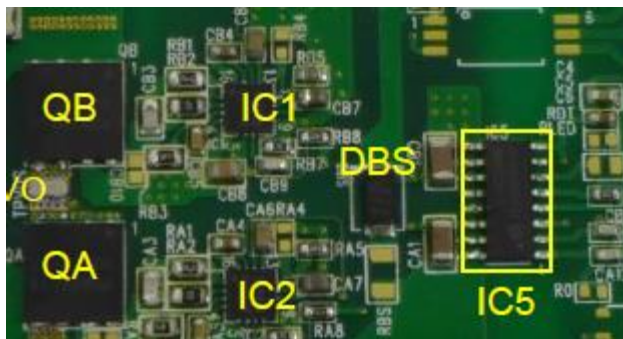
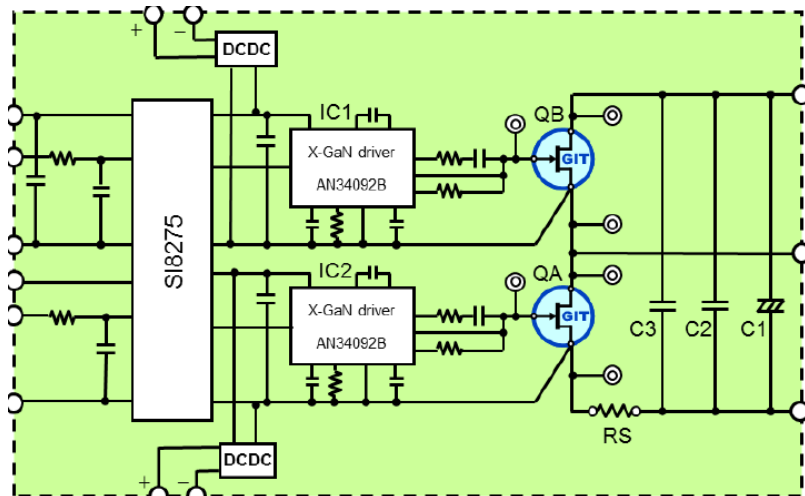
- 500 V Switching
- No overshoot / spike
- No oscillations
- ‘S-curve’ transitions
- Zero Loss Turn-on
- Zero Loss Turn-off
- Sync Rectification
- High frequency
- Small, low cost magnetics



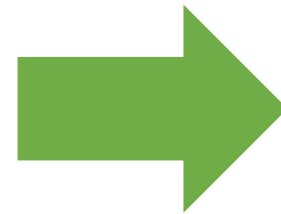


# Complex Design → *Made Simple*

## Half-Bridge *Discrete* GaN

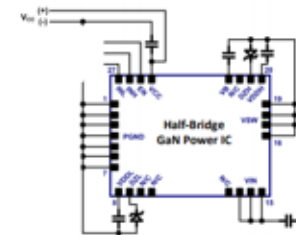


PCB Area: 24 x 42 ~ 1,000 mm<sup>2</sup>



- ✓ 20x smaller PCB area
- ✓ 40+ fewer components
- ✓ Lower cost
- ✓ Robust & protected
- ✓ Simple
- ✓ Easy layout

## Half-Bridge GaN *Power IC*



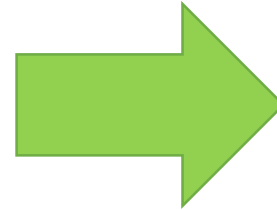
PCB Area: 6 x 8 = 48 mm<sup>2</sup>

# The World's Smallest 65W USB-PD Adapter

**MacBook <100 kHz**  
 <math><6.5 \text{ W/in}^3, 92\%</math>

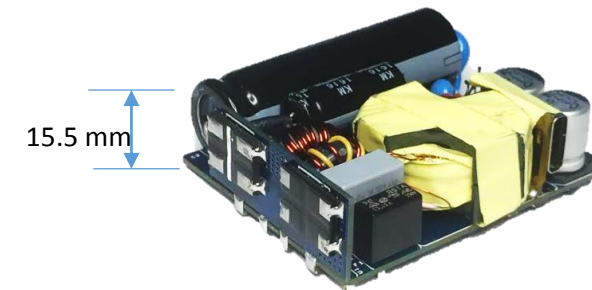
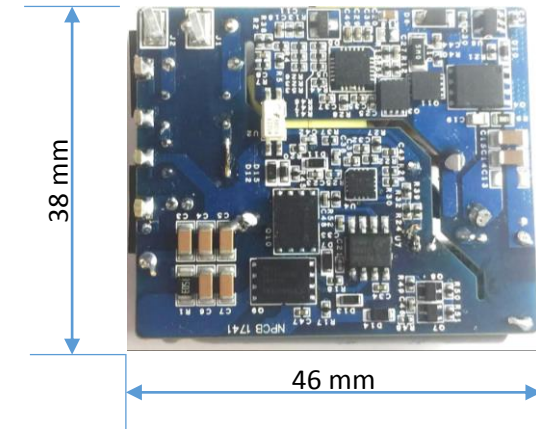


**Navitas 300 kHz**  
 <math>24 \text{ W/in}^3, 94\%</math>  
 = 45 cc cased

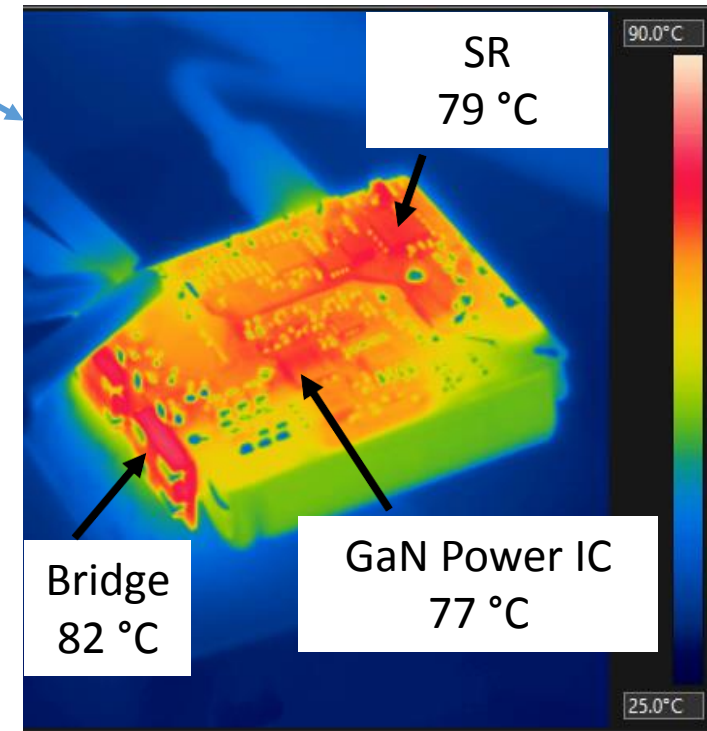
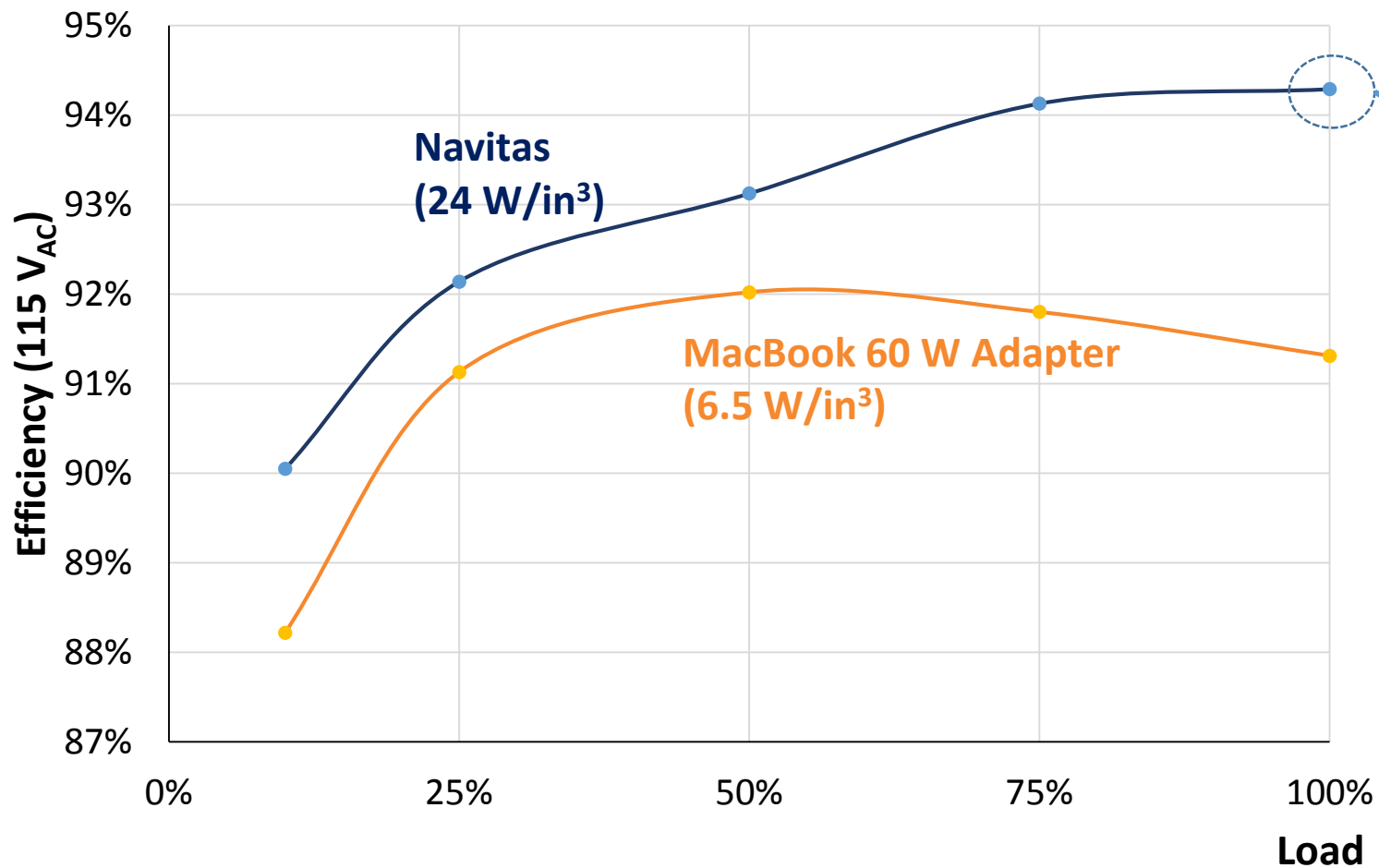


✓ **3-4x power density**

✓ **20% lower loss**

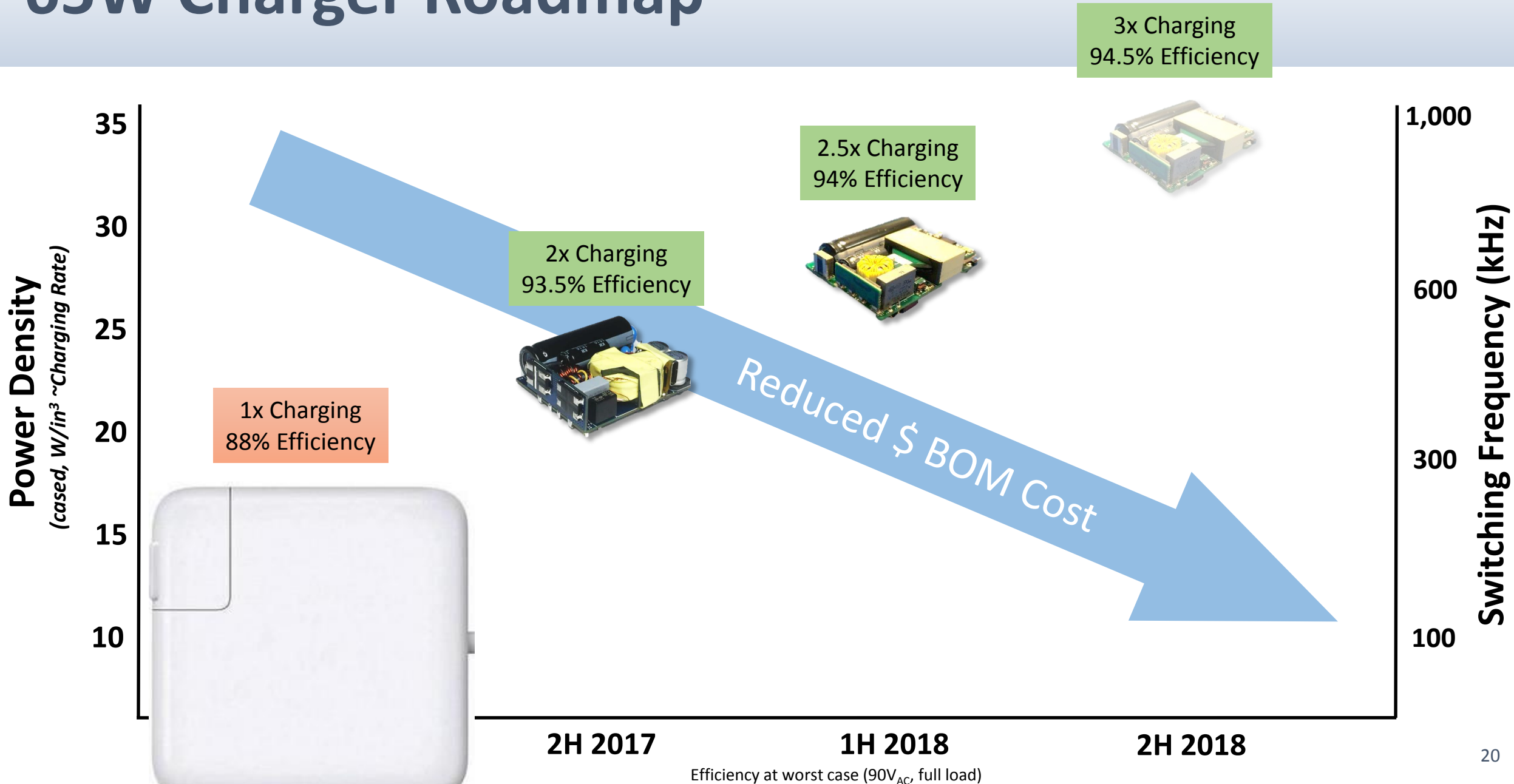


# Best-in-Class Efficiency, Cool Operation



115V<sub>AC</sub>, 65W, 20V<sub>OUT</sub>, 25°C

# 65W Charger Roadmap





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Albuquerque, NM, USA. November 1<sup>st</sup> 2017

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纳微 Navitas

65W USB-PD

