GaN Power Integrated Circuits

Dr. Nick Fichtenbaum, Co-Founder & VP Engineering

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• Why GaN Power ICs
• How to make GaN Power ICs
• Features of GaN Power ICs
• Commercial requirements for GaN products
• Products using GaN Power ICs
Potential of GaN Power Devices

Important Material Attributes

System Benefits

✓ Efficiency
✓ Cost Savings
✓ Power Density
Unlocking GaN’s Value

Fundamental GaN Material Properties

- High voltage operation
- Electric Field (MV/cm)
  - Si
  - SIC
  - GaN
- Energy gap (eV)
- Electric Field
- Melting point (°C)
- High conductivity (W/cm°C)
- High T° applications
- High frequency switching

Diagram showing comparisons and illustrations of dMode and eMode with various companies mentioned:
World’s First GaN Power ICs

Fastest, most efficient GaN Power FETs

- >20x faster than silicon
- >5x faster than cascoded GaN
- Proprietary design

First & Fastest Integrated GaN Gate Drivers

- >3x faster than any other gate driver
- Proprietary design
- 75+ patents granted/applied

World’s First
Power ICs

Up to 5x higher density & 20% lower system cost
The Drive for Better Drivers

- Low $V_{TH}$
- Low $R \times Q$
- Low $V_{GS_{Max}}$

### Gate Drive Challenges

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- **Low $V_{TH}$**
- **Low $R \times Q$**
- **Low $V_{GS\_Max}$**

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**GaN Power IC**

**No compromises**
Clean, Controlled, Easy to Use

• **Discrete driver**
  - Gate loop inductance creates overshoot (even with good layout)
  - Reliability concern

• **GaNFast™ GaN Power IC**
  - No gate loop parasitic
  - Clean and fast gate signal

• **GaNFast ICs unlock the efficiency, cost, and power density of GaN while making the customer experience easy to use and reliable**
• Why GaN Power IC?
• How to make GaN Power ICs?
• Features of GaN Power ICs
• Commercial requirements for GaN products
• Products using GaN Power ICs
Navitas eMode Power FET Technology

- Lateral device technology → Convenient isolation and easy voltage scaling
- High breakdown field (10X) and high mobility (2X) → Low $R_{DS(ON)}$, Low $Q_{OSS}$
- Lateral device technology → Low $Q_G$, easy to drive, easy to integrate
- Third quadrant operation, ie: bidirectional current flow, zero reverse recovery
- Processed in established CMOS line → High yield, high capacity
- Multiple metal technology using standard CMOS processing equipment
Navitas’ Unique Characteristics: Fabless with its own PDK

GaN HEMT is still an emerging technology in the market.
➢ Majority of GaN technologies and products developed are for high-voltage/power applications.
➢ Also, GaN devices are only available in unipolar n-type.

Navitas team has strong knowledge and capability to develop its own device and circuit libraries even with such handicaps.
• Excellent process design kit:
  • Device symbols
  • Pcells for automated device construction
  • Scalable, accurate
  • Verified for schematic and layout rules
  • Layout parameter extraction
• Angelov, ASM and silicon models are **not** suitable
  • Lack dMode, scalability, flexibility, speed
• Navitas GaN eMode FET scalable VerilogA model
  • Flexible: customized features/equations
  • High correlation between simulation and product
  • High-speed simulations
• GaN FET $I_DV_G$ Model with Temperature Effects
  • Solid lines = measured, dotted lines = Cadence simulation
Accurate over Drain Voltage

- Solid lines = measured, dotted lines = Cadence Spectre

- 20V rated eMode FET

- 650V rated eMode FET
PDK Verification

- Use simple ring oscillator structure to verify accuracy of PDK models
- Excellent agreement between simulated and measured performance
- Needs to include parasitic effects
Navitas GaN IC PDK

- PDK developed independent of the foundry
- Offers great deal of design flexibility
- Fast design/tape out cycle time
- Enables seamless integration of new devices and features
- Scalable models, streamlined for process corners

Navitas Proprietary GaN Building Blocks

- eMode and dMode transistors (7V - 650V)
- Integrated capacitors (7V – 650V)
- Integrated resistors
- Inverters
- Buffers
- Logic gates
- Pulse generators
- Level shifters
- ESD I/O circuits
Outline

• Why GaN Power IC?
• How to make GaN Power ICs?
• Features of GaN Power ICs
• Commercial requirements for GaN products
• Products using GaN Power ICs
Power GaN IC Product Portfolio

**Single Switch ("Singles")**

- 650 V eMode FET
- $R_{DS(ON)}$ 120-300m$\Omega$ available
- Integrated Gate Drive
- Programmable $dv/dt$ Control
- Integrated Regulator

**Two Switch ("Half-Bridge")**

- 2 x 650 V eMode FETs (Half-bridge)
- $R_{DS(ON)}$ 120-500m$\Omega$ available
- Symmetric and Asymmetric $R_{DS(ON)}$
- Integrated Gate Drive
- Shoot-through Protection
- Integrated Regulators
- Integrated Level-Shifter
- Integrated Boot-strap
Integrated Drive → Simple & Robust

- Wide Range $V_{CC}$ (10-30V)
- Regulator ensures $V_{GS}$ within SOA
- PWM Hysteresis for noise immunity
- No inductance or ringing in gate loop
- Total layout flexibility & simplicity
- Under voltage lockout protects the driver & FET when full power supply is not available
- Gate protected from external noise (Not pinned out of package)
dV/dt controllable with $R_{DD}$ from 10 V/ns to 90 V/ns
Integrated ESD Protection

GaN Power IC

Integrated ESD Protection

HBM, CDM > 1,000 V

ESD Qualification Tests

<table>
<thead>
<tr>
<th>Reference</th>
<th>Test Conditions</th>
<th>Duration</th>
<th>Lots</th>
<th>S.S.</th>
</tr>
</thead>
<tbody>
<tr>
<td>JS-001-2014</td>
<td>Human Body Model ESD</td>
<td>N/A</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>JS-002-2014</td>
<td>Charged Device Model ESD</td>
<td>N/A</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>

✓ Same ESD testing as Si devices can be applied to GaN
✓ Latch up testing not required in GaN devices
Shoot-Through Protection in Half-Bridge

Half-Bridge GaN Power IC

Non-Overlapping Logic Input
(Typical Operation)

Overlapping Logic Input
(Power IC Protection Mode)

High-side and Low-side gates never overlap due to shoot-through protection in power IC
Integrated Bootstrap

Bootstrap Diode Integration Benefits:

- Avoids risk of dV/dt induced diode failure
- Eliminates diode Cj and Irr power loss
- Eliminates necessity of using SiC at high $F_{SW}$
- Saves cost, especially if SiC is required
- Charges bootstrap capacitor losslessly
- Assures full charge/voltage is delivered
- Eliminates lossy current limiting resistor
- Saves board space in HV system

Bootstrap Diode Loss

$$f(C_{diode}, Q_{rr}, F_{SW})$$

https://www.onsemi.com/pub/Collateral/ES1J-D.PDF
Bootstrap Startup

High-side Startup Characteristics

Vb charging waveform

INH

INL

100ns

HS starts up after 4 100ns INL pulses

High side gate

INH

INL

100ns
• Why GaN Power ICs?
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• Features of GaN Power ICs
• Commercial requirements for GaN products
• Products using GaN Power ICs
✓ System Value (Features, Efficiency, Density)
✓ Reliability
✓ Cost
✓ System Value (Features, Efficiency, Density)
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Approach to Reliability of GaN Power ICs

Well Established Package Technology

650 V GaNFast Power FETs

Integrated GaN Gate Driver

GaNFast™ Power IC with exceptional Quality & Reliability

<table>
<thead>
<tr>
<th>Package Qualification</th>
<th>Traditional FET Tests</th>
<th>JESD47I (IC Qual Standard)</th>
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<tbody>
<tr>
<td>UHAST</td>
<td>HTRB</td>
<td>HTOL</td>
</tr>
<tr>
<td>HAST</td>
<td>HTGB</td>
<td>ELFR</td>
</tr>
<tr>
<td>THB</td>
<td>HAST</td>
<td>ESD</td>
</tr>
<tr>
<td>TC</td>
<td>THB</td>
<td>WLR</td>
</tr>
<tr>
<td>HTSL</td>
<td></td>
<td></td>
</tr>
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HTRB Acceleration & Lifetime Models

<table>
<thead>
<tr>
<th>Voltage/Temperature</th>
<th>100°C</th>
<th>125°C</th>
<th>150°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>650V</td>
<td>✓</td>
<td></td>
<td>✔</td>
</tr>
<tr>
<td>700V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>750V</td>
<td></td>
<td></td>
<td>✔</td>
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</table>

*Lifetime = A × (V⁻ⁿ) × (e^{E_A/kT})*

Time to Fail ∝ \( \frac{1}{(\text{Voltage})^{n=1.86}} \)

Time to Fail ∝ \( e^{(E_a=0.91eV)/kT} \)

V= 700 V, Temperature Acceleration

Lifetime in no load condition is >1E8 years, significant built-in margin

Projected Application Condition Using Model

T=150 °C, Voltage Acceleration
Mission Profile Driven HTOL (ZVS)

Full Power ($T_{DUT} = 100^\circ C$)

![Graph showing current and voltage with annotations](image)

1 us/div

Low side gate

VSW

PWM

S

D

REG

\(dV/dt\)

500 kHz

VCC

DZ

VDD

ZVS test bench replicates stresses seen in ACF application
### HTOL-based Lifetime Model

#### Voltage/Temperature

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<td>✓</td>
<td></td>
</tr>
<tr>
<td>575V</td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>600V</td>
<td>✓</td>
<td></td>
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#### Time to Failure

- **T=150 °C, Voltage Acceleration**
  \[ \frac{1}{(\text{Voltage})^{n=17.2}} \]

- **V= 650 V, Temperature Acceleration**
  \[ e^{\frac{E_a}{kT}} \]

---

**Note:**
- ✓ Indicates data available for the specified conditions.
- No ✓ indicates data not available.
Lifetime Estimation in Charger Application

Significant built-in reliability margin → even at worst case conditions (exceeds 10+ year lifetime requirement)
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GaNFast USB-C Chargers Have Arrived

Fast
Up to 3x more power
Up to 3x faster charging

Mobile
Half the size & weight of traditional chargers

Universal
One charger for **ALL** your devices
*One and Done!!*

**AUKEY**

- 27W
- 24W
- 30W

**RAVPower**

- 45W

*Made in Mind*
Latest Releases

- **World’s smallest 27W USB-C**
  - 41.5 cc, 0.65 W/cc
  - Available now from [amazon.com](http://amazon.com)

- **World’s smallest Charger 42W (30W-C + 18W-A) + Battery Pack (5,000 mAh)**
  - 31.5 x 85.5 x 81.5 mm
  - Available now from [Apple Store](https://apple.com)

[GAANFAST]
Questions?

Let’s go GaNFast™