



# 77<sup>TH</sup> DEVICE RESEARCH CONFERENCE

June 23-26, 2019 // University of Michigan, Ann Arbor // Ann Arbor, MI



# Navitas

*Let's go* **GaNFast**<sup>™</sup>

## GaN Power Integrated Circuits

Dr. Nick Fichtenbaum, Co-Founder & VP Engineering

[Nick.Fichtenbaum@navitassemi.com](mailto:Nick.Fichtenbaum@navitassemi.com)



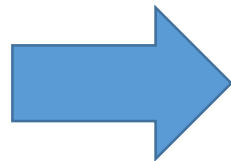
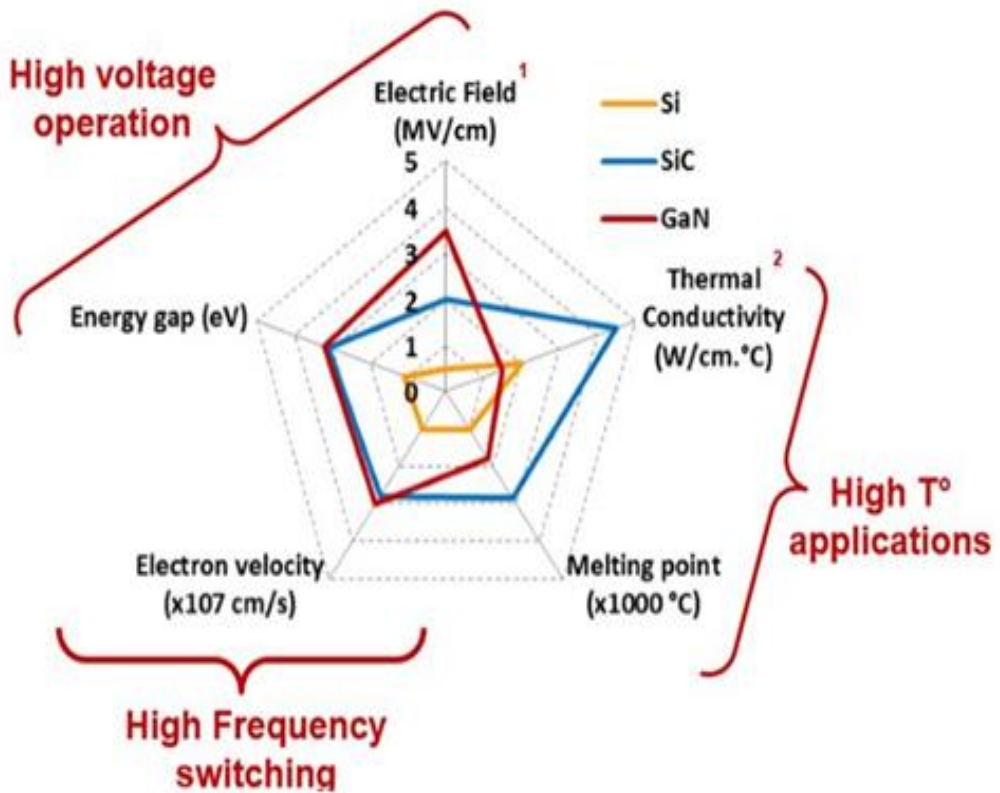
- Why GaN Power ICs
- How to make GaN Power ICs
- Features of GaN Power ICs
- Commercial requirements for GaN products
- Products using GaN Power ICs



# Potential of GaN Power Devices

## Important Material Attributes

## System Benefits

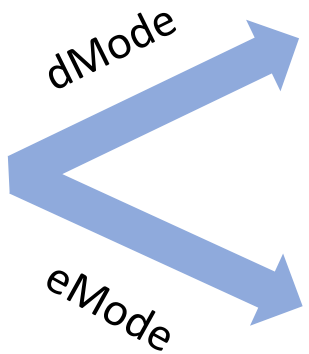
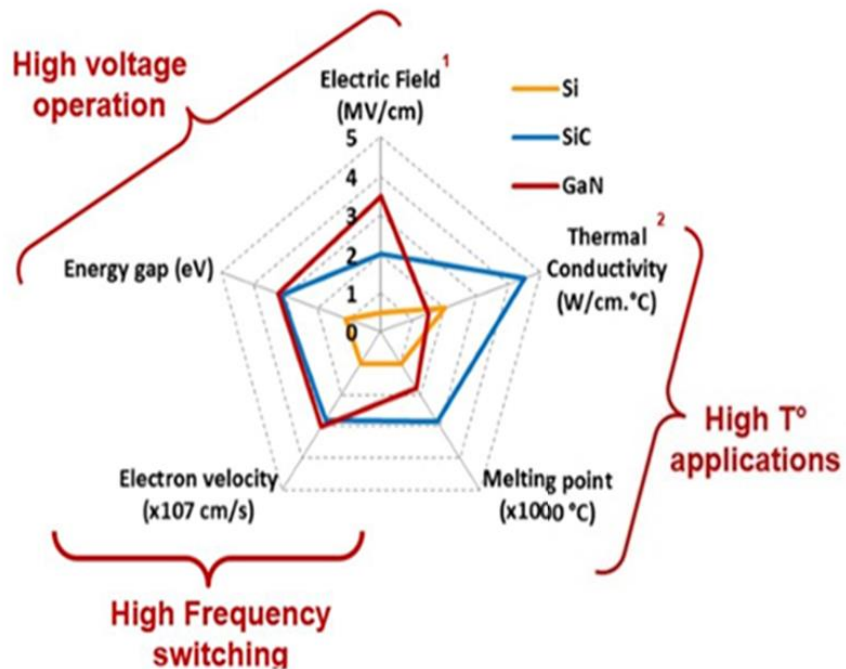


- ✓ Efficiency
- ✓ Cost Savings
- ✓ Power Density

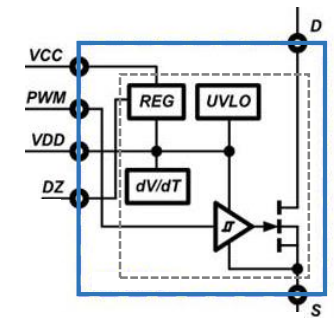
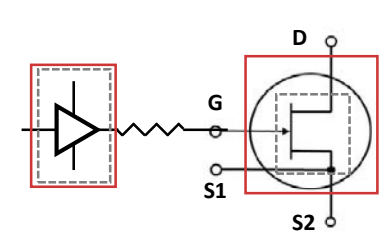
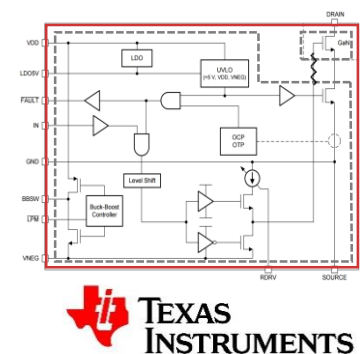
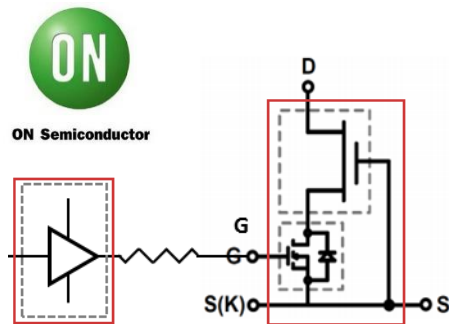


# Unlocking GaN's Value

## Fundamental GaN Material Properties



transphorm

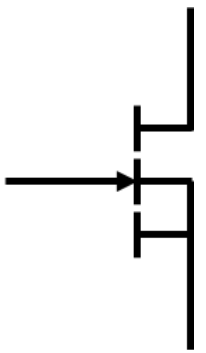




# World's First GaN Power ICs



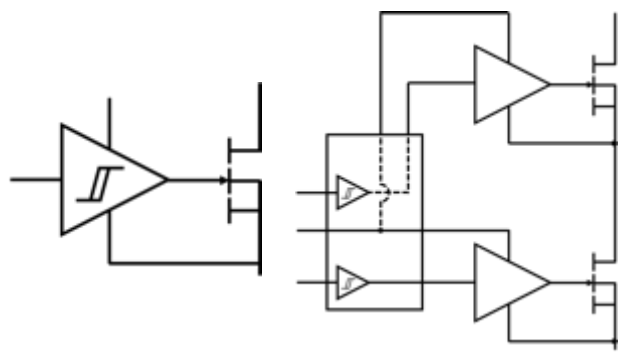
**Fastest, most efficient  
GaN Power FETs**



>20x faster than silicon  
>5x faster than cascoded GaN  
Proprietary design



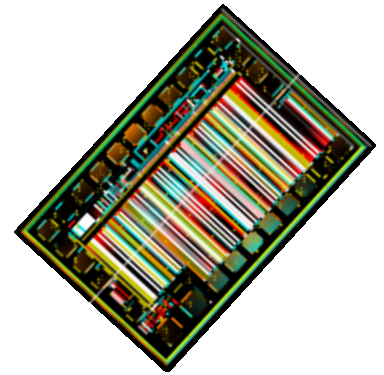
**First & Fastest Integrated  
GaN Gate Drivers**



>3x faster than any other gate driver  
Proprietary design  
75+ patents granted/applied



**World's First  
GaNFast™  
Power ICs**



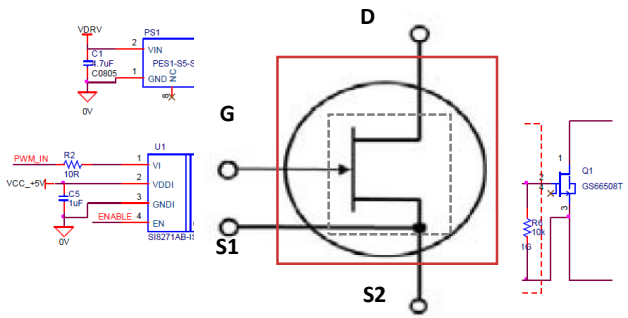
**Up to 5x higher density & 20% lower system cost**



# The Drive for Better Drivers

- Low  $V_{TH}$
- Low  $R \times Q$
- Low  $V_{GS\_Max}$

## Discrete FET + Discrete Driver



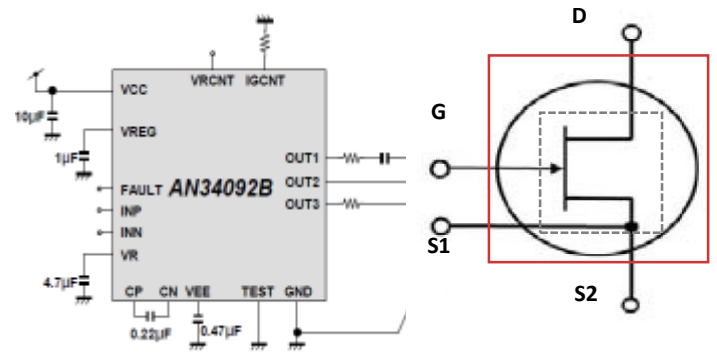
Gate Drive Challenges	Discrete FET + Discrete Driver	Discrete FET + Custom driver	GaN Power IC
Eliminate Gate Oscillations	✓		
Eliminate dV/dt Induced Turn-on	✓		
Regulate Gate Drive Voltage	✓		
Gate Overvoltage Protection	✓		
Reduce Design Complexity	✗		
Manage Noise Sensitivity	✗		
Fast Turn-on/off Speed	✗		
Gate ESD Protection	✗		
Layout Insensitive	✗		
Lowest PCB Area	✗		
Lowest Cost	✗		
Remove Negative Drive	✗		
Fast Start-up	✓		
Eliminate Standby Loss	✓		



# The Drive for Better Drivers

- Low  $V_{TH}$
- Low  $R \times Q$
- Low  $V_{GS\_Max}$

## Discrete FET + Custom Driver



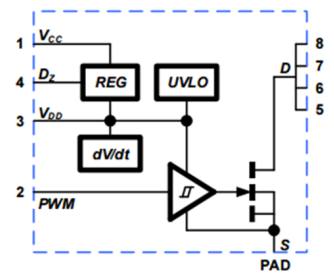
Gate Drive Challenges	Discrete FET + Discrete Driver	Discrete FET + Custom driver	GaN Power IC
Eliminate Gate Oscillations	✓	✓	
Eliminate dV/dt Induced Turn-on	✓	✓	
Regulate Gate Drive Voltage	✓	✓	
Gate Overvoltage Protection	✓	✓	
Reduce Design Complexity	✗	✓	
Manage Noise Sensitivity	✗	✓	
Fast Turn-on/off Speed	✗	✓	
Gate ESD Protection	✗	✗	
Layout Insensitive	✗	✗	
Lowest PCB Area	✗	✗	
Lowest Cost	✗	✗	
Remove Negative Drive	✗	✗	
Fast Start-up	✓	✗	
Eliminate Standby Loss	✓	✗	



# The Drive for Better Drivers

- Low  $V_{TH}$
- Low  $R \times Q$
- Low  $V_{GS\_Max}$

## GaN Power IC



**No compromises**

Gate Drive Challenges	Discrete FET + Discrete Driver	Discrete FET + Custom driver	GaN Power IC
Eliminate Gate Oscillations	✓	✓	✓
Eliminate dV/dt Induced Turn-on	✓	✓	✓
Regulate Gate Drive Voltage	✓	✓	✓
Gate Overvoltage Protection	✓	✓	✓
Reduce Design Complexity	✗	✓	✓
Manage Noise Sensitivity	✗	✓	✓
Fast Turn-on/off Speed	✗	✓	✓
Gate ESD Protection	✗	✗	✓
Layout Insensitive	✗	✗	✓
Lowest PCB Area	✗	✗	✓
Lowest Cost	✗	✗	✓
Remove Negative Drive	✗	✗	✓
Fast Start-up	✓	✗	✓
Eliminate Standby Loss	✓	✗	✓





# Clean, Controlled, Easy to Use

GaNFast™

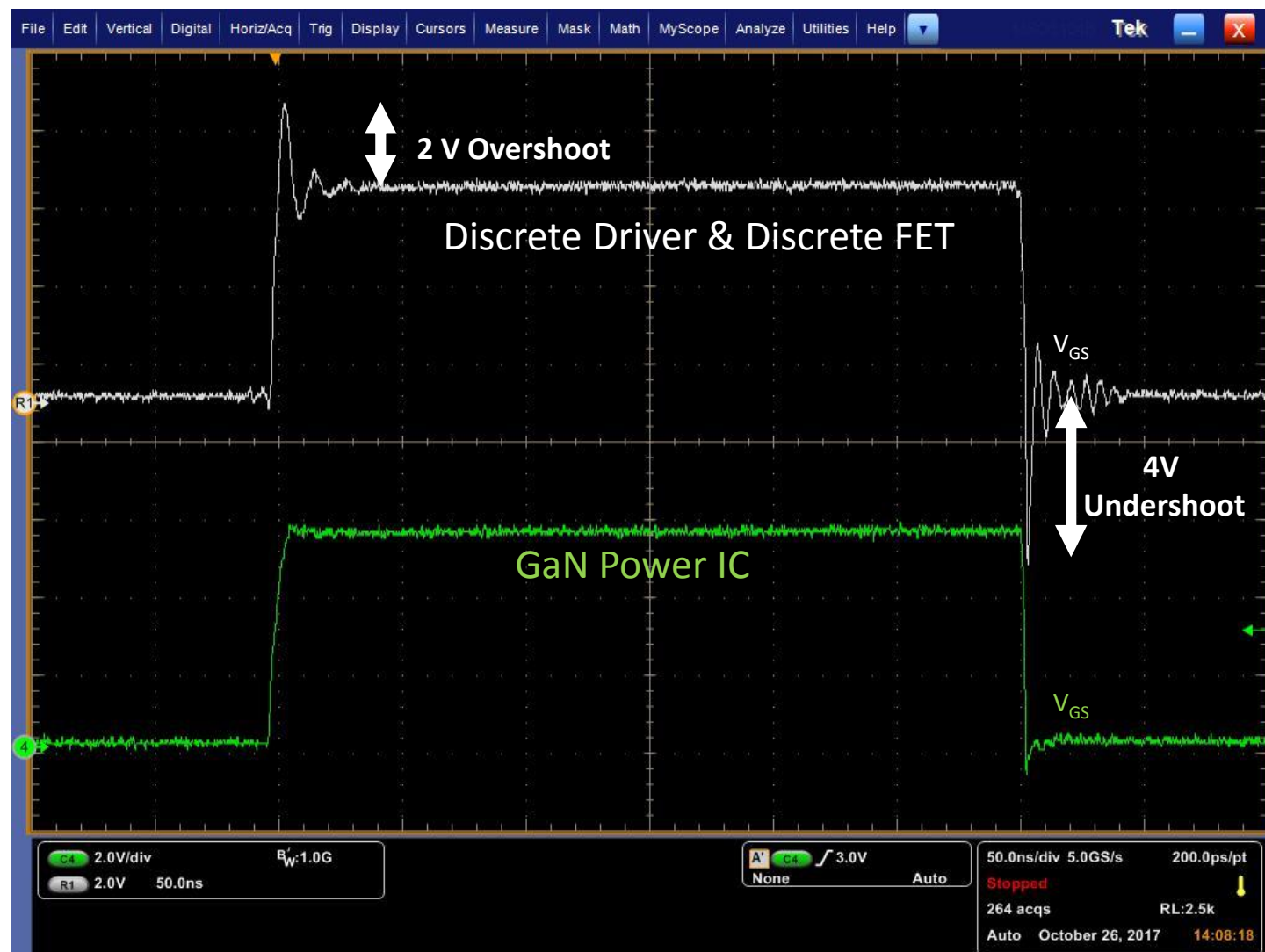
- **Discrete driver**

- Gate loop inductance creates overshoot (even with good layout)
- Reliability concern

- **GaNFast™ GaN Power IC**

- No gate loop parasitic
- Clean and fast gate signal

- GaNFast ICs unlock the efficiency, cost, and power density of GaN while making the customer experience easy to use and reliable

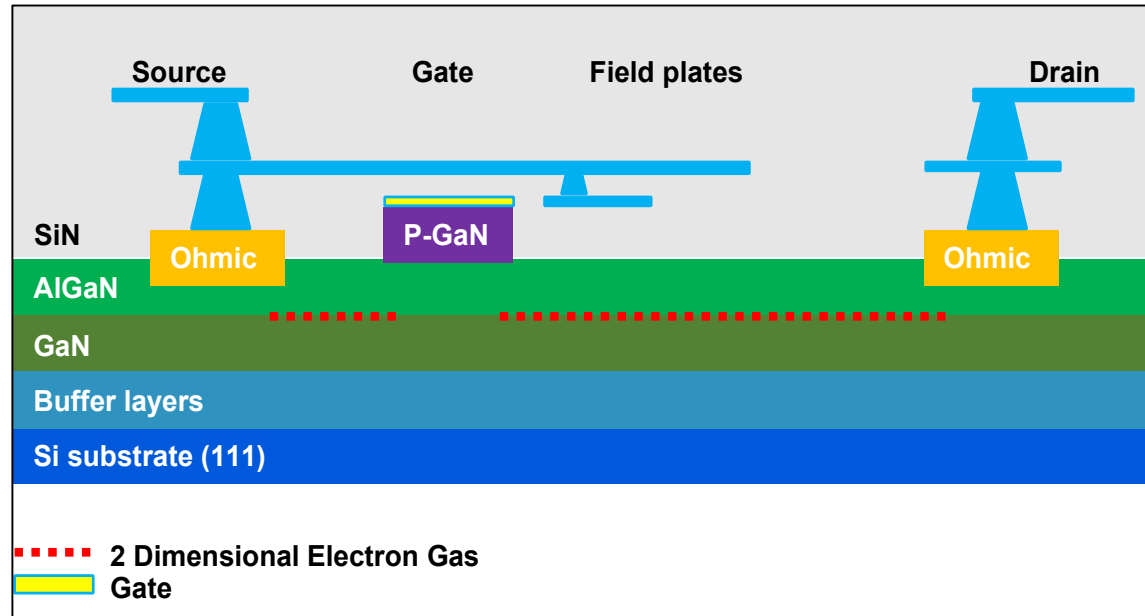




- Why GaN Power IC?
- **How to make GaN Power ICs?**
- Features of GaN Power ICs
- Commercial requirements for GaN products
- Products using GaN Power ICs



# Navitas eMode Power FET Technology



- Lateral device technology → Convenient isolation and easy voltage scaling
- High breakdown field (10X) and high mobility (2X) → Low  $R_{DS(ON)}$ , Low  $Q_{OSS}$
- Lateral device technology → Low  $Q_G$ , easy to drive, easy to integrate
- Third quadrant operation, ie: bidirectional current flow, zero reverse recovery
- Processed in established CMOS line → High yield, high capacity
- Multiple metal technology using standard CMOS processing equipment


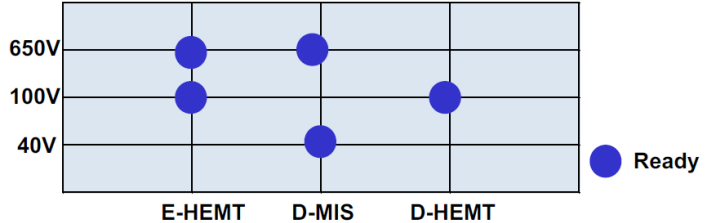


# Navitas' Unique Characteristics: Fabless with its own PDK



3

### GaN device offering

Technology	Function	Application
650V E-HEMT	AC-DC, DC-AC	Adaptor, Motor controller, PV inverter
650V D-MIS	AC-DC, DC-AC	Adaptor, Motor controller, PV inverter
100V E-HEMT	DC-DC	IBC, Server, Notebook
100V D-HEMT	RF-PA	WiFi, Base station
40V D-MIS	RF-switch	WiFi, Base station


- GaN production since 2015
- Engaged 15 customers/ 53 NTO
- >90% of GaN common tools are shared with CMOS manufacturing

Open Innovation Platform®

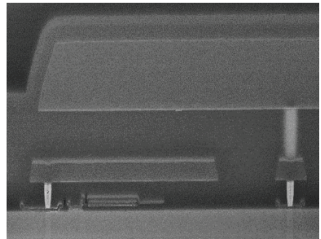
© 2016 TSMC, Ltd

6

### Production Challenges



- Complex epitaxy GaN deposition
- Warp/age/Fragile wafer handling
- 1.5X thick substrate
- Ultra thick metal
- CMOS compatible metallization
- Contamination control



Open Innovation Platform®

© 2016 TSMC, Ltd

GaN HEMT is still an emerging technology in the market.

➔ Majority of GaN technologies and products developed are for high-voltage/power applications.

➔ Also, GaN devices are only available in unipolar n-type.

Navitas team has strong knowledge and capability to develop its own device and circuit libraries even with such handicaps.



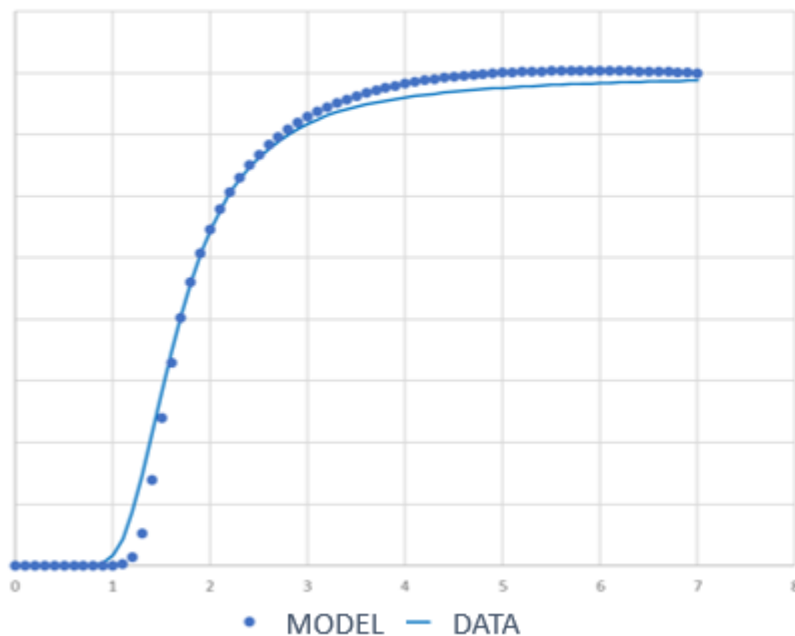
- Excellent process design kit:
  - Device symbols
  - Pcells for automated device construction
  - Scalable, accurate
  - Verified for schematic and layout rules
  - Layout parameter extraction
- Angelov, ASM and silicon models are not suitable
  - Lack dMode, scalability, flexibility, speed
- Navitas GaN eMode FET scalable VerilogA model
  - Flexible: customized features/equations
  - High correlation between simulation and product
  - High-speed simulations



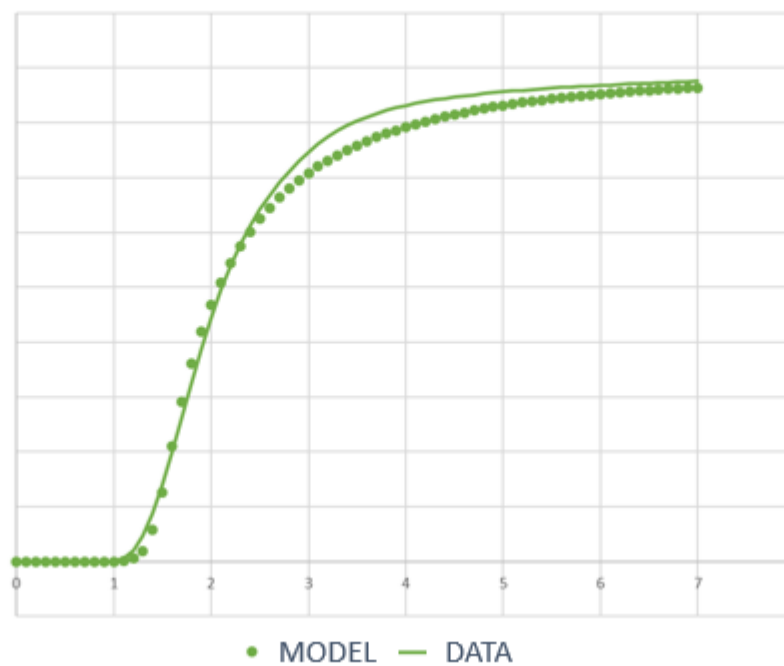
# Accurate over Temperature

- GaN FET  $I_D V_G$  Model with Temperature Effects
  - Solid lines = measured, dotted lines = Cadence simulation

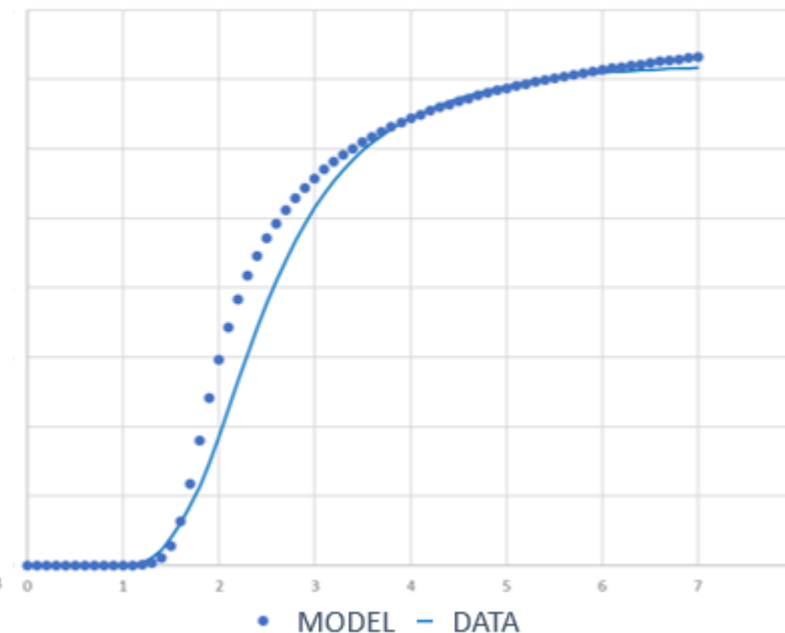
IDLIN/VG -40C



IDLIN/VG 25C



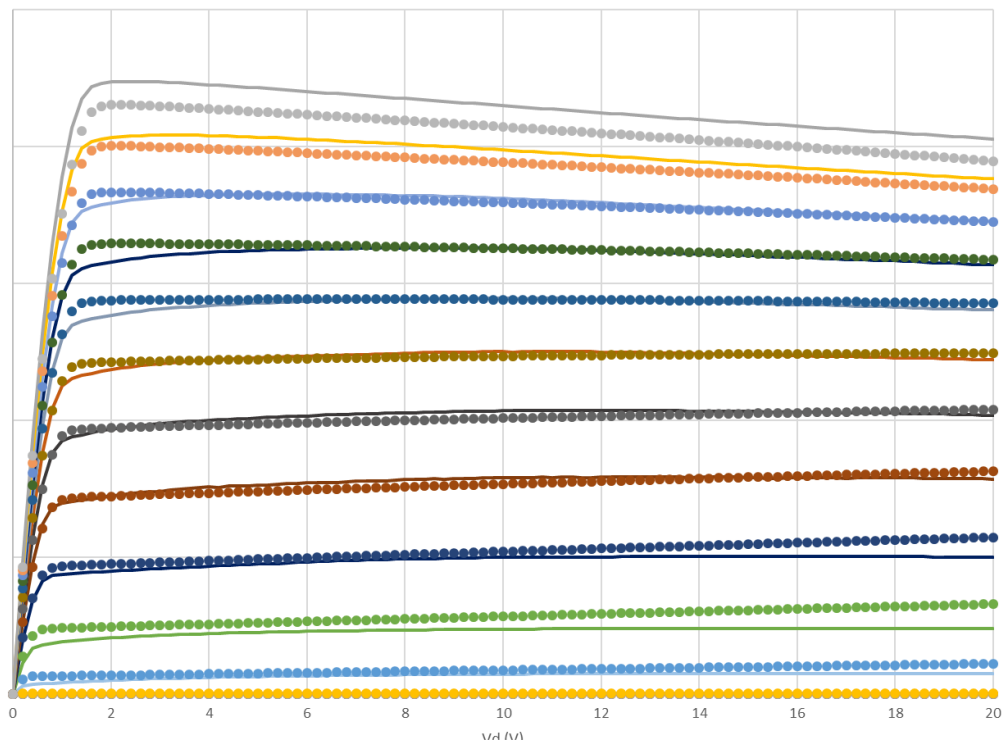
IDLIN/VG 125C



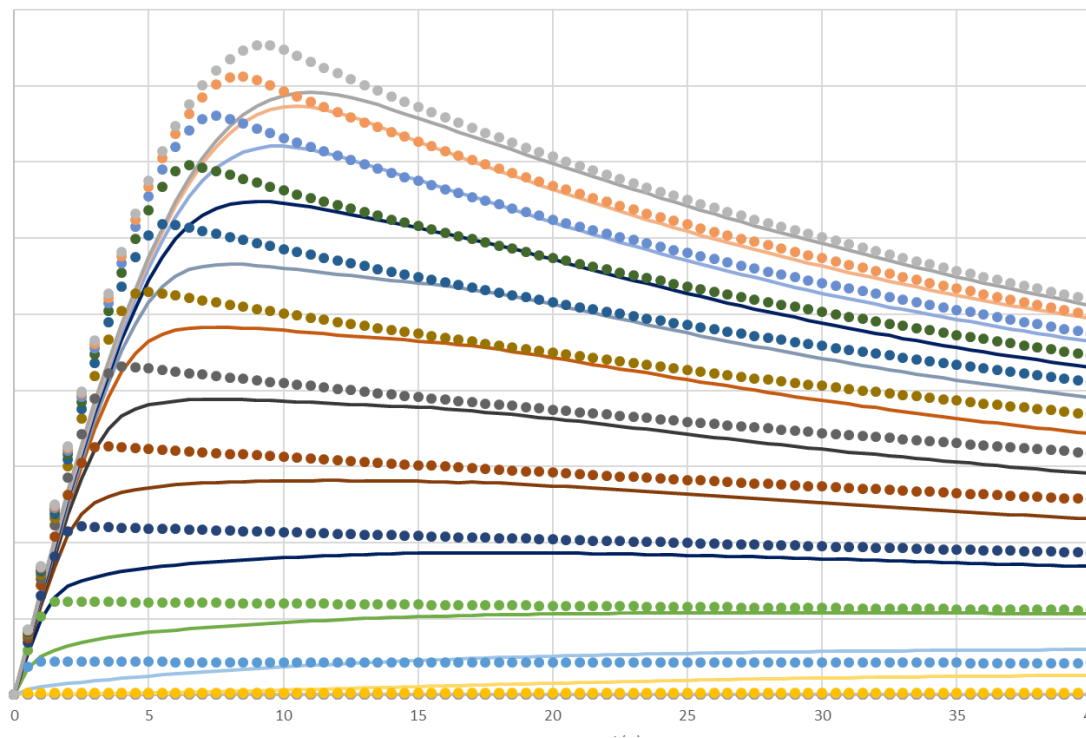


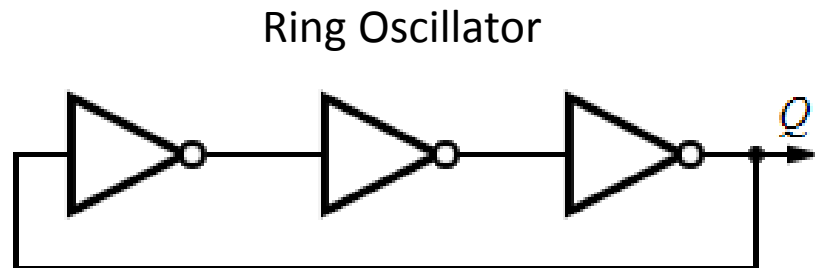
# Accurate over Drain Voltage

- Solid lines = measured, dotted lines = Cadence Spectre
- 20V rated eMode FET

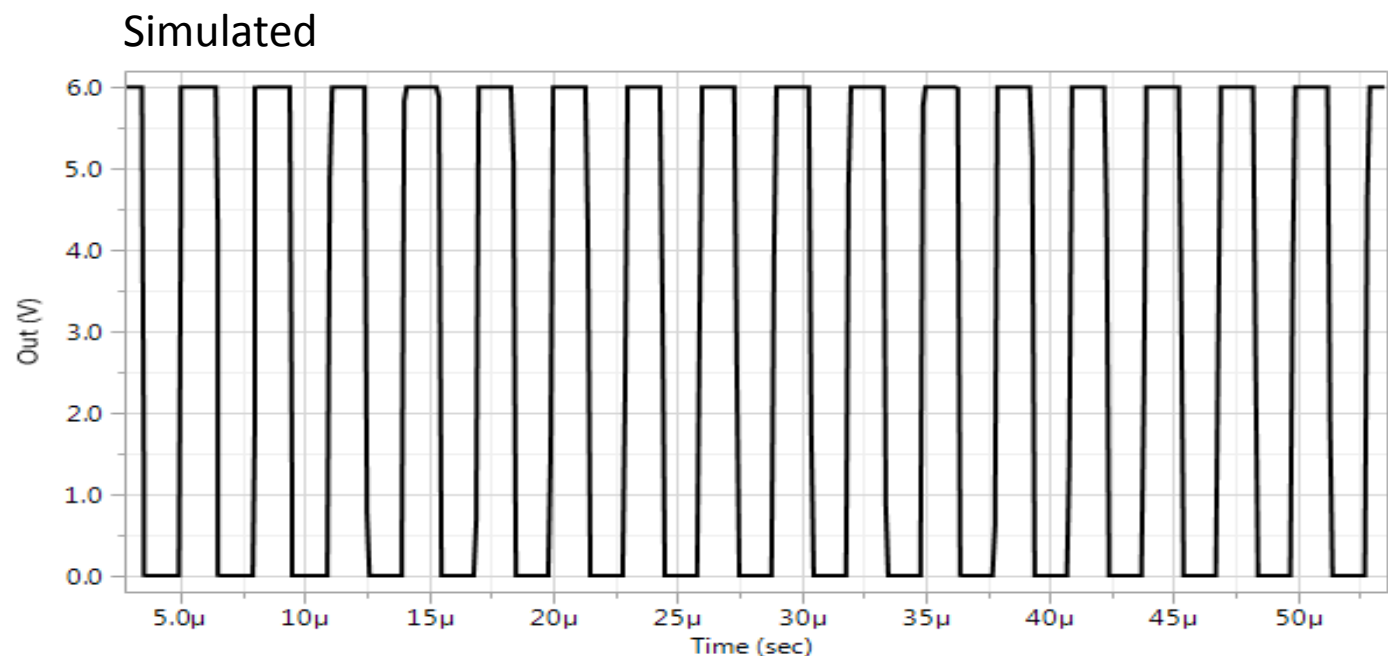
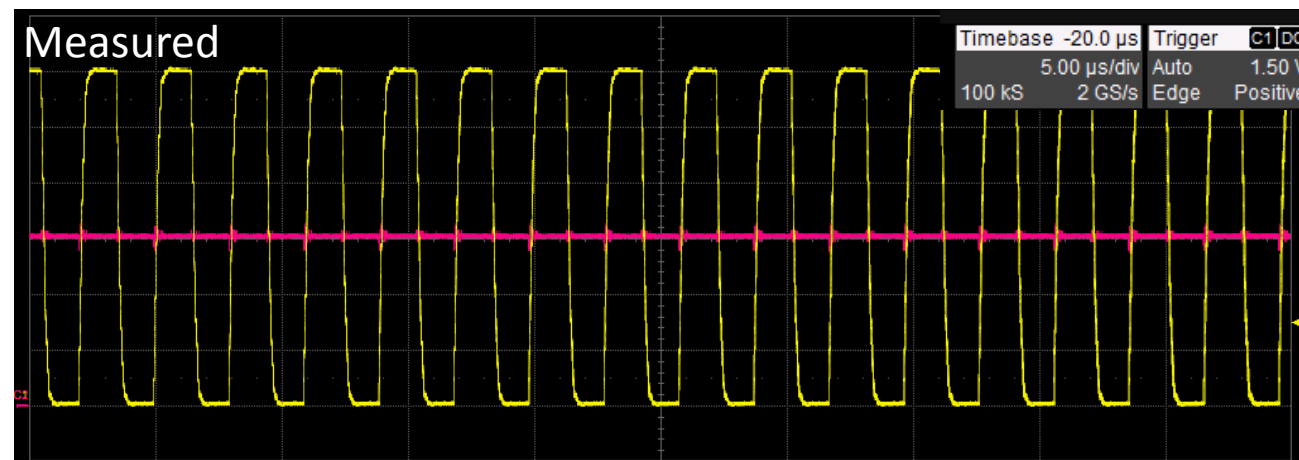


## 650V rated eMode FET





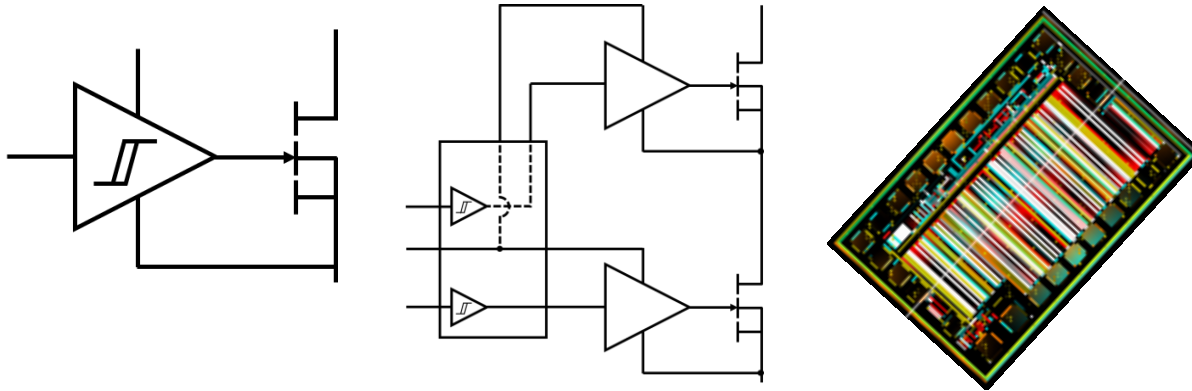
- Use simple ring oscillator structure to verify accuracy of PDK models
- Excellent agreement between simulated and measured performance
- Needs to include parasitic effects







First & Fastest Integrated GaN Gate Drivers



Navitas GaN IC PDK

- PDK developed independent of the foundry
- Offers great deal of design flexibility
- Fast design/tape out cycle time
- Enables seamless integration of new devices and features
- Scalable models, streamlined for process corners

Navitas Proprietary GaN Building Blocks

- eMode and dMode transistors (7V - 650V)
- Integrated capacitors (7V – 650V)
- Integrated resistors
- Inverters
- Buffers
- Logic gates
- Pulse generators
- Level shifters
- ESD I/O circuits



- Why GaN Power IC?
- How to make GaN Power ICs?
- **Features of GaN Power ICs**
- Commercial requirements for GaN products
- Products using GaN Power ICs





# Integrated Drive → Simple & Robust

GaNFast™

Wide Range  $V_{CC}$   
(10-30V)

Total layout flexibility  
& simplicity

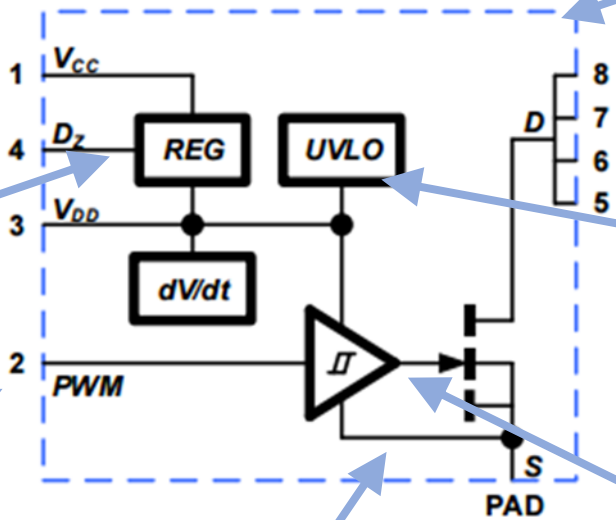
Regulator ensures  
 $V_{GS}$  within SOA

Under voltage lockout protects the  
driver & FET when full power supply  
is not available

PWM Hysteresis for  
noise immunity

Gate protected from external noise  
(Not pinned out of package)

No inductance or  
ringing in gate loop

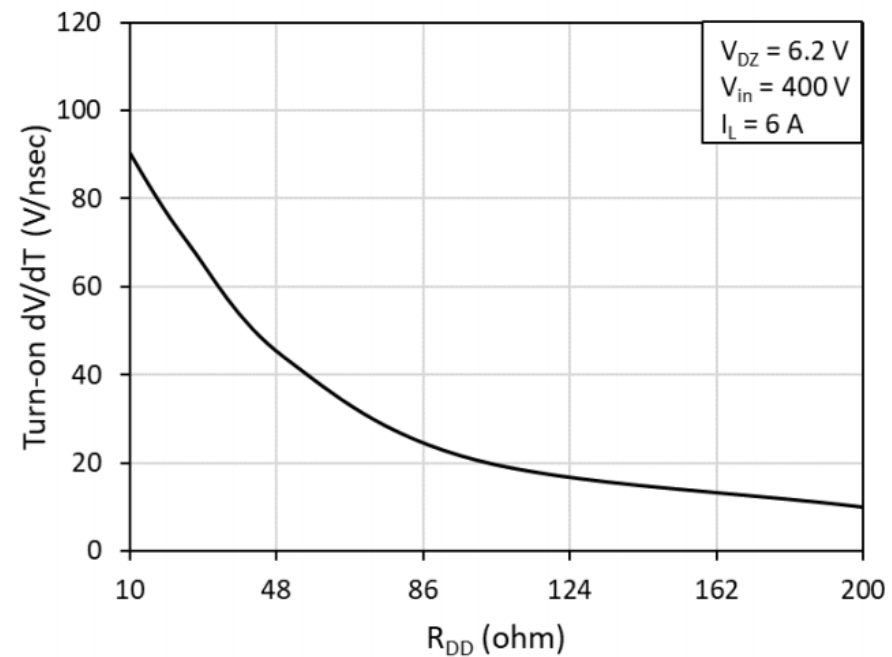
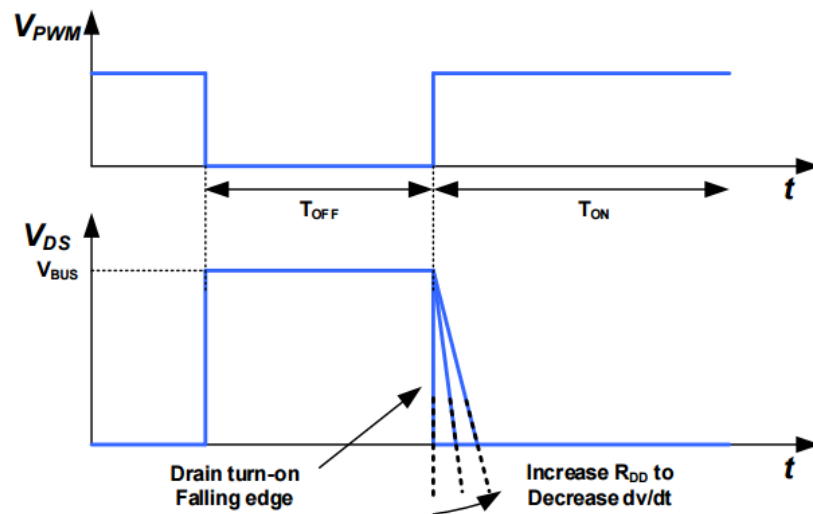
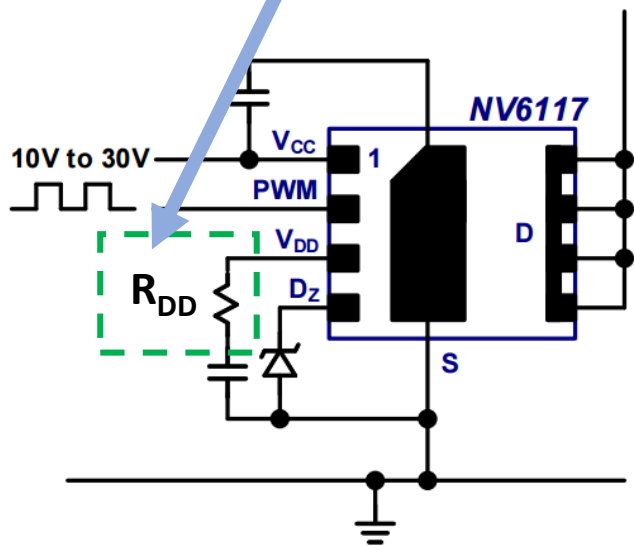




# Voltage Slew Rate Control ... Easy EMI Tuning



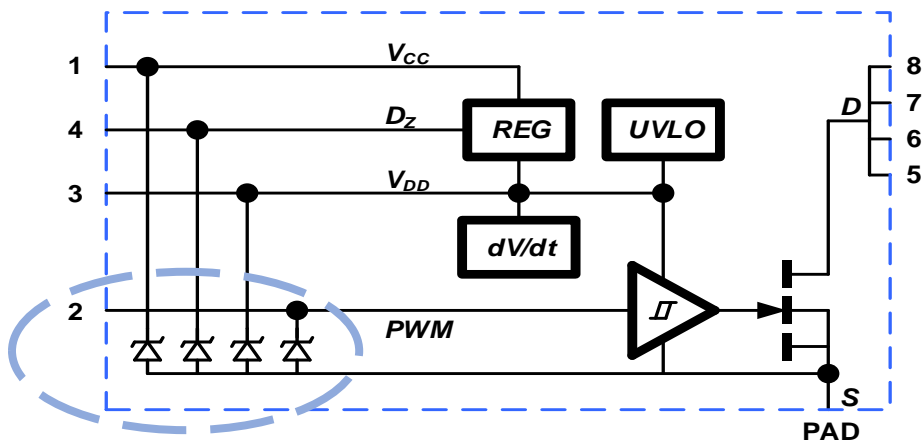
$dV/dt$  controllable with  $R_{DD}$  from 10 V/ns to 90 V/ns





# Integrated ESD Protection

## GaN Power IC



Integrated ESD Protection

HBM, CDM > 1,000 V

## ESD Qualification Tests

Reference	Test Conditions	Duration	Lots	S.S.
JS-001-2014	Human Body Model ESD	N/A	1	3
JS-002-2014	Charged Device Model ESD	N/A	1	3

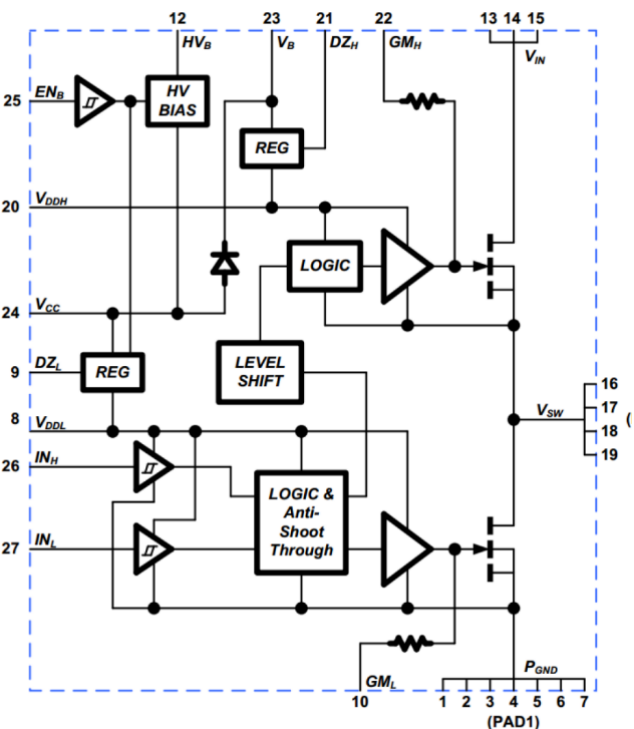
- ✓ Same ESD testing as Si devices can be applied to GaN
- ✓ Latch up testing not required in GaN devices



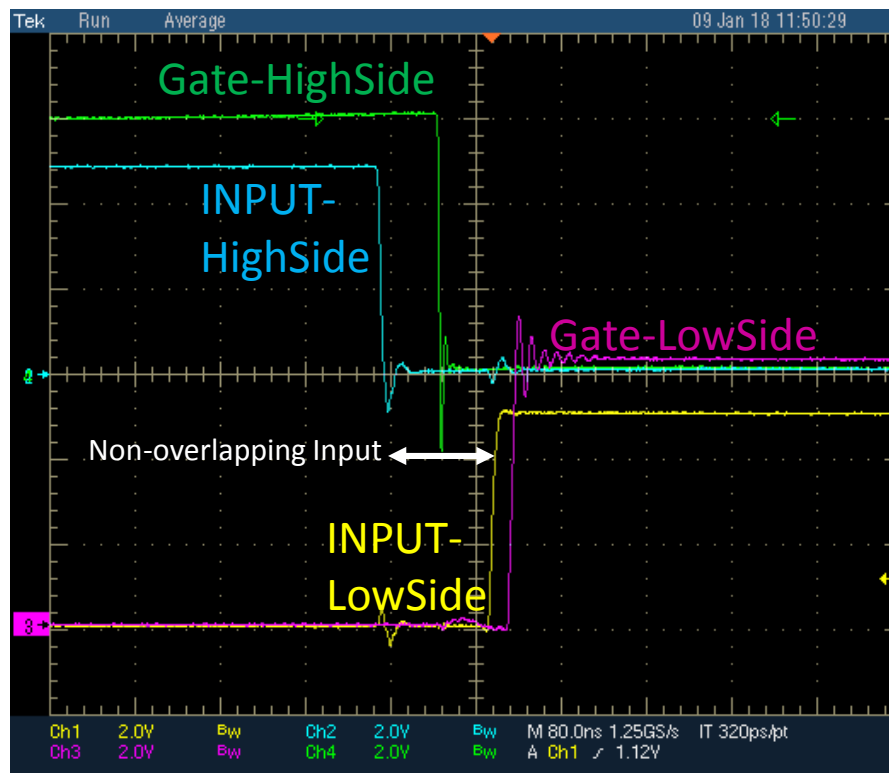
# Shoot-Through Protection in Half-Bridge



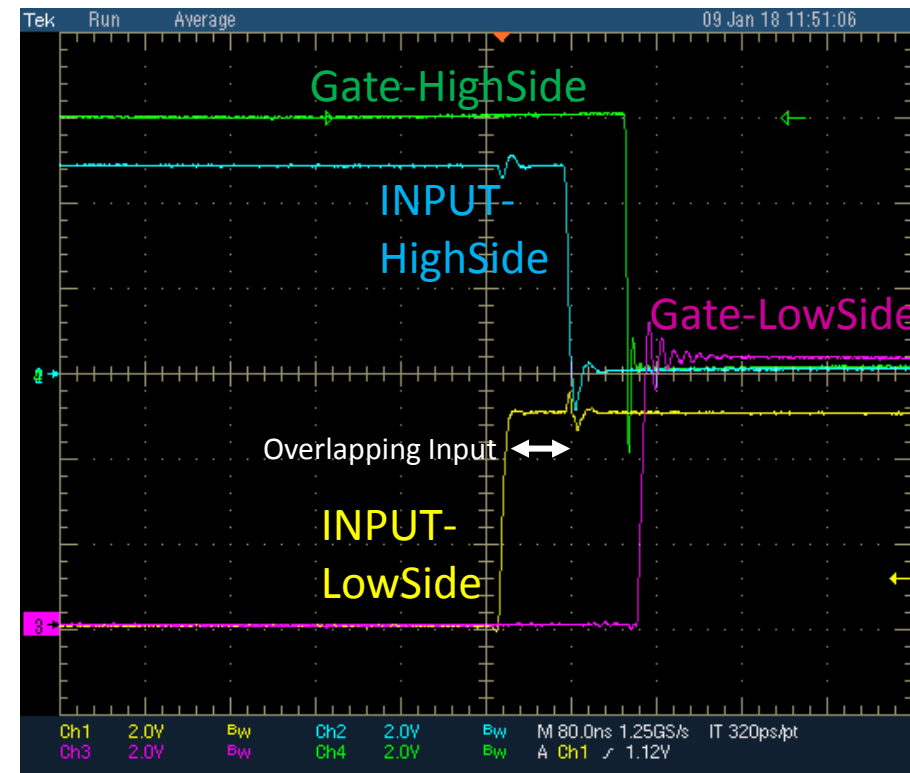
Half-Bridge GaN Power IC



Non-Overlapping Logic Input  
(Typical Operation)



Overlapping Logic Input  
(Power IC Protection Mode)

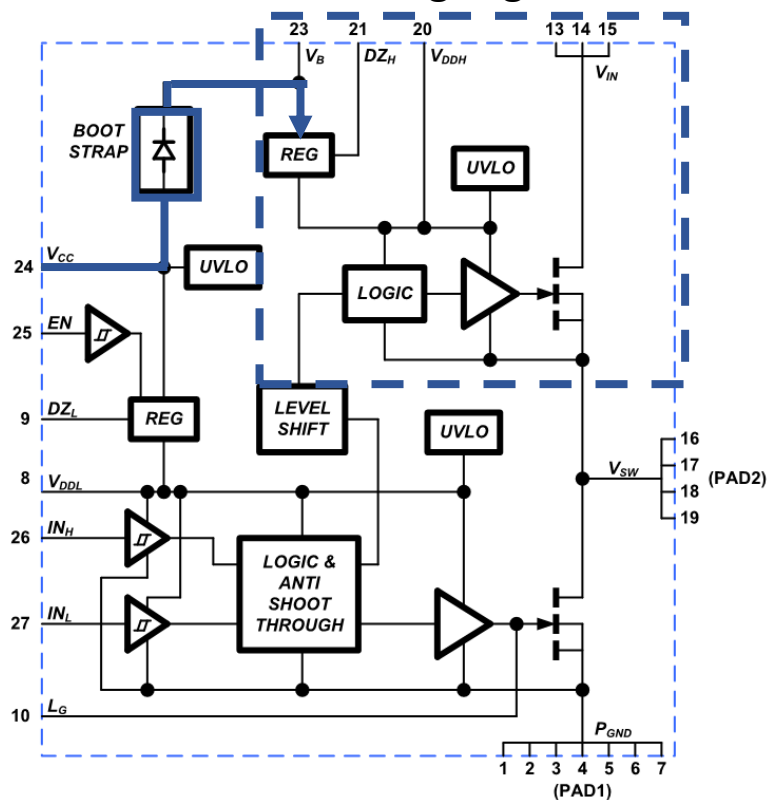


High-side and Low-side gates never overlap due to shoot-through protection in power IC

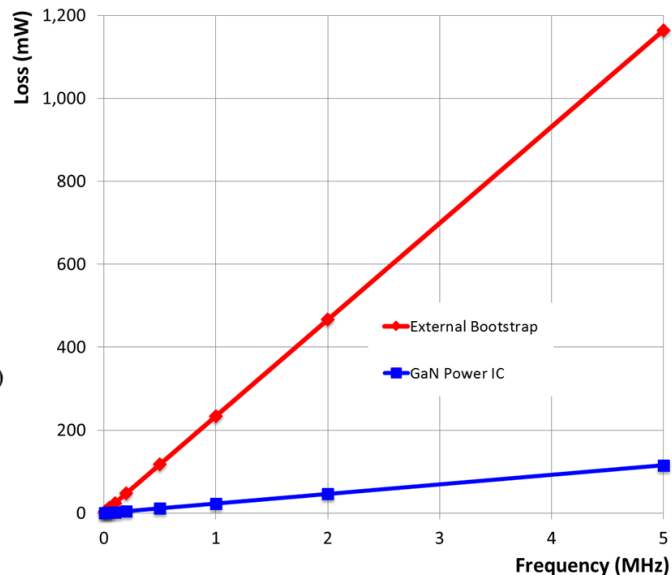


# Integrated Bootstrap

## Floating High Side



External diode ES1J (600 V, 1 A,  $V_f = 1.7V$  at 1 A, SMA)



## Bootstrap Diode Loss

$$f(C_{diode}, Q_{rr}, F_{sw})$$

## Bootstrap Diode Integration Benefits:

- Avoids risk of dV/dt induced diode failure
- Eliminates diode  $C_j$  and  $I_{rr}$  power loss
- Eliminates necessity of using SiC at high  $F_{sw}$
- Saves cost, especially if SiC is required
- Charges bootstrap capacitor losslessly
- Assures full charge/voltage is delivered
- Eliminates lossy current limiting resistor
- Saves board space in HV system

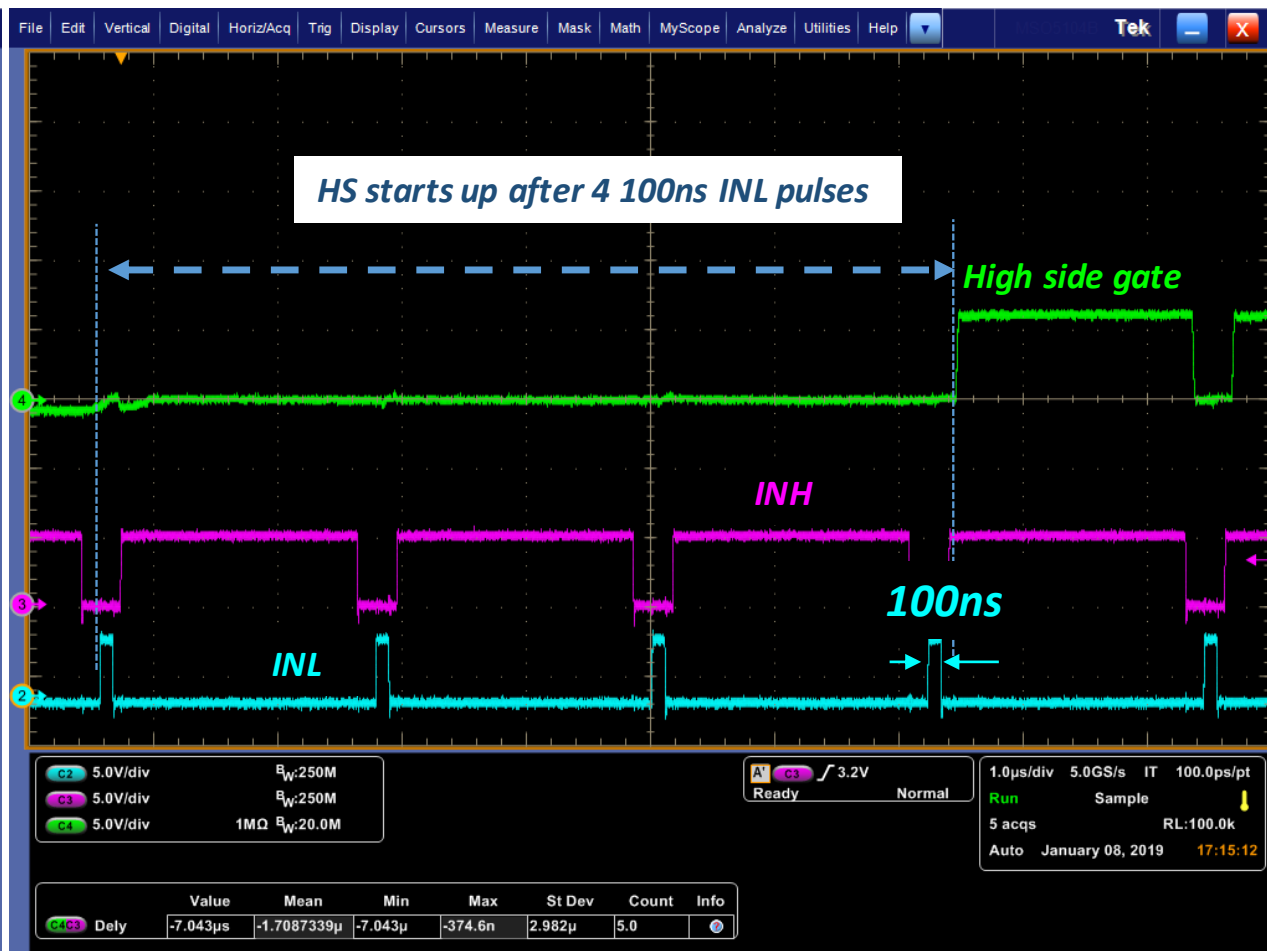
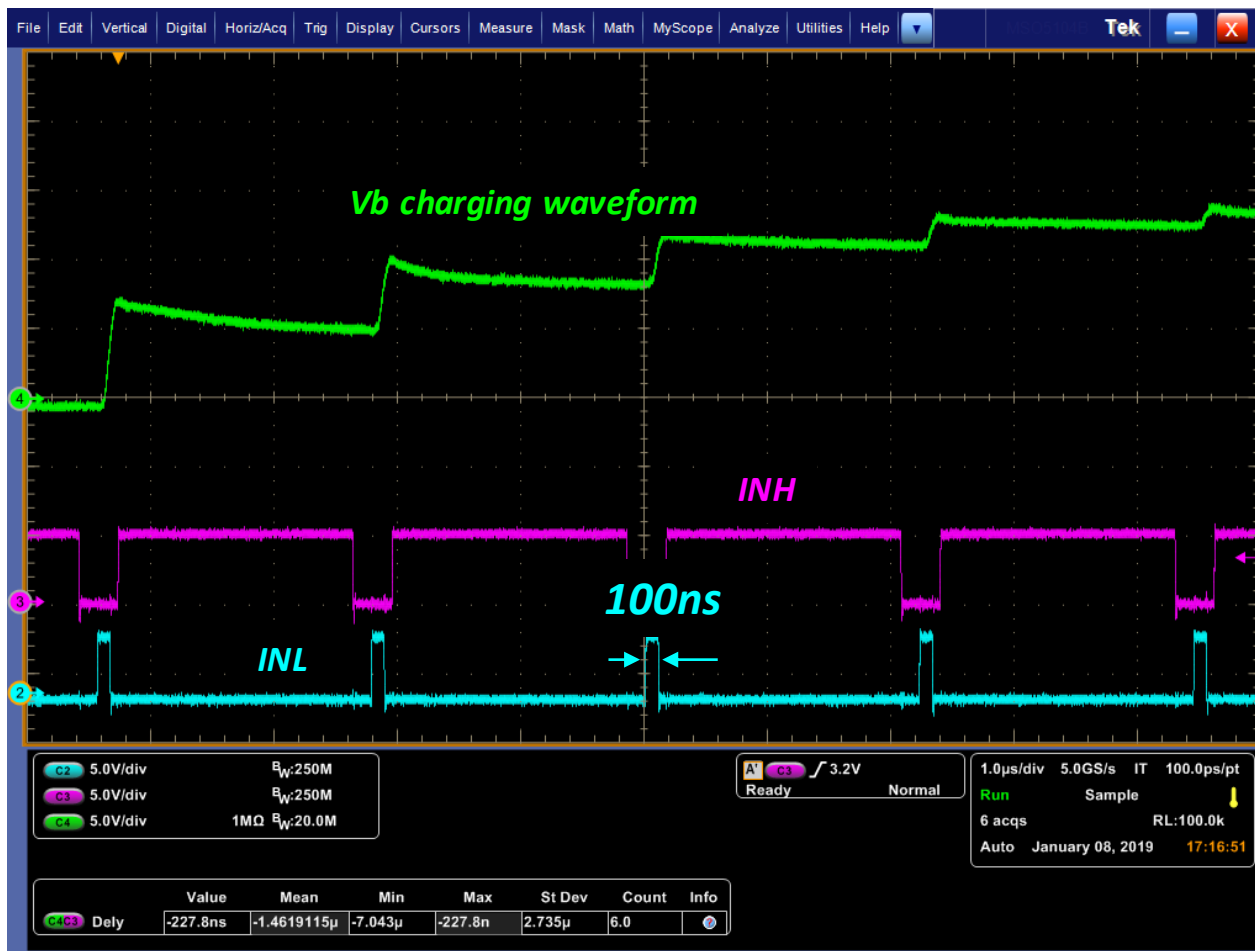
<https://www.onsemi.com/pub/Collateral/ES1J-D.PDF>





# Bootstrap Startup

## High-side Startup Characteristics





- Why GaN Power ICs?
- How to make GaN Power ICs?
- Features of GaN Power ICs
- **Commercial requirements for GaN products**
- Products using GaN Power ICs



- ✓ System Value (Features, Efficiency, Density)
- ✓ Reliability
- ✓ Cost





- ✓ System Value (Features, Efficiency, Density)
- ✓ Reliability
- ✓ Cost





# Approach to Reliability of GaN Power ICs

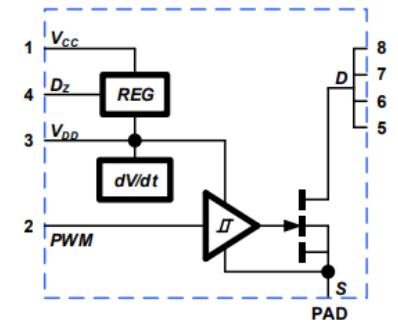
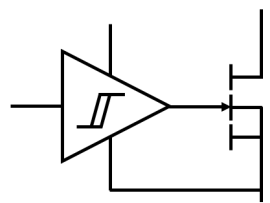
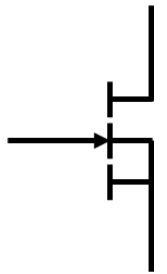


Well Established Package Technology

650 V GaNFast Power FETs

Integrated GaN Gate Driver

GaNFast™ Power IC with exceptional Quality & Reliability



- Package Qualification**
- UFAST
  - HAST
  - THB
  - TC
  - HTSL

- Traditional FET Tests**
- HTRB
  - HTGB
  - HAST
  - THB

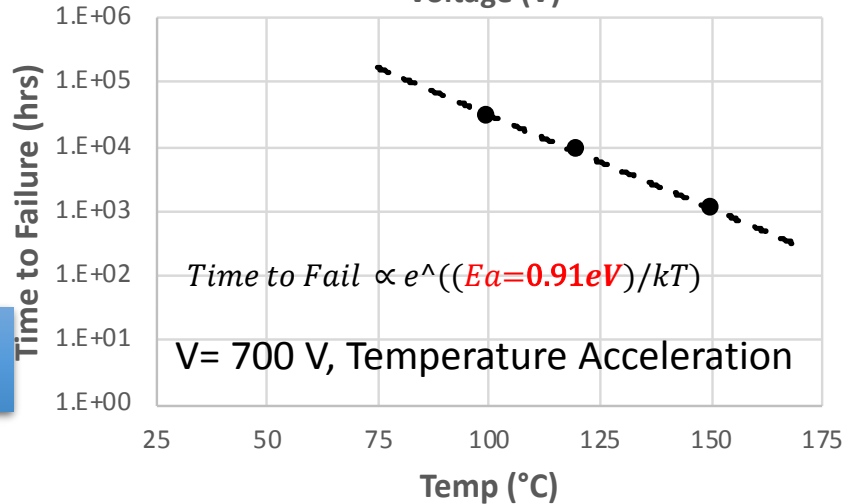
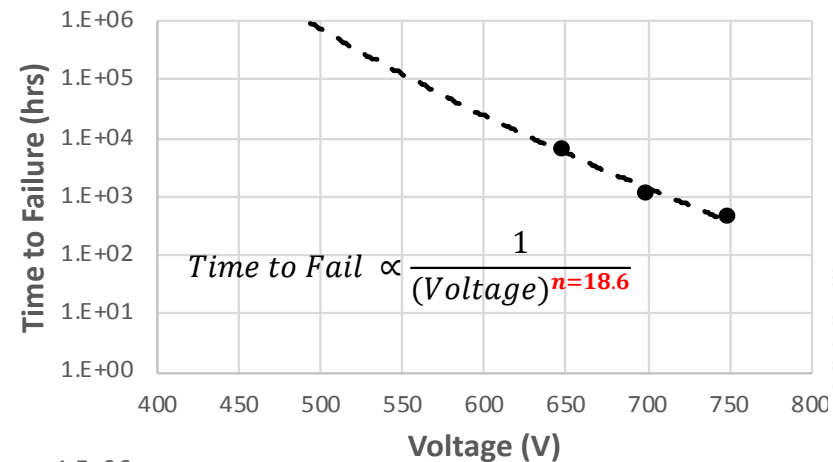
- JESD471 (IC Qual Standard)**
- HTOL
  - ELFR
  - ESD
  - WLR



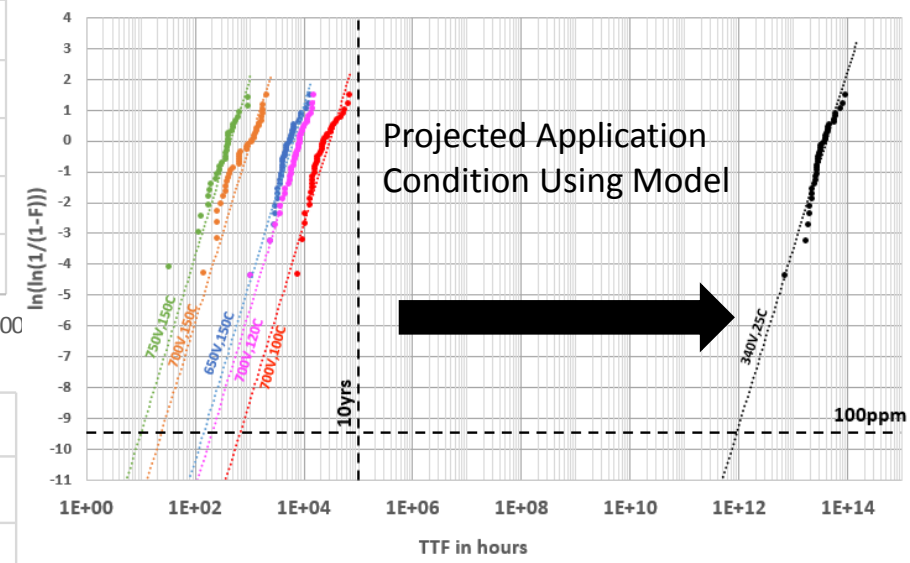
# HTRB Acceleration & Lifetime Models

Voltage/ Temperature	100°C	125°C	150°C
650V			✓
700V	✓	✓	✓
750V			✓

T=150 °C, Voltage Acceleration



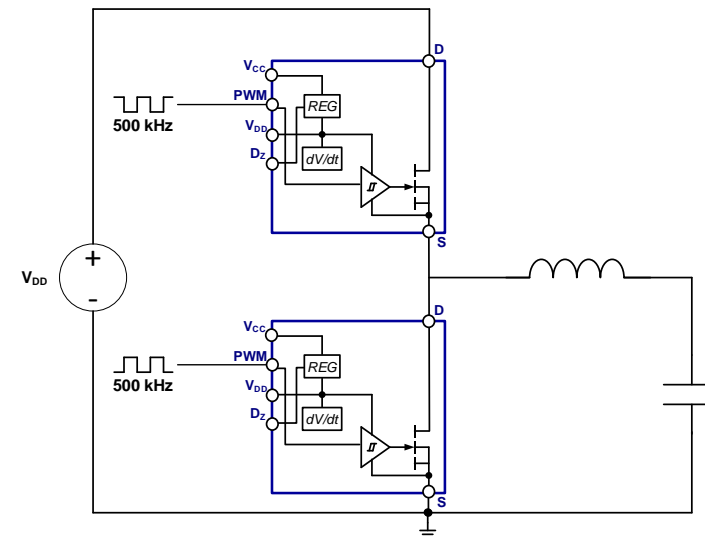
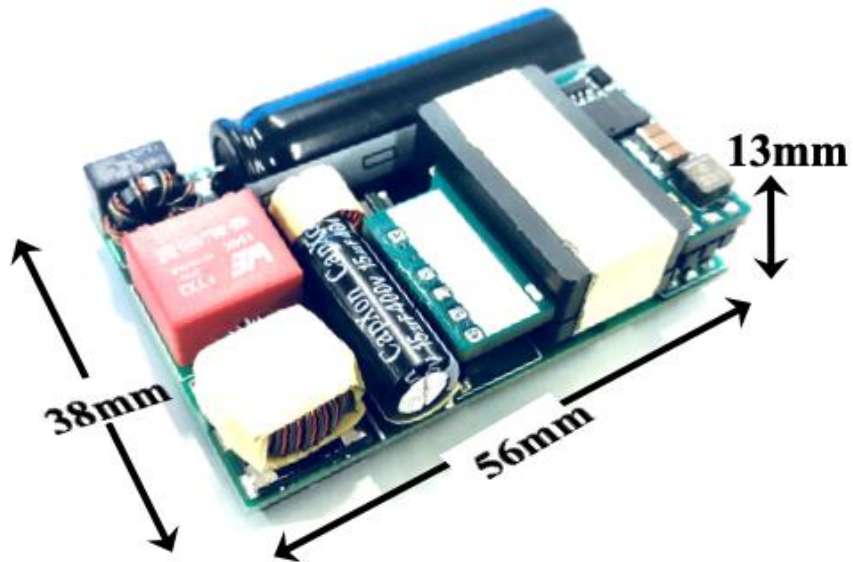
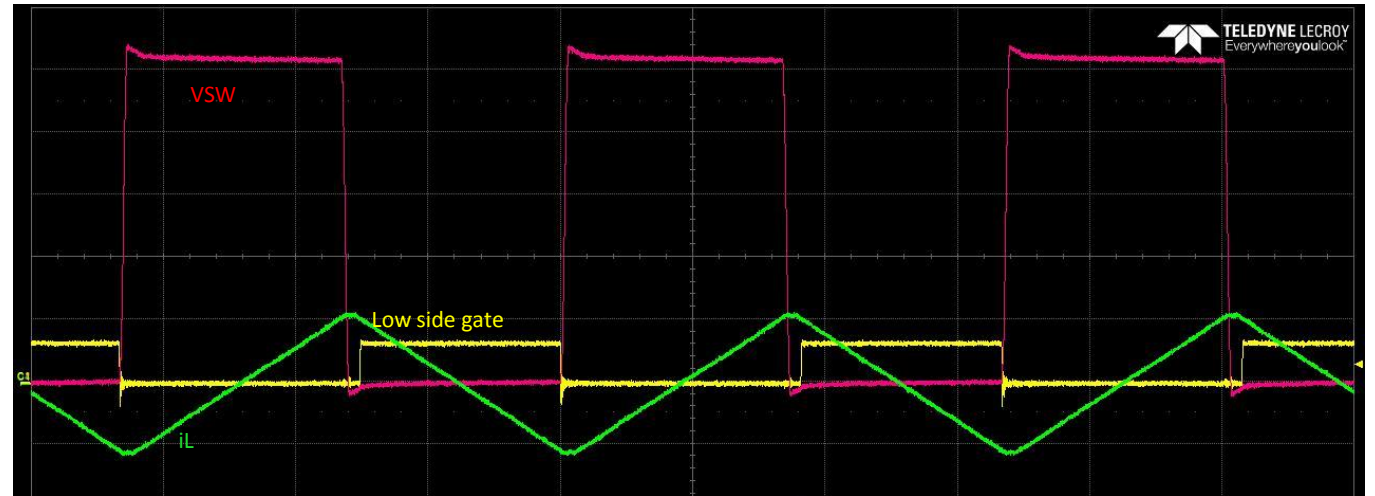
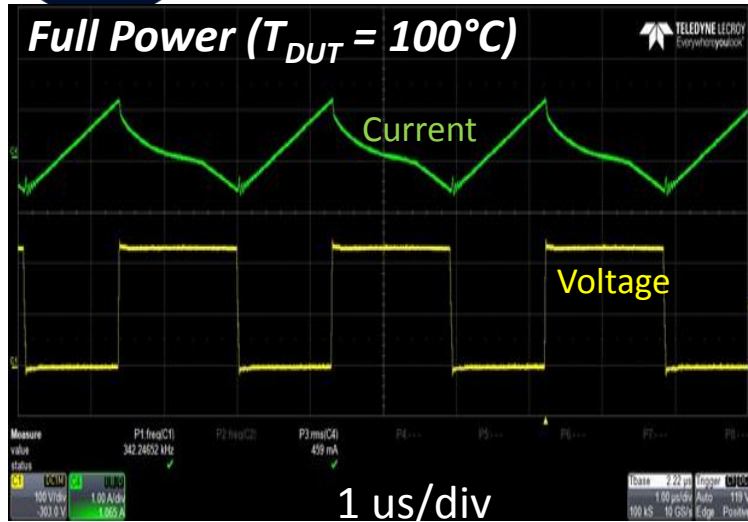
$$Lifetime = A \times (V^{-n}) \times (e^{\frac{E_A}{kT}})$$



Lifetime in no load condition is >1E8 years, significant built-in margin



# Mission Profile Driven HTOL (ZVS)

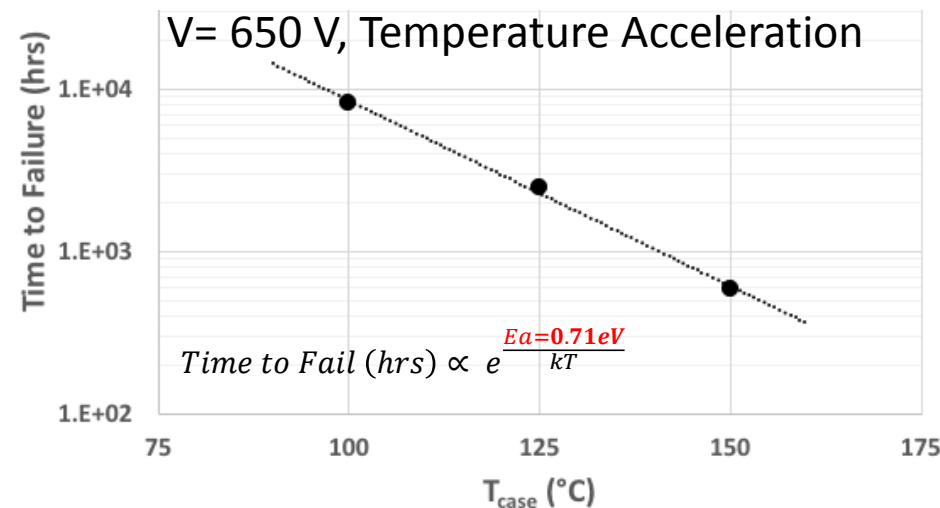
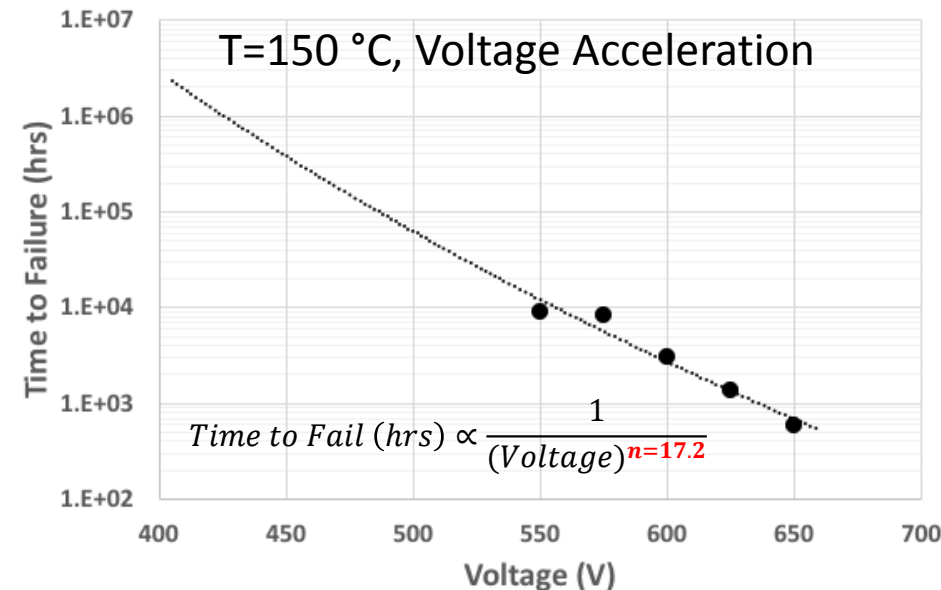


ZVS test bench replicates stresses seen in ACF application



# HTOL-based Lifetime Model

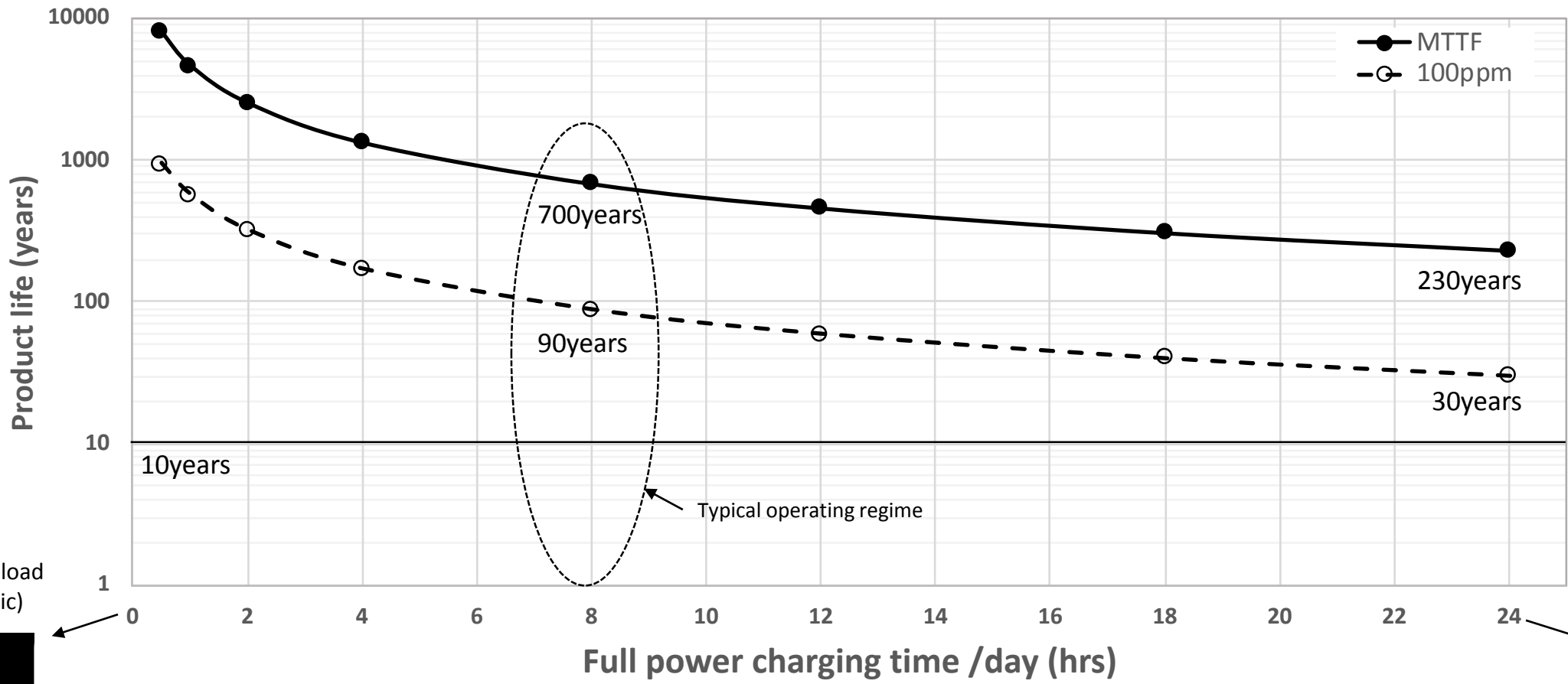
Voltage/ Temperature	100°C	125°C	150°C
550V			✓
575V			✓
600V			✓
625V			✓
650V	✓	✓	✓





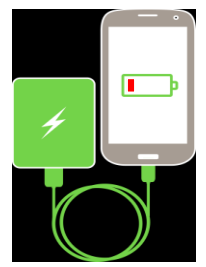
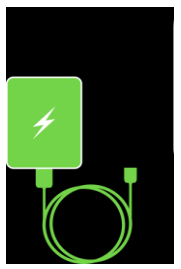


# Lifetime Estimation in Charger Application



100% No load (unrealistic)

100% full power (unrealistic)



Significant built-in reliability margin → even at worst case conditions (exceeds 10+ year lifetime requirement)



- Why GaN Power IC?
- How to make GaN Power ICs?
- Features of GaN Power ICs
- Commercial requirements for GaN products
- **Products using GaN Power ICs**

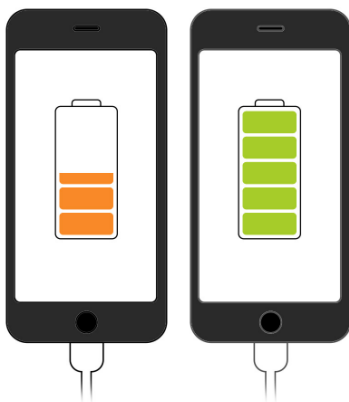


# GaNFast USB-C Chargers Have Arrived



## Fast

Up to 3x more power  
Up to 3x faster charging



## Mobile

Half the size & weight  
of traditional chargers



## Universal

One charger for **ALL** your devices  
**One and Done!!**



Macbook 12"  
Dell XPS 15/13

iPhone XS  
Google Pixel 2

Nintendo Switch  
And more...

### AUKEY



27W



24W



30W

### MADE IN MIND



45W

### RAVPOWER®

45W





# Latest Releases



- **World's smallest 27W USB-C**
- 41.5 cc, 0.65 W/cc
- Available now from [amazon.com](https://www.amazon.com)

- **World's smallest Charger 42W (30W-C + 18W-A) + Battery Pack (5,000 mAh)**
- 31.5 x 85.5 x 81.5 mm
- Available now from [Apple Store](https://www.apple.com)



# Questions?

**GaNFast™**



*Let's go* **GaNFast™**