GaN Reliability Through Integration and Application Relevant Stress Testing

APEC 2018 PSMA Sponsored Industry Session:
"Reliability and Ruggedness – How to Address these Challenges in Wide Bandgap Semiconductor Devices"
Thursday March 8th, 2018

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GaN Device Implementations

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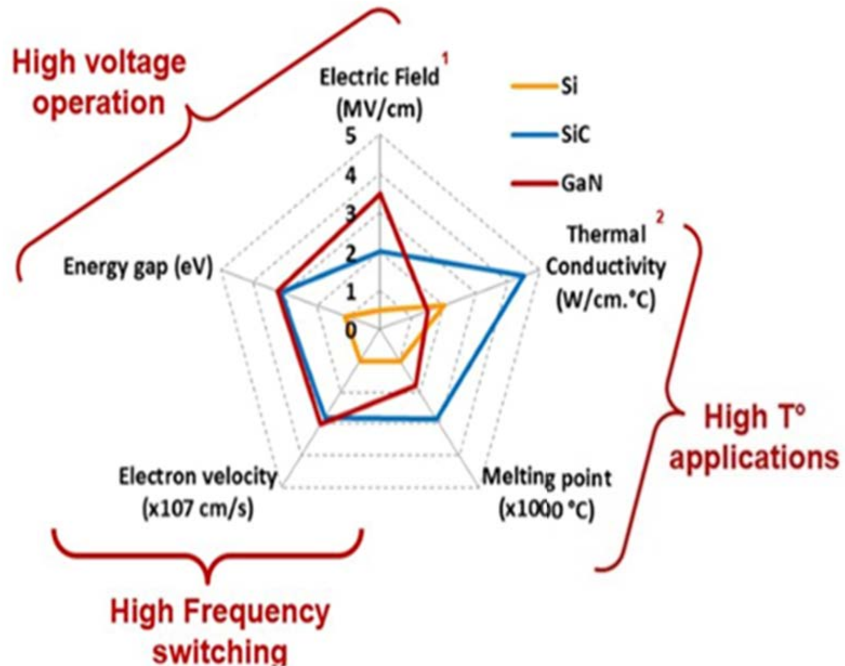
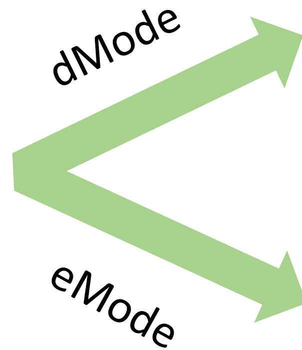
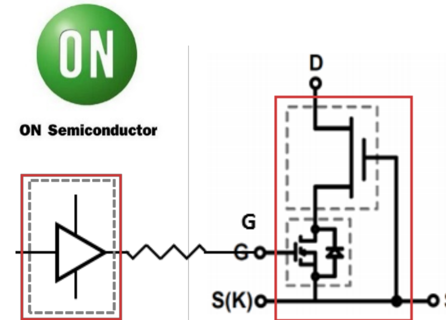
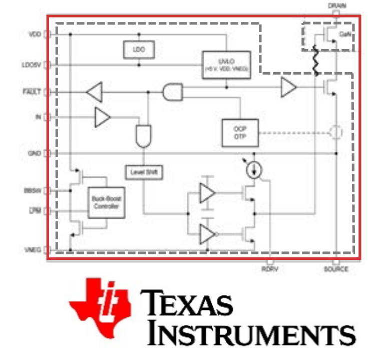
Fundamental GaN Material Properties



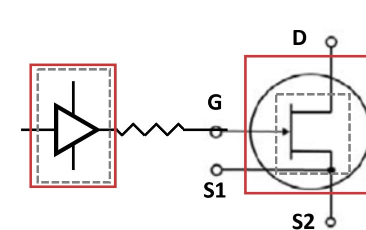


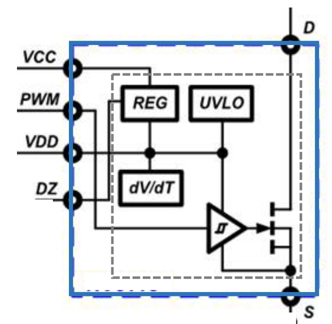
transphorm





Texas Instruments





Panasonic Infineon

GaN Systems EPC EFFICIENT POWER CONVERSION

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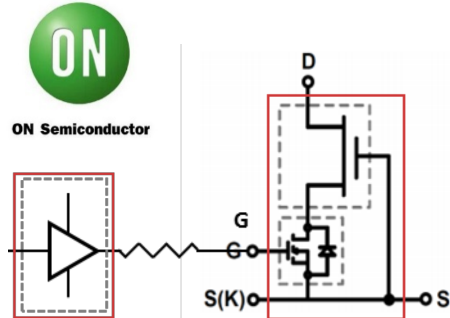
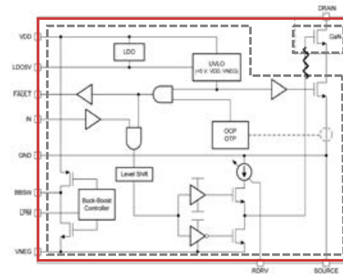
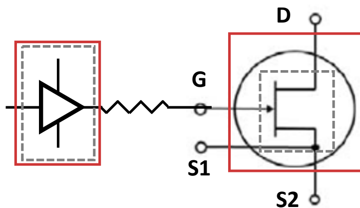
Gate Protection is Paramount in GaN

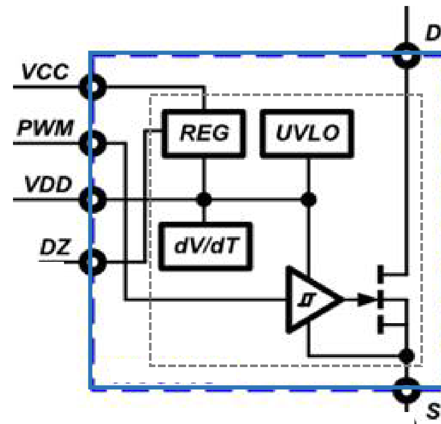




dMode (Dielectric Based Gate)

- Max V_{GS} similar to Si devices
  - Need to manage max negative gate bias on GaN for reliability
- Slew rate control important with multiple chips in a package





eMode (pGaN Based Gate)

- V_{GS} needs to be managed
  - Clamp diodes & current based-drive
  - Layout optimization
  - GaN Power IC (integrated regulator + driver)
- C dv/dt Induced Turn-on concern
  - Negative gate drive
  - Minimize parasitics
  - GaN Power IC (integrated driver)

Clean, Controlled FET Gate

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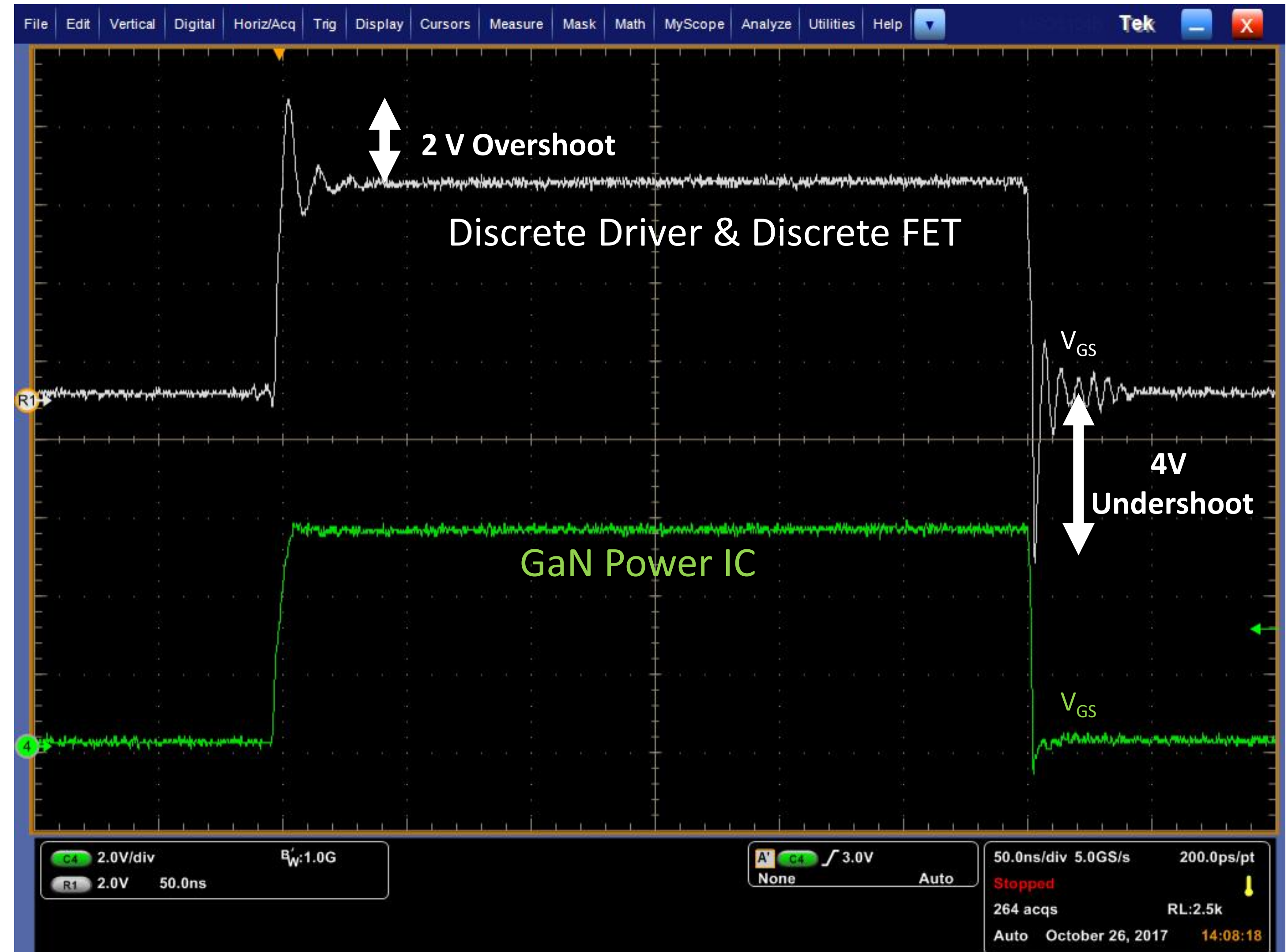
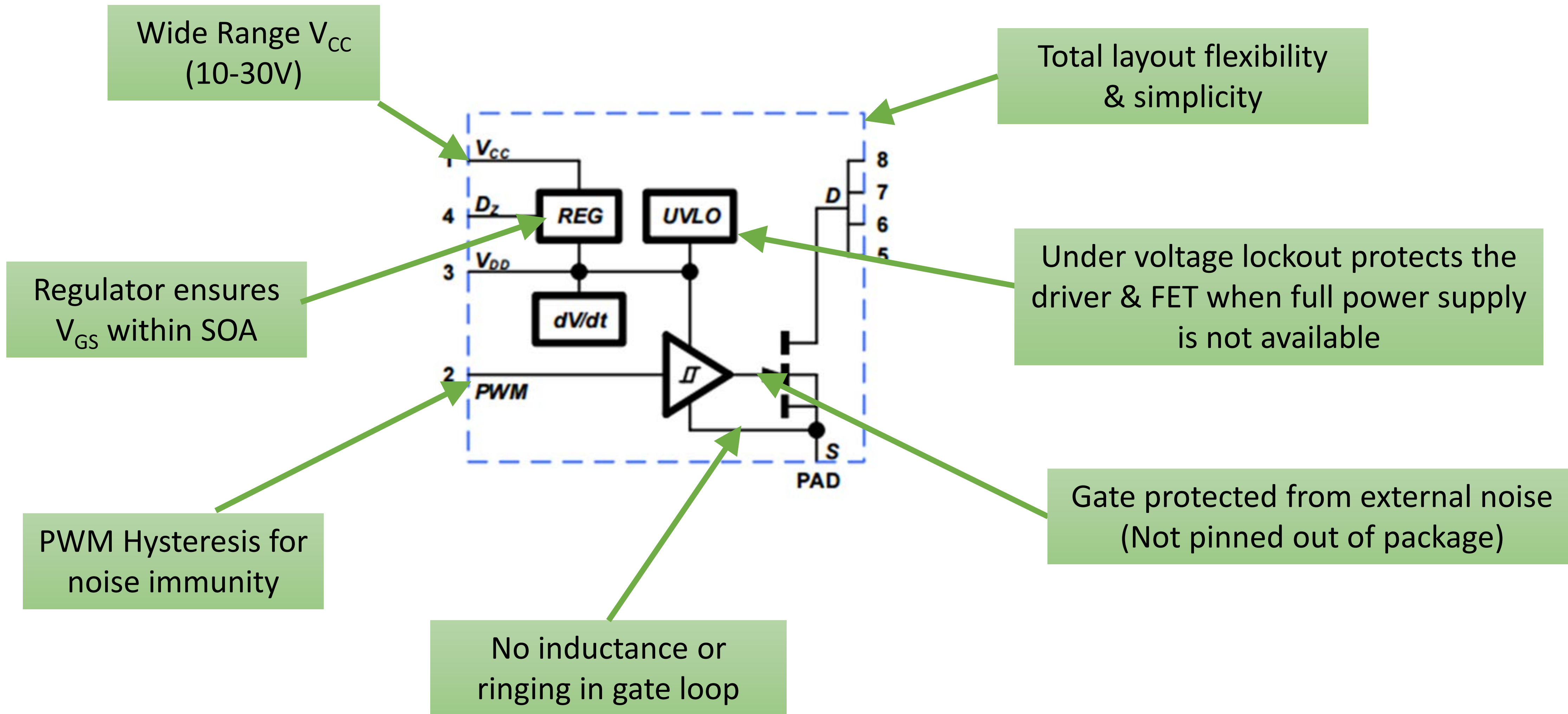
- **Discrete driver**
  - Gate loop inductance creates overshoot (even with good layout)
- **GaNFast™ Power IC**
  - No gate loop parasitic
  - Clean and fast gate signal



Integrated Drive→ *Simple & Robust*



Shoot-Through Protection in Half-Bridge

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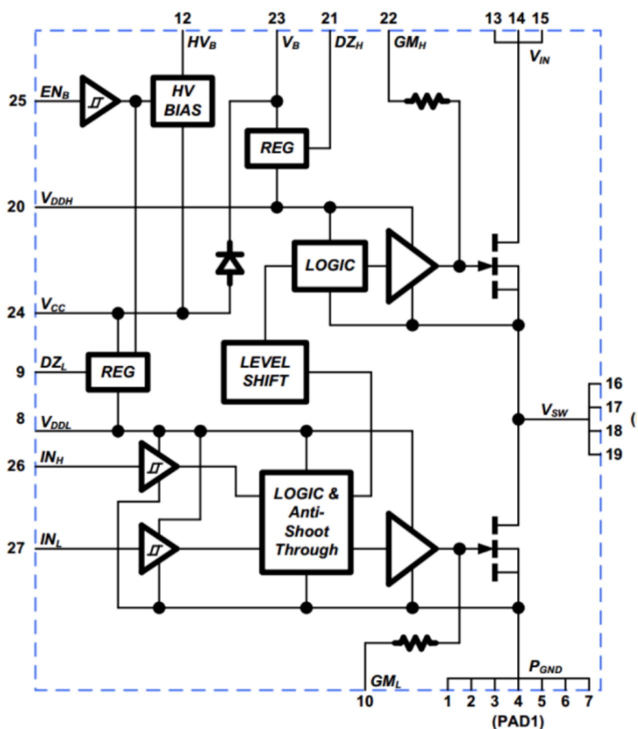
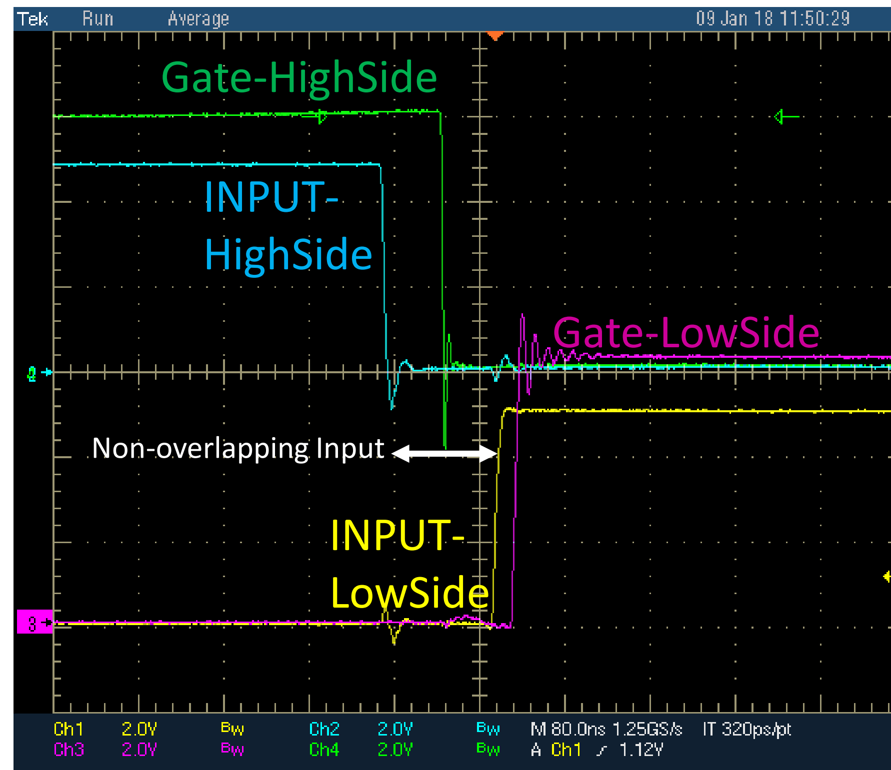
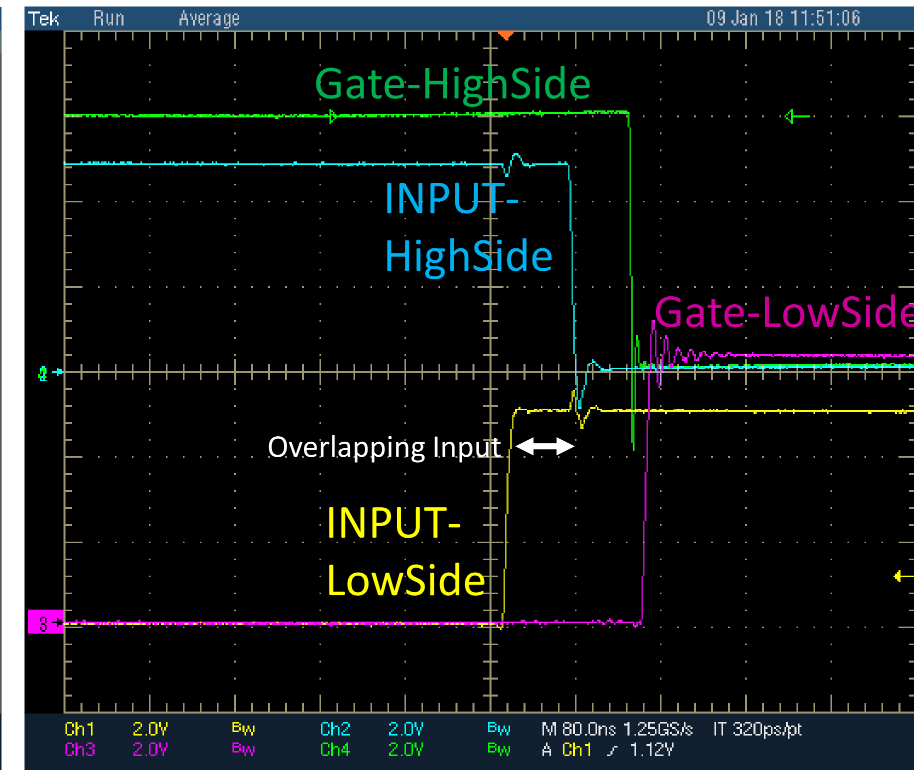
Half-Bridge GaNFast Power IC



Non-Overlapping Logic Input (Typical Operation)



Overlapping Logic Input (Power IC Protection Mode)



High-side and Low-side gates never overlap due to shoot-through protection in power IC

Is Typical Si JEDEC Qual Sufficient?

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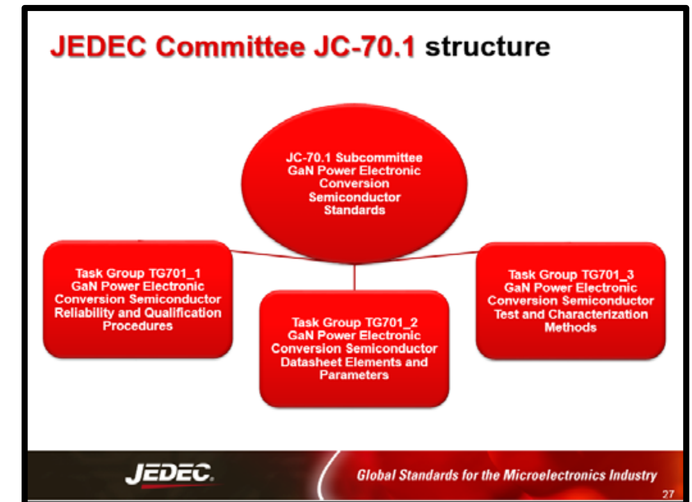
Typical Si-Based Qual Plan

Package Stress

Die Stress

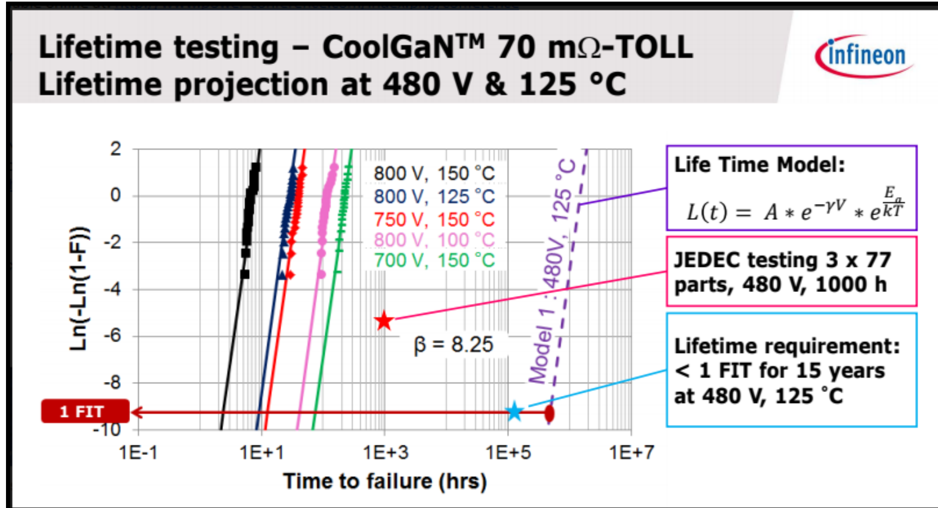
Reference	Test Conditions	Duration	Lots	S.S.
JESD22-A113 J-STD-020	Preconditioning (MSL1): Moisture Preconditioning + 3x reflow: HAST, UHAST, TC & PC	N/A	3	308
JESD22-A104	Temperature Cycle: -55°C / 150°C	1,000cy	3	77
JESD22-A122	Power Cycle: Delta Tj = 100°C	10,000cy	3	77
JESD22-A110	Highly Accelerated Stress Test: 130°C / 85%RH / 100V V_{DS}	96hrs	3	77
JESD22-A108	High Temperature Reverse Bias: 150°C / 520V V_{DS}	1,000hrs	3	77
JESD22-A108	High Temperature Gate Bias: 150°C / 6V V_{GS}	1,000hrs	3	77
JS-001-2014	Human Body Model ESD	N/A	1	3
JS-002-2014	Charged Device Model ESD	N/A	1	3

New GaN Standards Needed

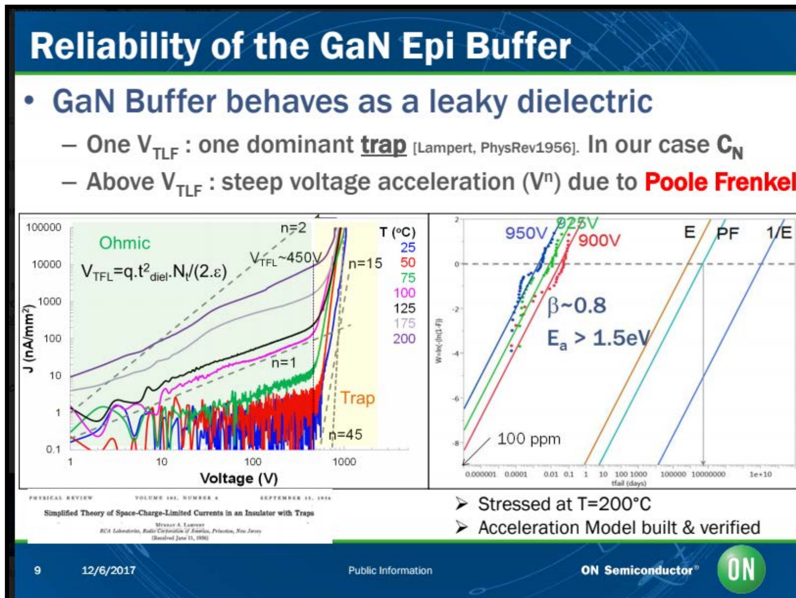


Courtesy: Stephanie Watts Butler (Texas Instruments) and Tim McDonald (Infineon) “From GaNSPEC DWG to JEDEC JC-70.1: An update on industry qualification standards for Gallium Nitride power conversion devices”

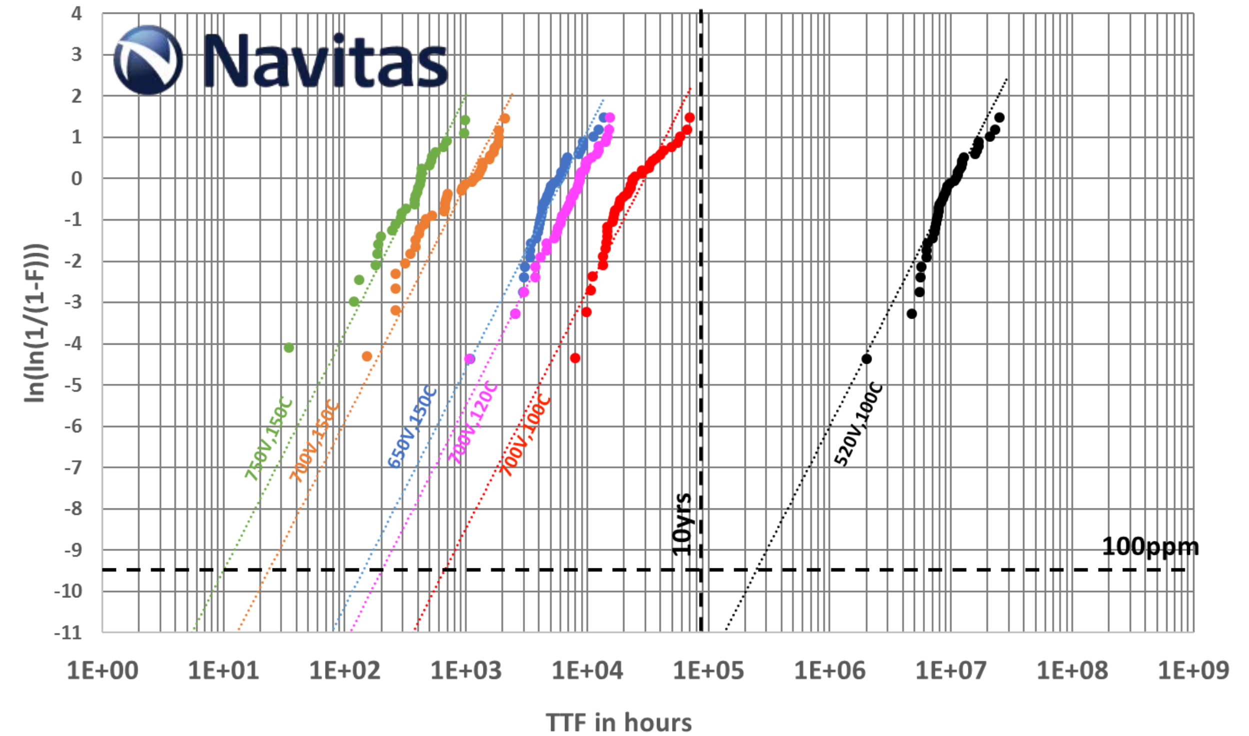
‘Beyond JEDEC’ -- Lifetime based on HTRB?



Bodos Power Electronics Conference 2017, Munich Airport Hilton, December 05, 2017



P. Gassot et al. Bodo Power Conference Munich, Dec. 2017



$$Lifetime = A \times (V^{-\gamma}) \times (e^{\frac{E_A}{kT}})$$

HTRB Lifetime @ 100 ppm is > 20 yrs at application condition

‘Beyond’ JEDEC – Implications for GaN Power ICs?

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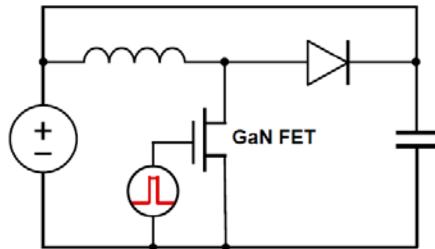
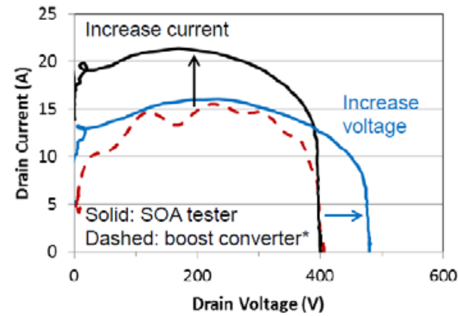
Switching SOA test-vehicle

Boost converter with output tied to input (familiar double-pulse tester)





http://www.ti.com/lit/wp/slyy070/slyy070.pdf

Reliability Lifecycle of GaN Power Devices

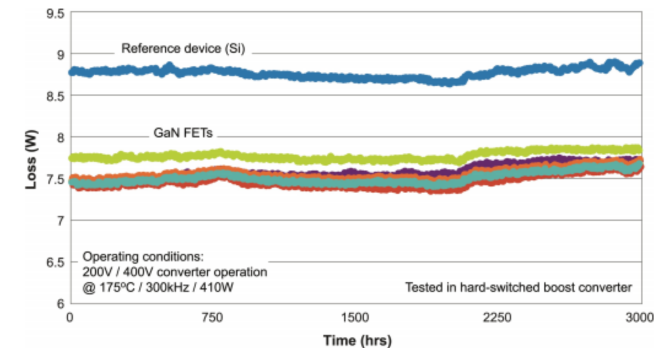
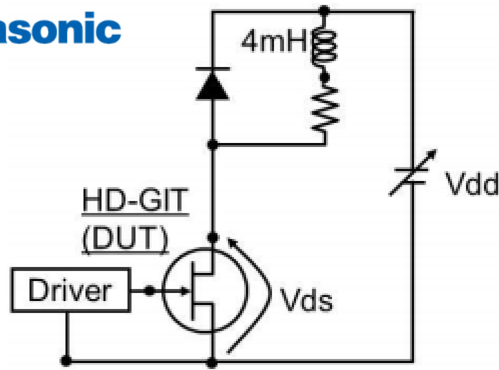
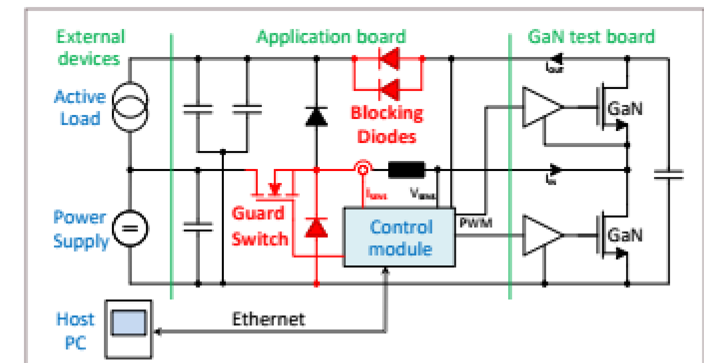


Figure 3. Loss plot for HTOL of seven 600-V-rated GaN-on-Si FETs and a reference device to 3000 hours at Tj=175°C; each device operated in a boost converter at 300kHz with a boost ratio 200V:400V, 410W output power

http://www.transphormusa.com/document/white-paper-reliability-lifecycle-gan-power-devices/



How2PowerToday: September 2015 issue



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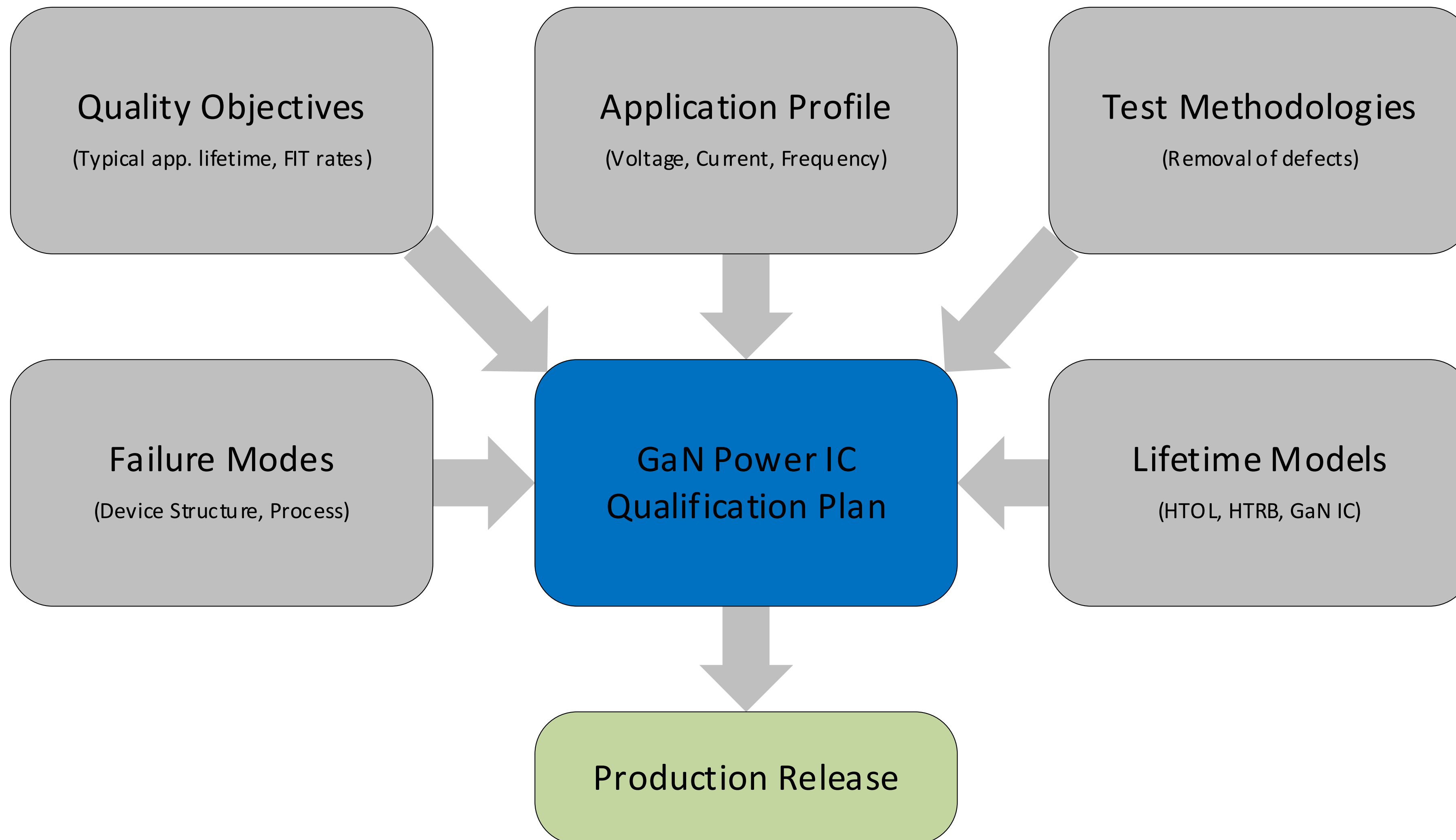
Mission Profile Defines GaNFast Power IC Qualification



Typical Application (Consumer Chargers)

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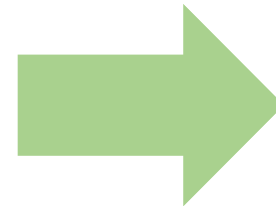
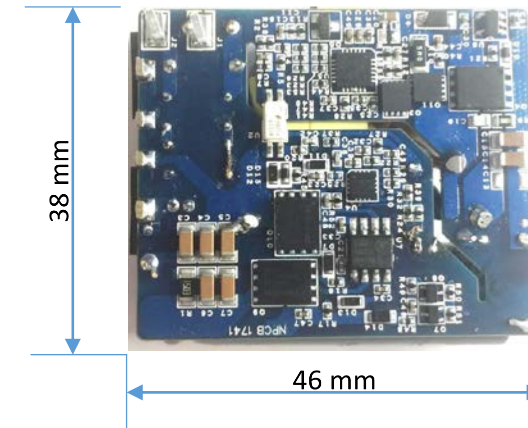
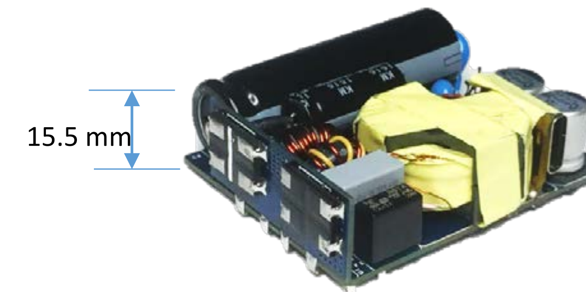
MacBook <100 kHz
<6.5 W/in³, 92%



- **ACF (ZVS) Topology**
- **300 kHz – 1 MHz**
- **120 V – 240 V_{AC}**

Navitas ~300 kHz
24 W/in³ , 94%
= 45 cc cased





Application Profile for ACF Charger

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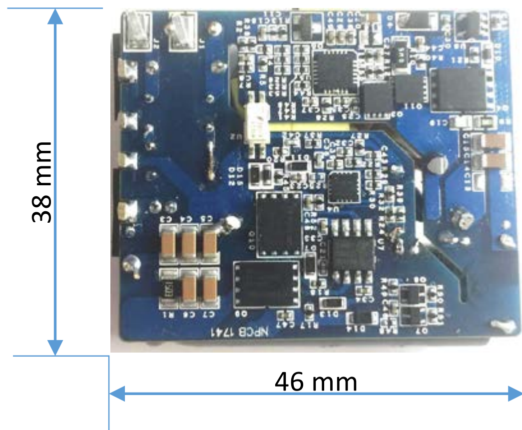
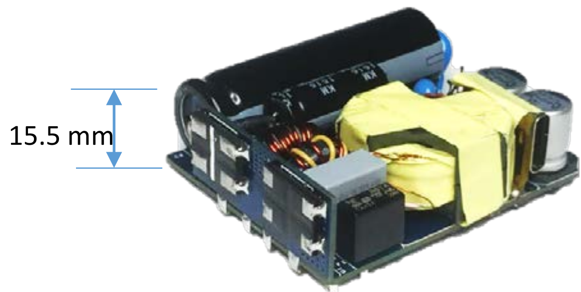
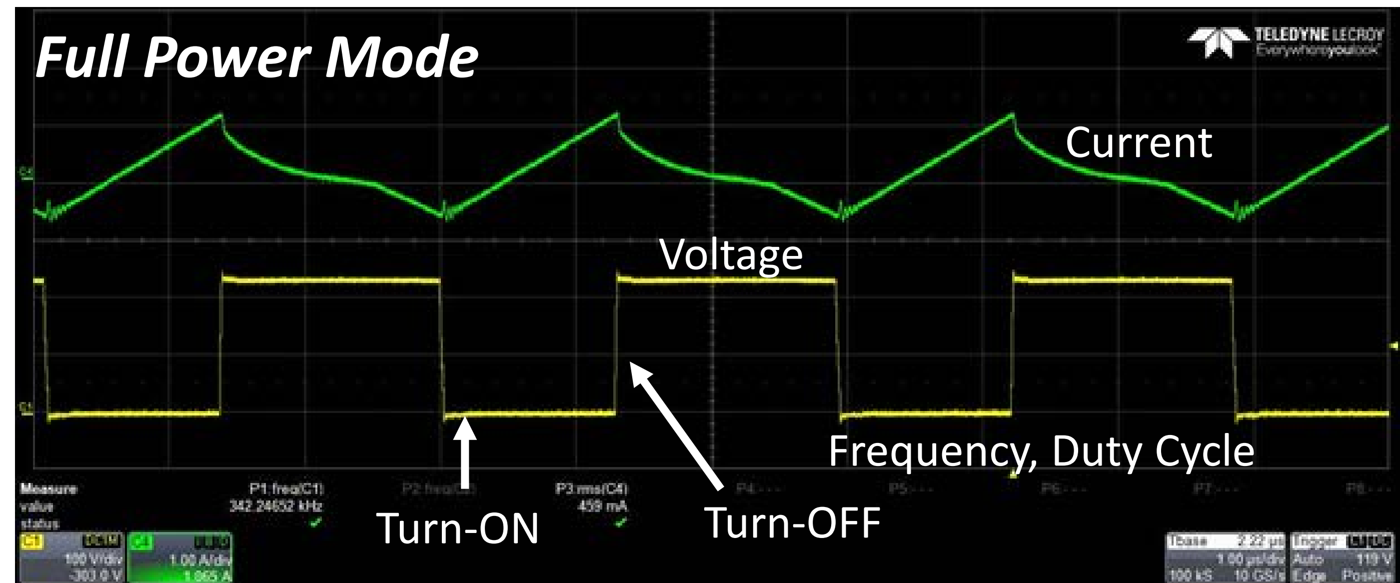
Navitas ~300 kHz
24 W/in³ , 94%
= 45 cc cased







Application Factors

- Voltage (300 – 480 V)
- Current (1-3 A)
- Frequency (100-1,000 kHz)
- Temperature (25 – 100 C)
- Duty Cycle
- Turn-on / Turn-off Profile
- ZVS vs. Hard-Switching

ZVS Application Profile (FET)

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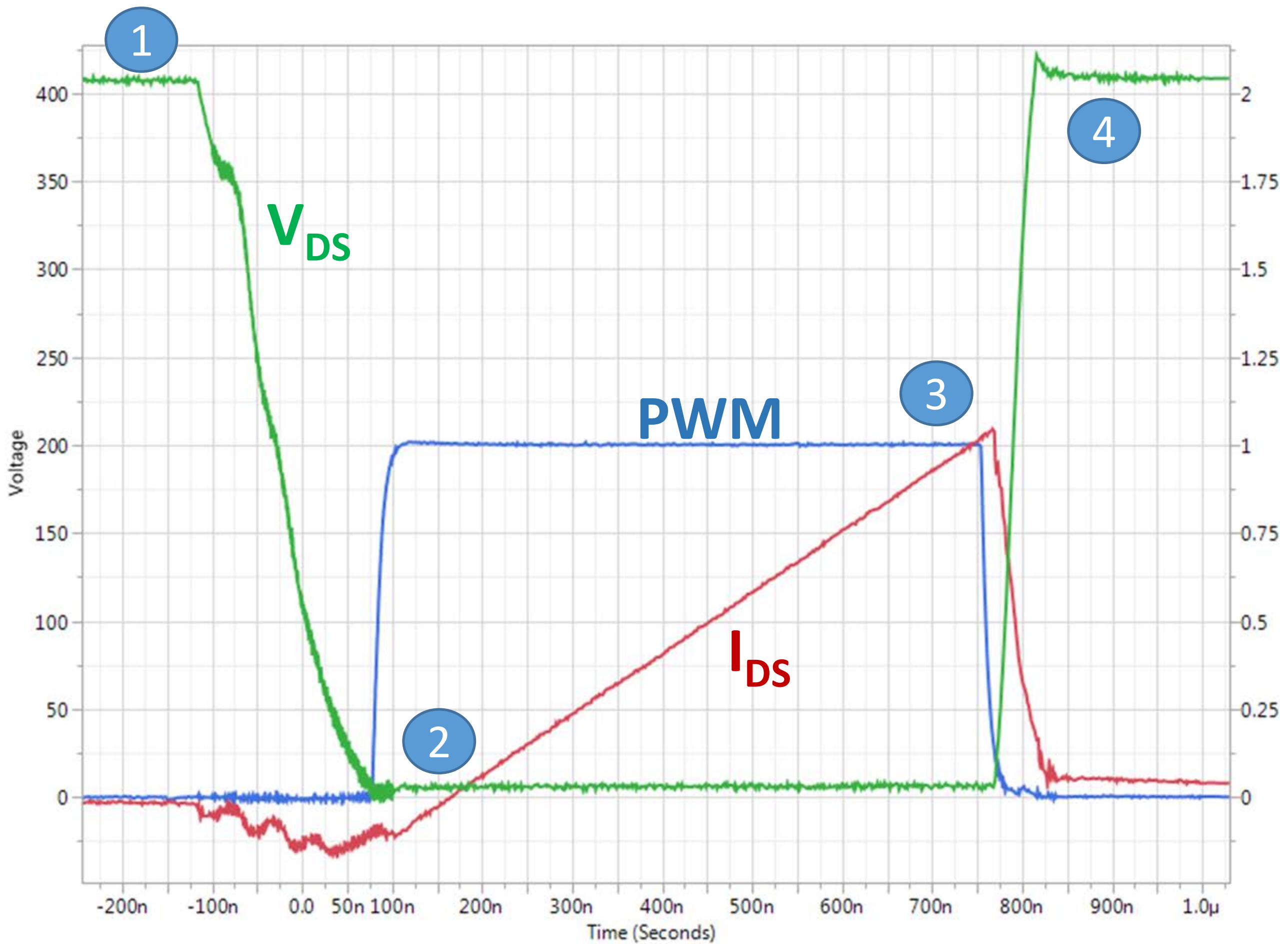


I_{DS} vs. V_{DS} (Load Line)

Hard-Switched Turn-OFF (Lossless charging of C_{OSS})

High-Side Diode Conduction

ON-State

Zero-Voltage Turn-ON

Blocking Mode

1.2, 1, 0.8, 0.6, 0.4, 0.2, 0, -0.2

Ids (Normalized)

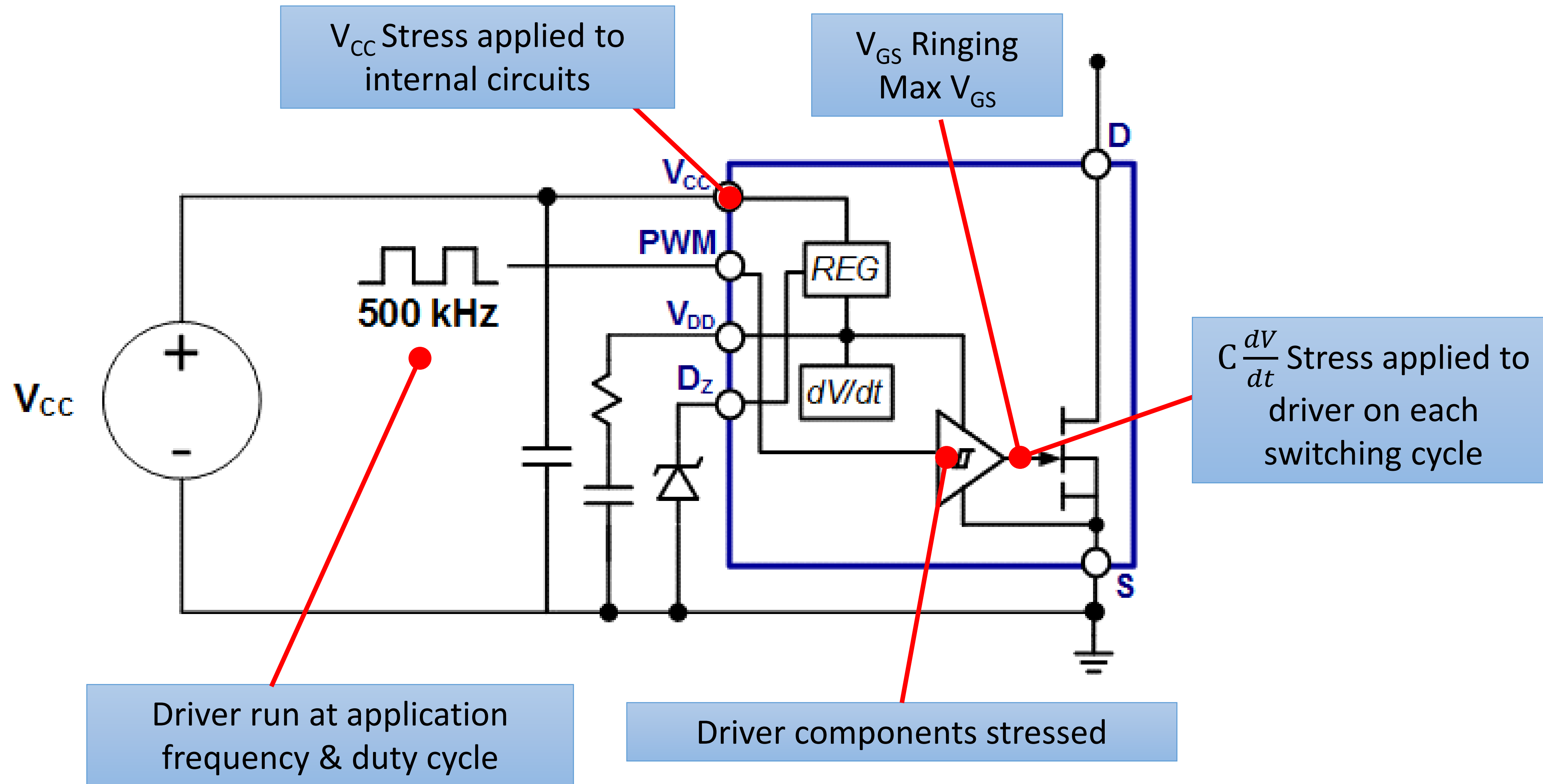
0, 50, 100, 150, 200, 250, 300, 350, 400

Voltage (V)

1, 2, 3, 4

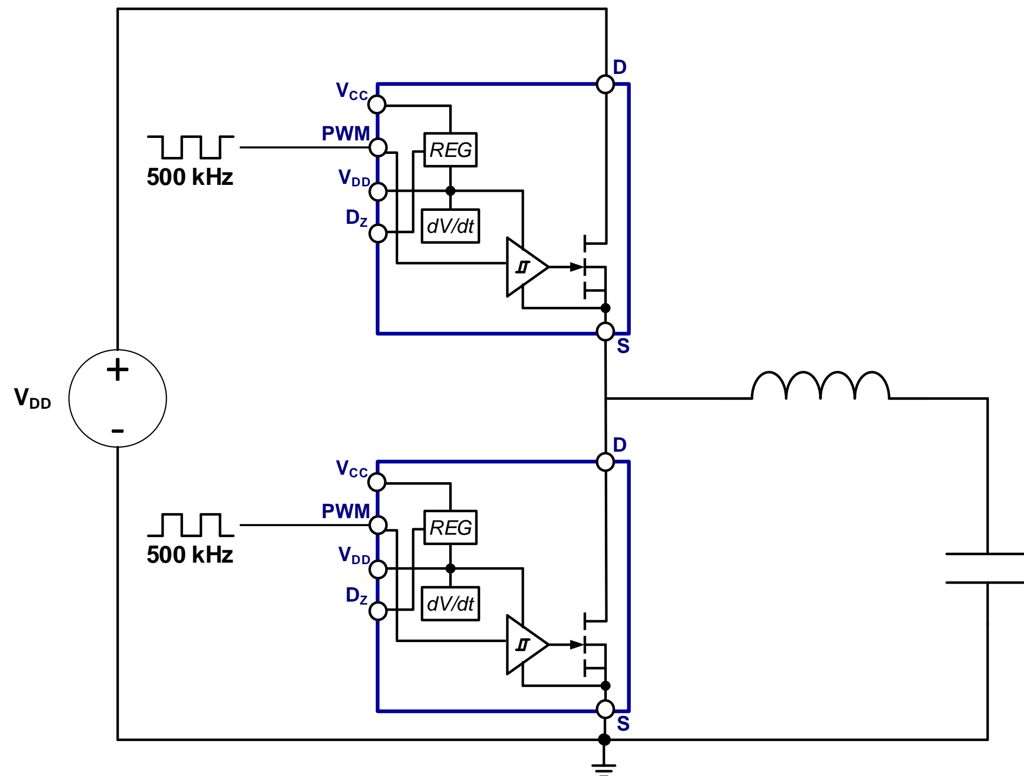
'Soft-Switching' or ZVS (Zero-Voltage Switching) represents an application relevant stress on the power FET

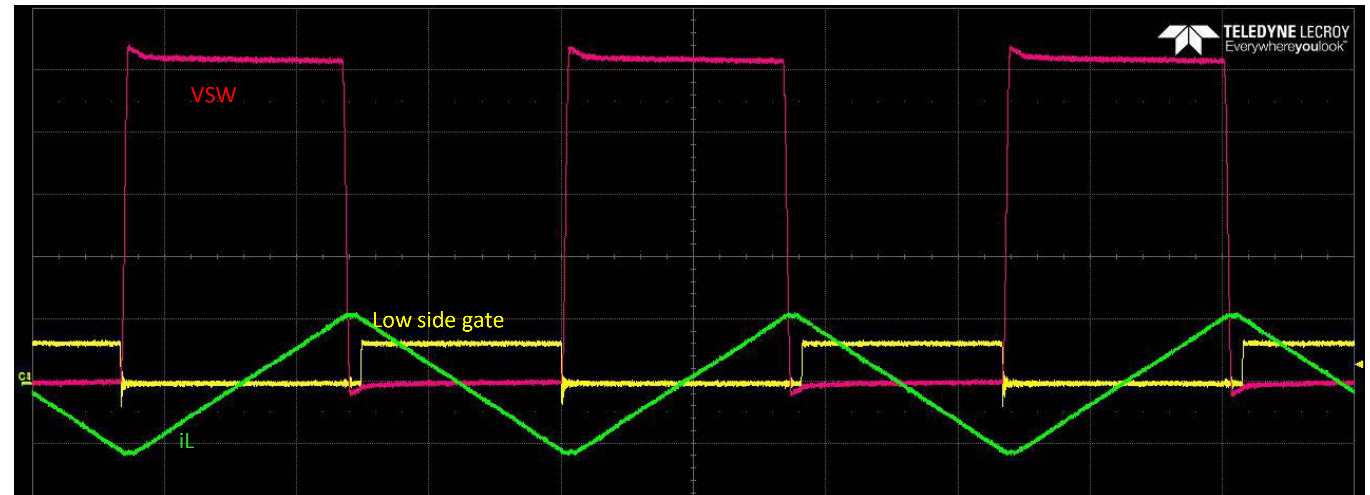
ZVS Application Profile (IC)



ZVS High Temp Op Life (HTOL) Circuit

Navitas





HTOL Circuit Variables

- Voltage
- Current
- Frequency

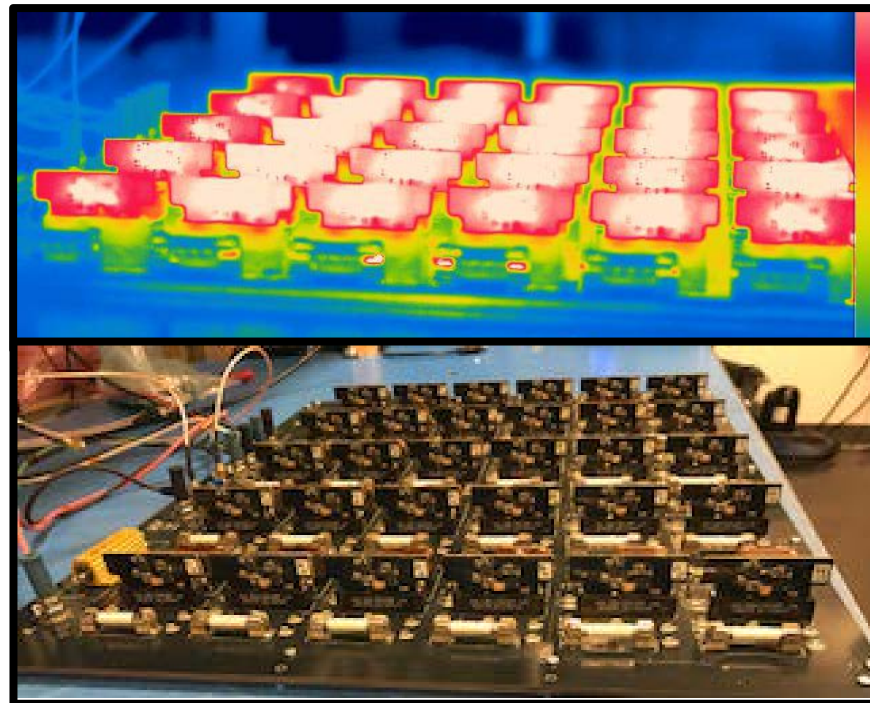
- Temperature
- Duty Cycle

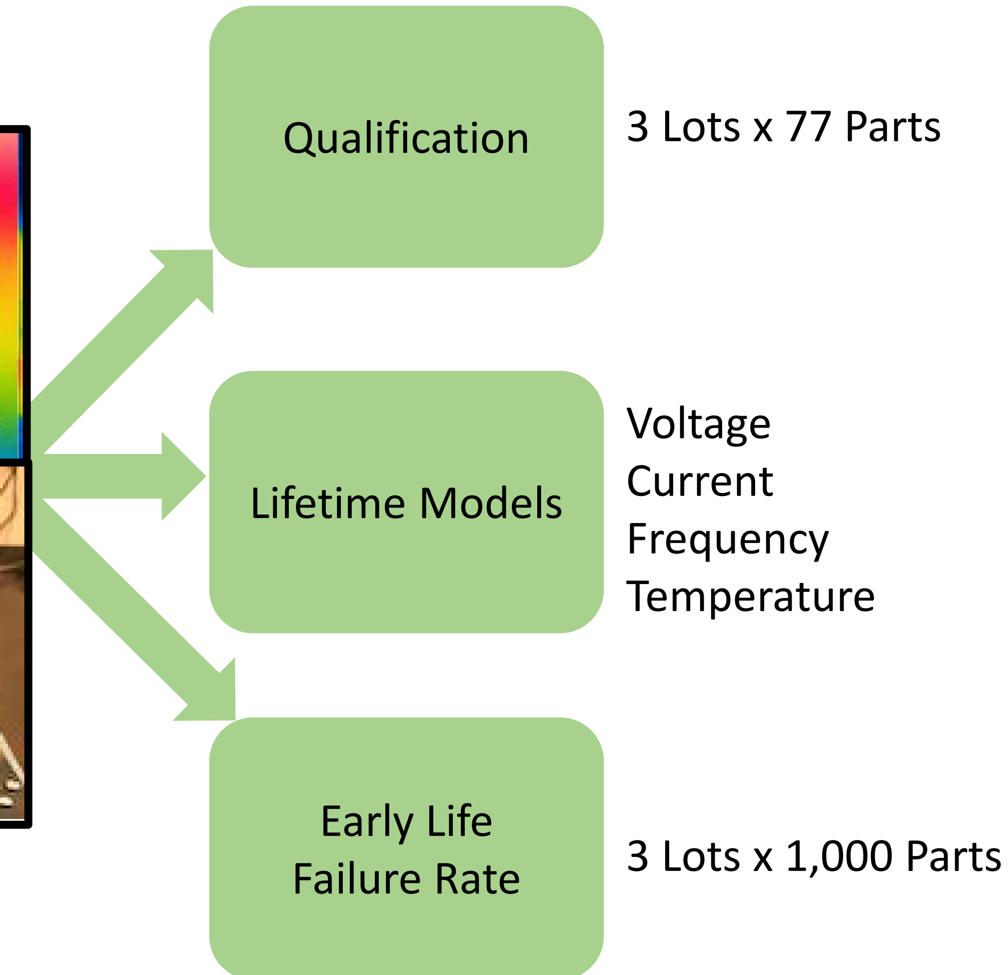
- L-C load applied to half-bridge topology along with complementary inputs & dead time setting to achieve soft-switching
- Power consumption is the only loss elements (DUT, Inductor) since energy is recycled → many cells in parallel
- Circuit allows for same application stress on GaNFast Power IC as customer application (Voltage, Current, Frequency)
- Applies application conditions to the driver & integrated IC so power IC is also qualified in the same test

ZVS HTOL Applied to Statistical Sample Sizes

- Matches all elements of application profile
  - FET & IC
- Many cells in parallel
  - Statistical sample sizes
- Low total power consumption
- Conditions changeable to develop lifetime and acceleration models

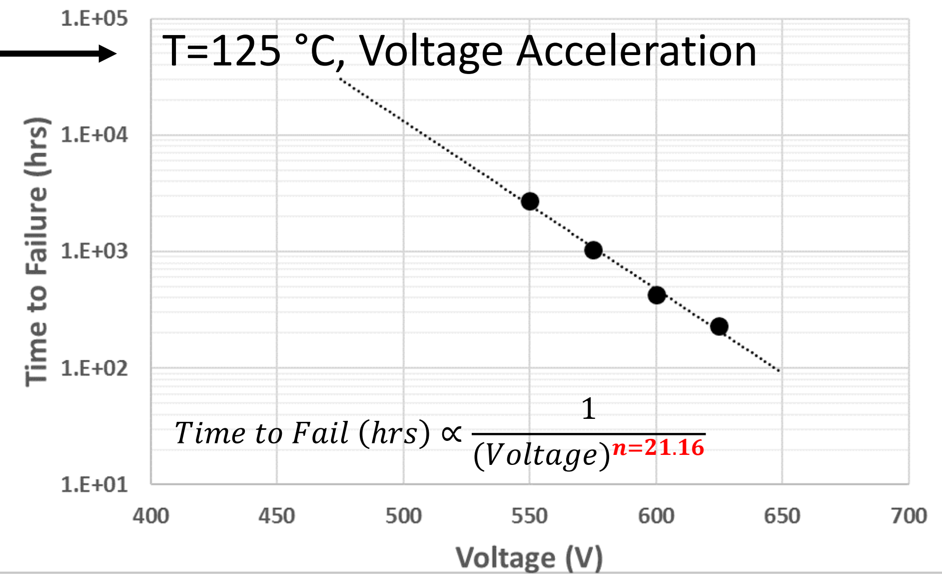
HTOL Mother Board

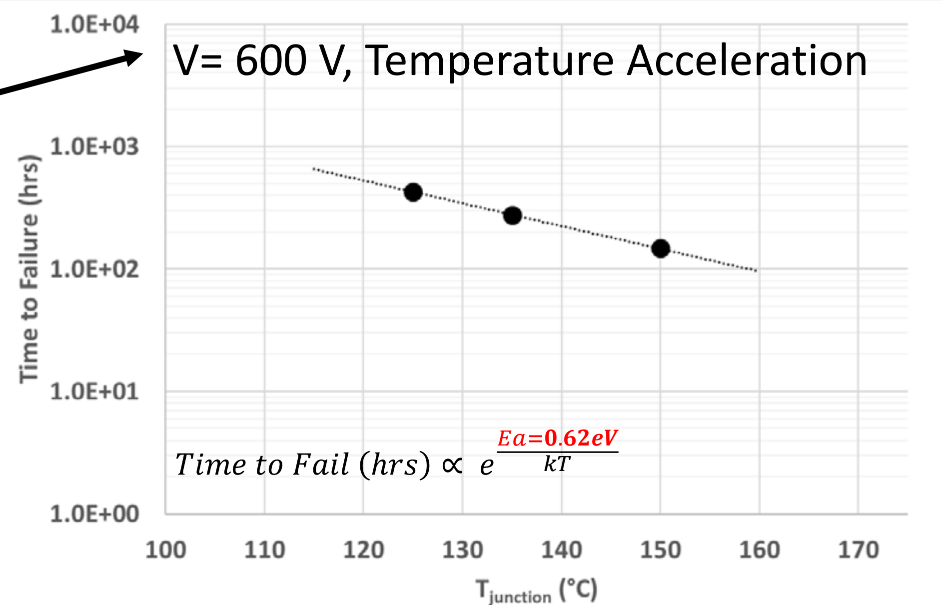




HTOL-based Lifetime Model

Voltage/ Temperature	125	135	150
550	✓		
575	✓		
600	✓	✓	✓
625	✓		





Lifetime Estimation in Charger Application (ACF)

$$Temperature\ Acceleration\ Factor(AF_{temp}) = e^{\frac{E_a}{k}\times(\frac{1}{T_{application}} - \frac{1}{T_{reliability}})}$$

$$E_a = 0.62eV$$

$$Voltage\ Acceleration\ Factor(AF_{voltage}) = (\frac{V_{reliability}}{V_{application}})^n$$

$$n = 21$$

$$Total\ Acceleration\ Factor(AF_{Total}) = AF_{TEMP}\ x\ AF_{VOLTAGE}$$

$$Lifetime\ estimate\ in\ application = AF_{Total}\ x\ Time\ to\ failure\ in\ reliability\ (TTF_{reliability})$$

ACF Charger Full-Power Profile →

AC line Voltage (V)	Rectified AC voltage (V)	Reflected Voltage (V)	Switch Voltage (V)	Full power Temp (°C)
120	170	125	295	85
240	340	125	465	85

$$Lifetime = AF_{Total}\ x\ TTF_{reliability} = \mathbf{81\ years}\ @\ 240V\ AC\ input$$

Predicted lifetime in charger application (ACF) exceeds 10yr lifetime requirement

'Beyond' JEDEC Qual Plan for GaN

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GaN-Based Qual Plan

	Reference	Test Conditions	Duration	Lots	S.S.
Package Stress	JESD22-A113 J-STD-020	Preconditioning (MSL1): Moisture Preconditioning + 3x reflow: HAST, UHAST, TC & PC	N/A	3	308
Package Stress	JESD22-A104	Temperature Cycle: -55°C / 150°C	1,000cy	3	77
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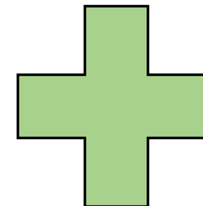
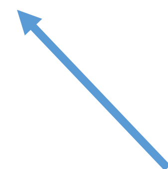
Package Stress / Die Stress	JESD22-A108	High Temperature Gate Bias: 150°C / 6V V_{GS}	1,000hrs	3	77
Die Stress	JESD22-A108	High Temperature Operating Life	1,000hrs	3	77
Die Stress	JS-001-2014	Human Body Model ESD	N/A	1	3
	JS-002-2014	Charged Device Model ESD	N/A	1	3



Lifetime Models (HTOL, HTRB)

Failure Modes Established



Application Specific HTOL Test Bench