2022中国电力电子与能量转换大会
暨中国电源学会第二十五届学术年会及展览会
2022 China Power Electronics and Energy Conversion Congress
& The 25th China Power Supply Society Conference and Exhibition

"GaNFast™ and GeneSiC™: Twin Engines Drive the Future of High-Power Applications"

Navitas
Energy • Efficiency • Sustainability

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Navitas GaNFast™ Power IC
Navitas GeneSiC Power

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Twin Engines

Navitas

31 Ga Gallium
7 N Nitrogen
+
14 Si Silicon
6 C Carbon

GaNFast™

GeneSiC SEMICONDUCTOR

Pure-Play, Next-Generation Power Semiconductors

Contents

- Characteristics of WBG (GaN & SiC) Devices
- Package-dependent thermal design comparisons
- Summary

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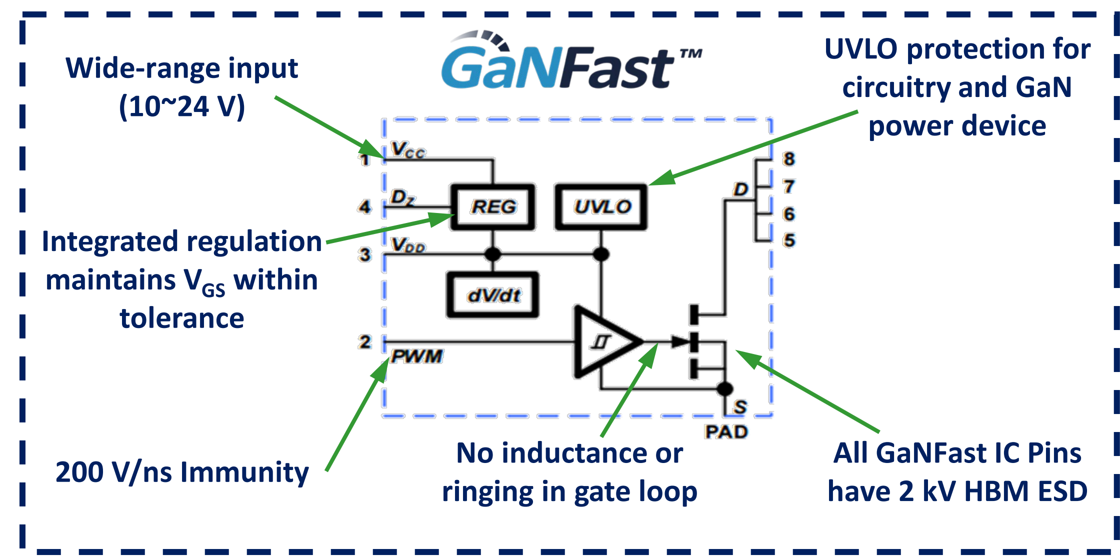
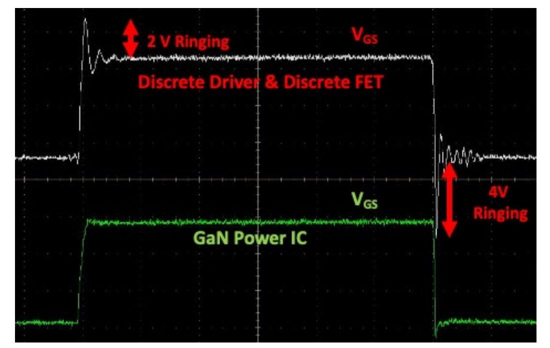
GaNFast Delivers Value, Reliability, Low Cost

- **Company founded in 2014**
  - NASDAQ IPO Oct 2021 (NVTS)
  - #1 worldwide GaN supplier
- **650 V_{DS} (800 V_{PK}) lateral GaN-on-Si process**
  - EMode (normally OFF) GaN power device
  - Zero Q_{RR} and E_{ON}/E_{OFF} much lower than Si or SiC
- **Advanced monolithic integration capability**
  - Regulated gate drive minimizes inductance & ringing
  - Logic and Protection functions fully-integrated
  - Enhanced Reliability not feasible in GaN discretes



Discrete GaN is Unprotected GaN



Excessive voltage stress degrades reliability and risks failure

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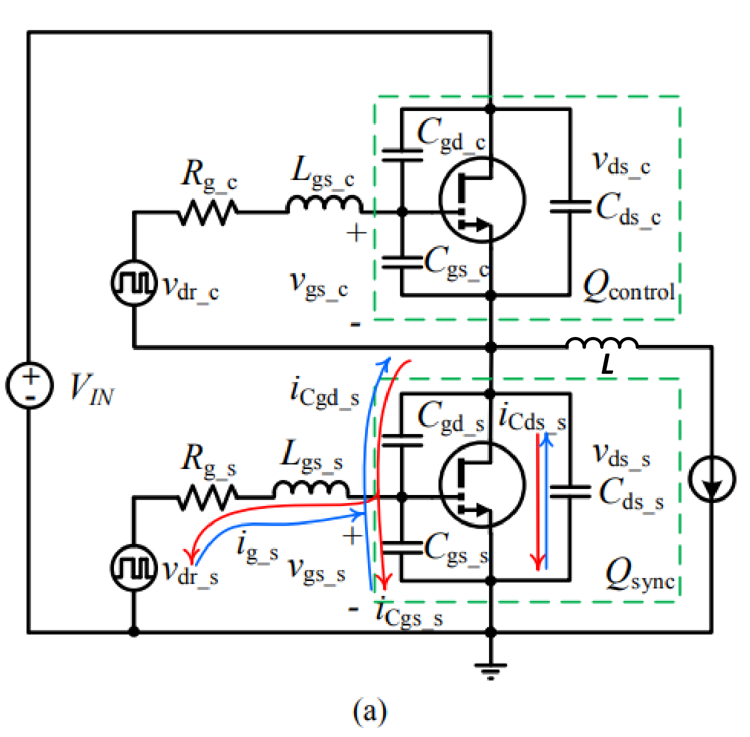
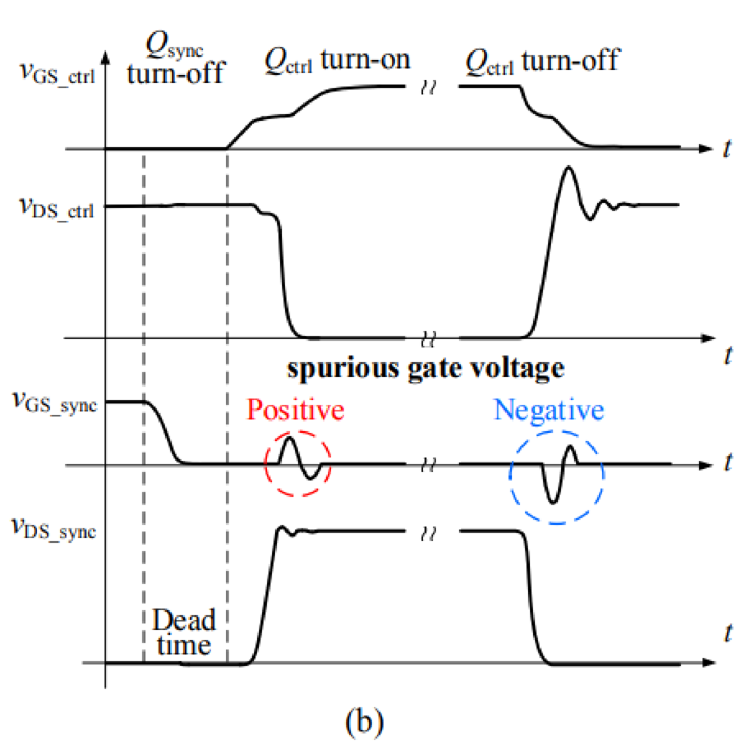
Crosstalk issue caused by fast switching

- Typical half-bridge circuit and crosstalk waveforms



Half bridge circuit



Typical waveforms

- **Root cause:**
  - Fast switching and high dV/dt
  - Low Vth voltage of V_{GS}
  - Long drive loop brings the increase of parasitic parameters
  - Weak CMIT performance of the driver ICs

Ref: Wang J , Liu D , Dymond H , et al. Crosstalk suppression in a 650-V GaN FET bridgeleg converter using 6.7-GHz active gate driver[C]// 2017 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 2017.

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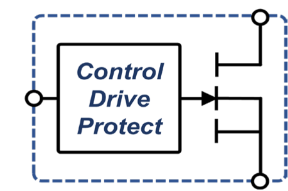
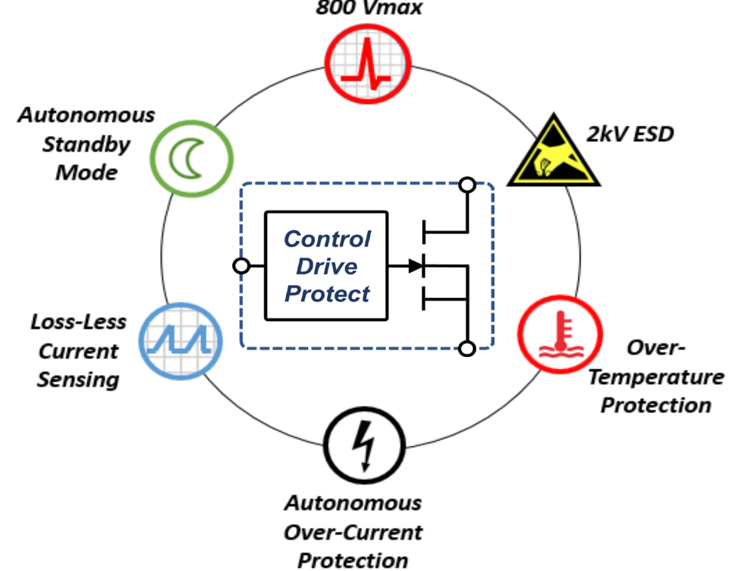
Benefits of Integration

- Component reliability, and ***system*** reliability

Silicon FET

Unprotected GaN





- Old, slow
- High Q_g
- High C_{OSS}
- F_{SW} < 100 kHz

- Exposed gate
- External gate drive
- dV/dt sensitivity
- Layout sensitivity
- ESD sensitivity
- Unknown reliability
- Unknown robustness

✓ Internal Gate
✓ Integrated Gate Drive
✓ dV/dt Immunity
✓ Layout Insensitive
✓ 2 kV ESD rating
✓ Proven Reliability
✓ Proven Robustness

GaNFast plus:

✓ Autonomous Standby
✓ Autonomous Protection
✓ Loss-less Current Sensing
✓ High Precision
✓ High Efficiency

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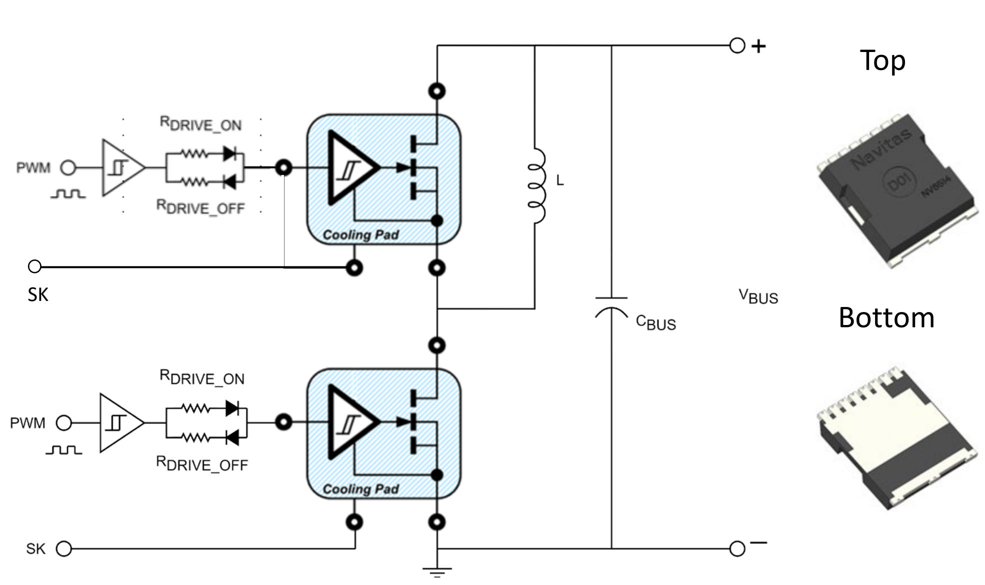
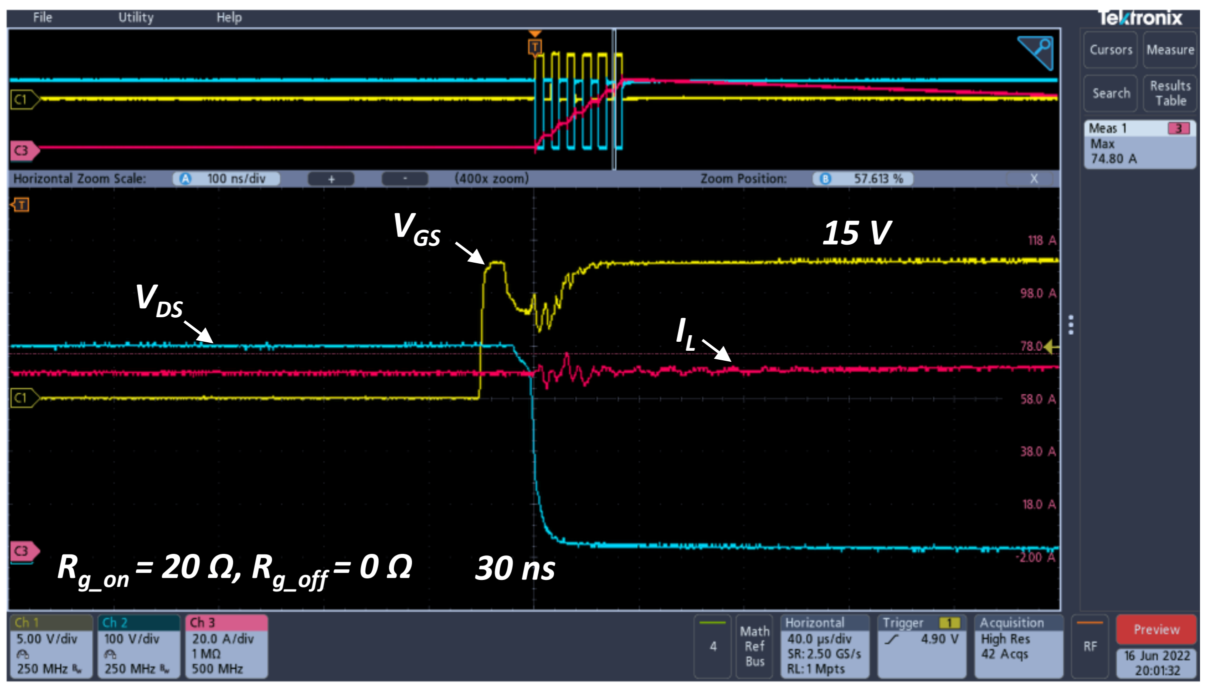
GaNFast TOLL Device Characteristics

- **Features:**
  - TOLL (transistor outline, lead-less), 18 mΩ typical $R_{DS(ON)}$ @25°C
  - 12~18 V for DRIVE to SK
  - Integrated 5 V power supply unit. A typical 15 V drive voltage needs 30 ns for stability
  - Integrated level-shift and deglitch circuit for improved anti-interference performance



Double pulse test Circuit



Typical drive waveform

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GeneSiC™

Patented Trench-Assisted Planar Gate SiC MOSFETs

Up to 6.5 kV

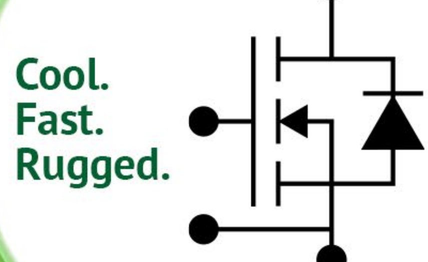
Largest range of SiC FETs & diodes
(650 V to 6.5 kV)

Fast Switching

Highest efficiency hard-switch, soft-switch
(Lowest E_{ON}, E_{OFF}, E_{ZVS} losses)

Cool Operation

Lowest $R_{DS(ON)}$ at high temperature
(25% lower than industry typical)



Cool.
Fast.
Rugged.

100%-Tested Robust Avalanche

Highest published capability to handle excess energy in fault condition

Long Short-Circuit Withstand Time

World-class survival duration in fault condition

High-Power Paralleling

Matching currents
(Stable V_{TH})

Based on Navitas testing of 1200V SiC MOSFETs vs. competitor products

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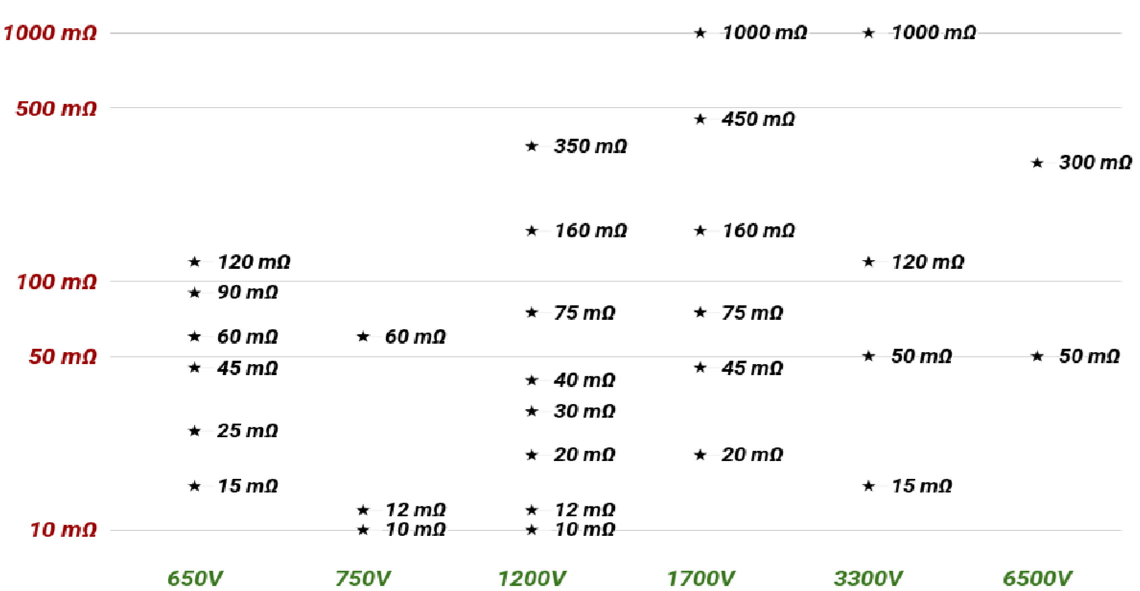
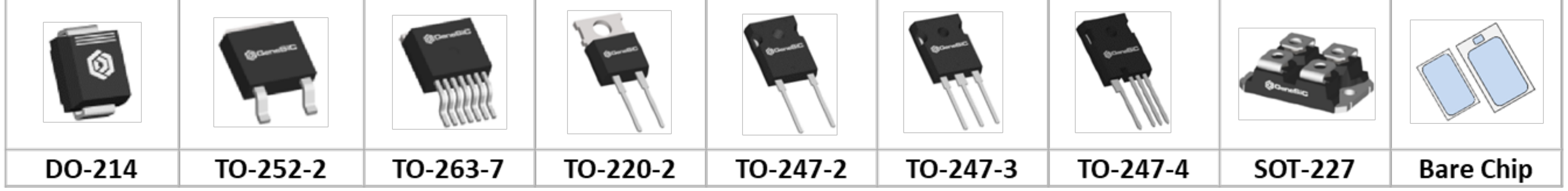
Broadest SiC FET Portfolio[1]

GeneSiC™ 650–6,500V Trench-Assisted Planar SiC FETs



- 50+ SiC MOSFETs, array of standard packages
- Only supplier with 650V to 6,500V SiC MOSFETs

- Broadest industry offering for 1700V SiC MOSFETs



1) based on GeneSiC voltage range of production released SiC MOSFETs compared to all publicly identified voltage ranges of other SiC suppliers.

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Best High-Speed, High-Temp Performance

Supplier	Resistance		Energy Loss				Figure-of-Merit (Low number is better)	
	$R_{DS(ON)}$ @ 25°C (mΩ)	$R_{DS(ON)}$ @ 175°C (mΩ)	E_{ON} @ 25A (μJ)	E_{OFF} @ 35A (μJ)	E_{OSS} @ 800V (μJ)	E_{ZVS} E_{OFF}-E_{OSS} (μJ)	**Hard-Switching** R_{DS} @ 175°C x (E_{ON}+E_{OFF}) (Ω-μJ)	**Soft-Switching** R_{DS} @ 175°C x E_{ZVS} (Ω-μJ)
GeneSiC	40	57	600	80	34	46	**38.8**	**2.6**
#2	40	68	600	80	40	40	46.2	2.7
#3	40	80	850	390	35	355	99.2	28.4
#4	40	71	550	150	35	115	49.7	8.2
#5	45	85	520	65	29	36	49.7	3.1

Lowest power loss at high temp, high speed

Highest Efficiency, Energy Savings Small Size, Light Weight, Low System Costs!

Reference 1,200V SiC FET, 40-45mΩ devices; GeneSiC = Trench-Assisted Planar G3R40MT12J; based on Navitas test result & competitive data sheet parameters.

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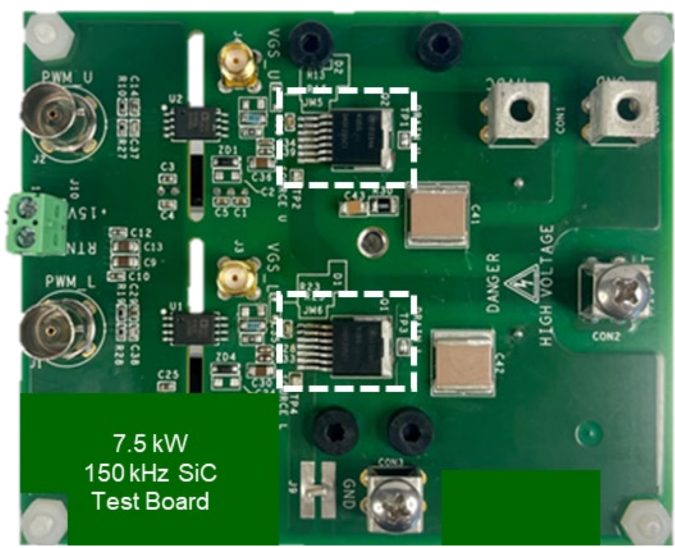
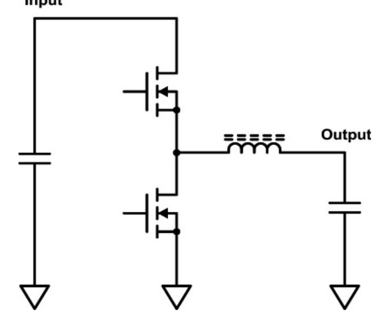
Faster, Cooler, Longer Lifetime

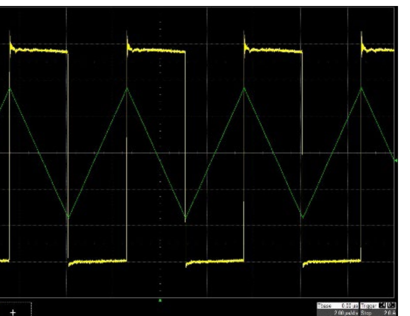


Test Board

- GeneSiC trench-assisted planar FET vs. Competitor SiC FET
  - 1,200 V, 40 mΩ, D2pak in half-bridge
  - Represents 7.5 kW DC-DC converter (e.g. data center, EV)
  - 150 kHz switching = ~10x faster than Si IGBT example
- GeneSiC: **>80% energy savings (>3,000 kWh/yr) *vs Si IGBTs***
  -25°C cooler = 3x longer life *vs other SiC*
  (reduced maintenance / repair costs)



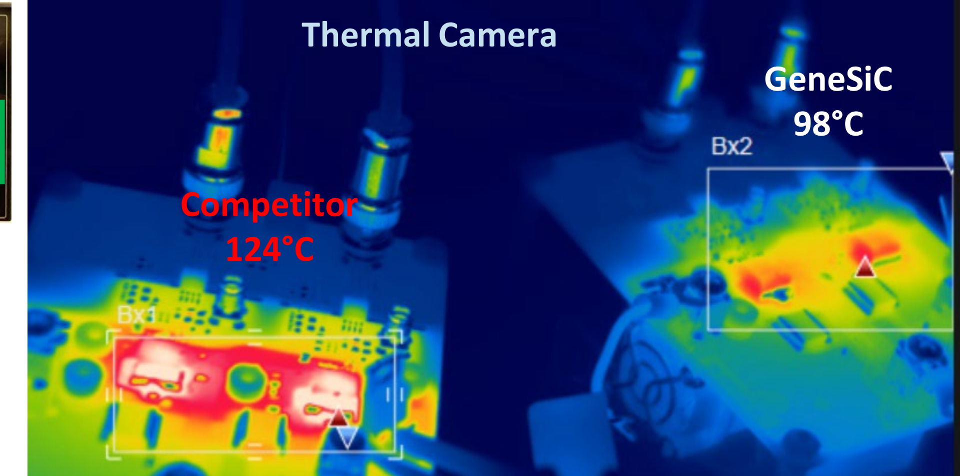
Test Circuit
(1-phase of 3-phase motor drive)



Switching Waveforms
(40 A pk-pk, 20 A turn-off}

Competitor SiC
45 W system loss

GeneSiC
40 W *system* loss
-30% *SiC* loss



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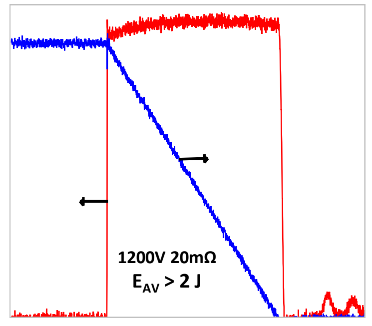
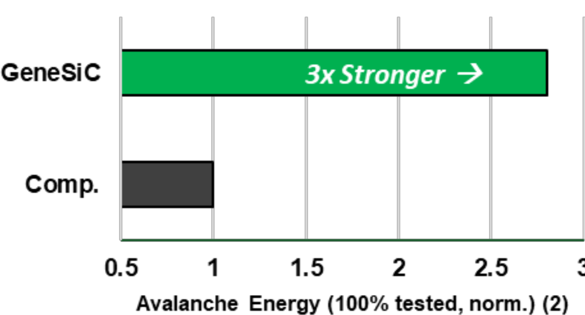
High Quality, High Reliability

100%-Tested Avalanche

Highest published capability to handle excess energy in fault condition

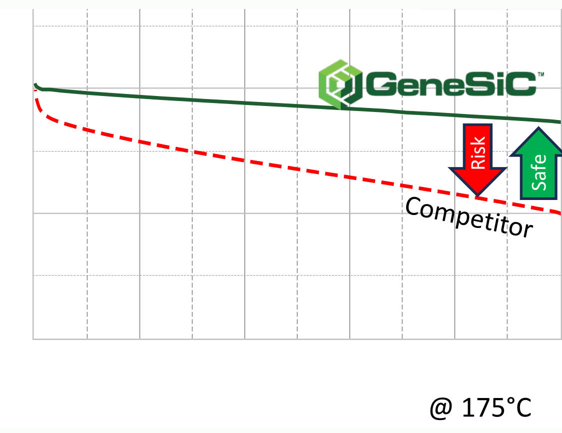


Critical in applications like motor drives to withstand unclamped inductive load (UIL) energy dump in situations like motor open-circuit (O.C.)



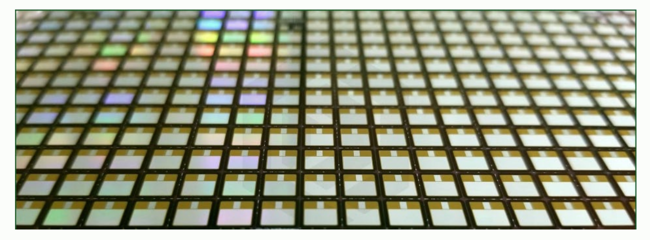
High Power Paralleling

Matching currents (Stable V_{TH})



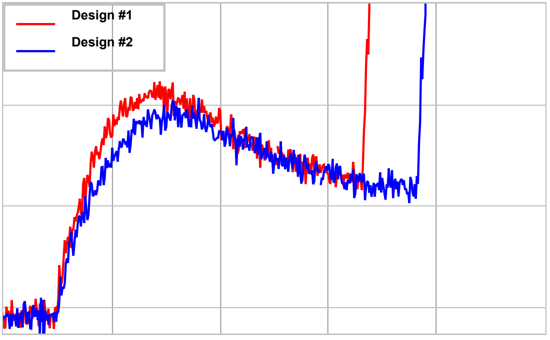
Competitor products allow threshold voltage to drop under high voltage, creating risk of turn-on error

GeneSiC packaged and bare-die FETs can be paralleled reliably for high-power applications

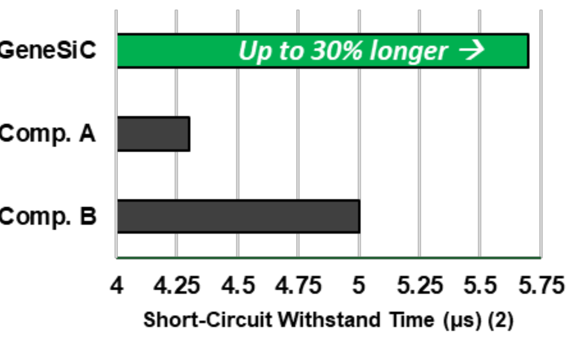


Long Short-Circuit Withstand Time

World-class survival duration in fault condition



Critical to prevent failures like motor short circuit where the FET faces full voltage (V_{DD}) in ON-state.



Zero reported GeneSiC-related field failures!

1) *As of September '23, per GeneSiC records*
2) *1,200 V, 20 mΩ FET*

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Challenges for the packaging and thermal design

TOLL

TO-247

Top Side

X2

55 mm^2

112 mm^2

Bottom Side

TO-247-4P

TOLL

D

D S SS G

G SS S

Bonding wire solution

source

through via

stop layer

HEMT die

heatsink

thermal vias

EETOP

GaN Systems GS61008P vertical cross-section （source： EETOP）

铜夹片技术

Nexperia CCPAK vertical cross-section

Increase the area of copper substrate as much as possible to enhance heat dissipation!

- With GaN/SiC die shrink, the package is also reduced, which saves footprint but brings challenges of the heat dissipation
- The design of system heat dissipation becomes very important in practical applications

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Full-bridge Eval Board and Test Platform

Full-bridge circuit

Drive circuit

- DEMO board Top view
- DEMO board Bottom view

AL

Coolant channel

TOLL packaging device

DBC or TIM

Finger

- Side view
- Top view

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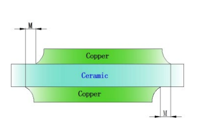
Review: Heat Dissipation TIMS



	Bonded Copper (BC)		GAP-FILLER	Thermal pad		Sil-pad
	AL_2O_3	ALN	CR350	Tgard-K52-2	Tpcm7000	Tgard-K5000
Specification	0.63 mm, 96% AL_2O_3 +0.3 mm, 99.99%, Cu	0.63 mm, ALN + 0.3 mm, 99.99%, Cu	Thermal glue (0.8 mm)	Phase change material (0.076 mm)	Phase-change material (0.13)	0.127 mm
Thermal conductivity (W/m.k) or Resistance	>24	>170	3.6	0.13~0.30°C-in^2/W @20 psi clip pressure	7.5	0.40°C-in^2/W @ 50 psi clip pressure
Dielectric strength-AC (KV/mm)	>20	>20	>9	>7.8	0	>4.5
Coefficient of Thermal Expansion (x10-6/K)	6.8 （20℃~300℃）	4.7 (20℃~300℃)	N/P	N/P	N/P	N/P
Cost Contains Two devices (¥)	2.5	12	1.41	1.7	3	0.81

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Review: TOLL Thermal Designs

- Toll devices
- Solder
- Copper inlay
- Solder
- Copper of DBC
- Ceramic
- Copper of DBC
- TIM
- Cold plate

Case 1

0.05mm
1.6mm
0.05mm
0.3mm
0.635mm
0.3mm
0.12mm
3mm

R_jc
R_solder1
R_cop1
R_ solder2
R_cop2
R_ceramic
R_cop3
R_TIM
R_AL

Case 2

0.05mm
1.6mm
• TIM 0.12mm
0.3mm
0.635mm
0.3mm
0.12mm
3mm

R_jc
R_solder
R_cop1
R_TIM1
R_cop2
R_ceramic
R_cop3
R_TIM2
R_AL

Case 3

• TIM 0.8mm
3mm

R_jc
R_solder
R_cop.
R_TIM
R_AL

Case 4

• SIL Pad 0.203mm
3mm

R_jc
R_solder
R_cop.
R_SIL pad
R_AL

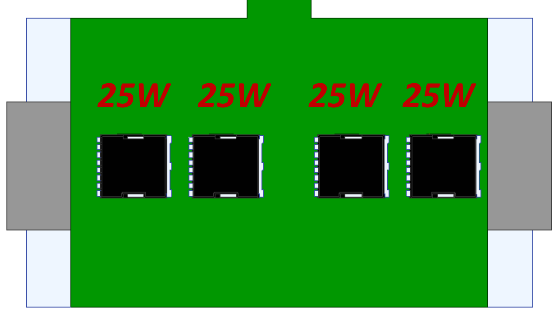
Case 5

Dielectric layer

R_jc
R_solder
R_cop.
R_Die.
R_AL

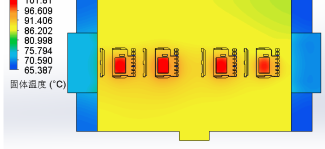
- 5 practical application conditions for analysis.

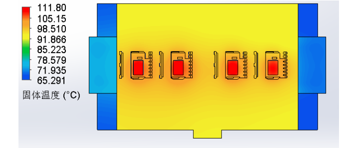
TOLL Simulation Results

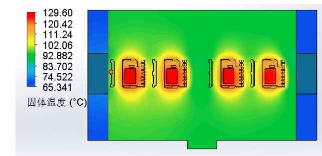


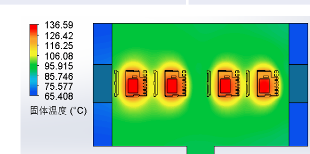
- 25 W Loss pre devices
- 65°C coolant water
- 85°C ambient temperature
- T_j design target is 125°C

Case 1		Case 2		Case 3		Case 4	
Layers	T (°C)	Layers	T (°C)	Layers	T (°C)	Layers	T (°C)
Die	102.09	Die	112.07	Die	129.95	Die	136.71
Die attach	100.59	Die attach	110.5	Die attach	128.26	Die attach	135
Exposed Pad	100.16	Exposed Pad	110.06	Exposed Pad	127.82	Exposed Pad	134.57
Solder	97.907	Solder	107.81	Solder	125.6	Solder	132.38
Copper Inlay	96.976	Copper Inlay	106.88	Copper Inlay	124.7	Copper Inlay	131.5
Solder	93.906	TIM	103.81				
DBC Cu Top Layer	93.586	DBC Cu Top Layer	92.555				
DBC Al_2O_3 Layer	93.34	DBC Al_2O_3 Layer	92.301	0.8 mm TIM	122.05	0.203 mm SIL PAD	116.31
DBC Cu Bot. Layer	86.594	DBC Cu Bot. Layer	85.601				
0.12 mm TIM	86.43	0.12 mm TIM	85.442				
Cold Plate	81.563	Cold Plate	80.662	Cold Plate	82.302	Cold Plate	81.899
Coolant	65	Coolant	65	Coolant	65	Coolant	65









- Case 1 is the best thermal solution for the Toll packaging.

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TOLL System Thermal Resistance

- Thermal resistance : $R_{th} = \Delta T/\Delta P$

Case 1		Case 2		Case 3		Case 4	
Layers	Rth (°C/W)	Layers	Rth (°C/W)	Layers	Rth (°C/W)	Layers	Rth (°C/W)
R_Die	0.06	R_Die	0.0628	R_Die	0.0676	R_Die	0.0684
R_Die attach	0.0172	R_Die attach	0.0176	R_Die attach	0.0176	R_Die attach	0.0172
R_Exposed Pad	0.09012	R_Exposed Pad	0.09	R_Exposed Pad	0.0888	R_Exposed Pad	0.0876
R_jc	0.16732 R_jc	***R_jc***	0.1704 R_jc	***R_jc***	0.174 R_jc	***R_jc***	0.1732 R_jc
R_Solder	0.03724 R_solder1	R_Solder	0.0372 R_solder	R_Solder	0.036 R_solder	R_Solder	0.0352 R_solder
R_Copper Inlay	0.1228 R_cop1	R_Copper Inlay	0.1228 R_cop1	R_Copper Inlay	0.106 R_cop.	R_Copper Inlay	0.120 R_cop.
R_Solder	0.0128 R_ solder2	R_TIM	0.4502 R_TIM1				
R_DBC Cu Top Layer	0.00984 R_cop2	R_DBC Cu Top Layer	0.01016 R_cop2				
R_DBC Al_2O_3 Layer	0.26984 R_ceramics	R_DBC Al_2O_3 Layer	0.268 R_ceramic	R_0.8 mm TIM	1.58992 R_TIM	R_0.203 mm SIL PAD	1.864 R_SIL pad
R_DBC Cu Bot. Layer	0.00656 R_cop3	R_DBC Cu Bot. Layer	0.00636 R_cop3				
R_0.12mm TIM	0.19468 R_TIM	R_0.12mm TIM	0.1912 R_TIM2				
R_Cold Plate	0.66252 R_AL	R_Cold Plate	0.62648 R_AL	R_Cold Plate	0.69208 R_AL	R_Cold Plate	0.67596 R_AL
R_j_Coolant	1.4836	***R_j_Coolant***	1.8828	***R_j_Coolant***	2.598	***R_j_Coolant***	2.8684

- **Case 1** has the lower thermal resistance than others.

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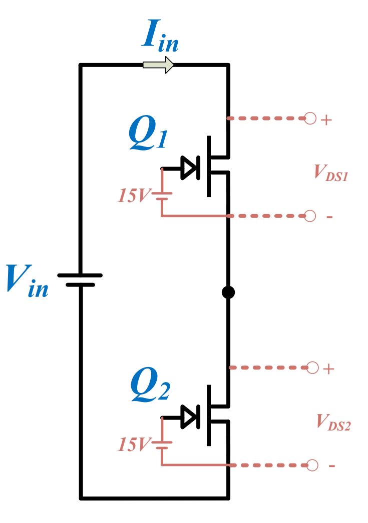
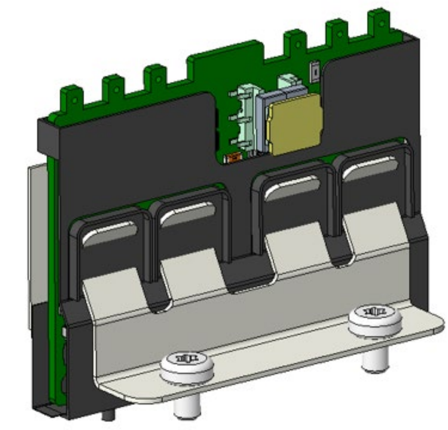
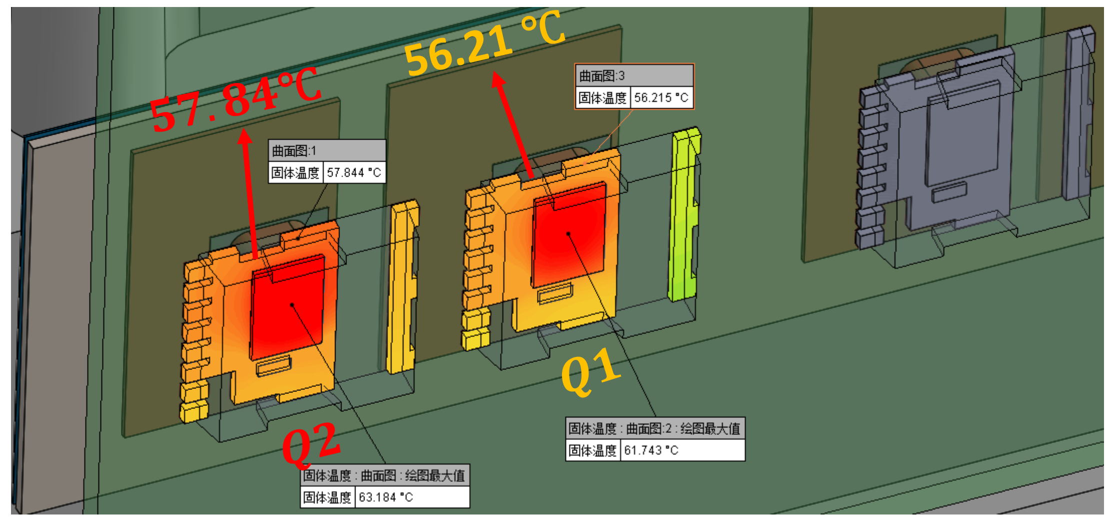
System Thermal Resistance Verification

- Q1 & Q2 short circuit.
- V_{IN} = 3 V, I_{IN} = 31.2 A
- V_{DS1} = 0.764 V, V_{DS2} =0.756 V





- **Simulation Result:**

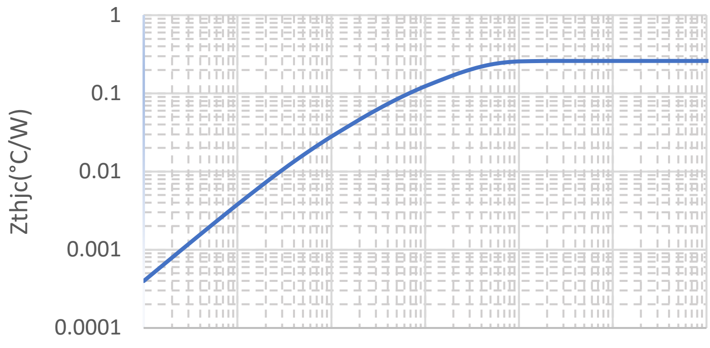


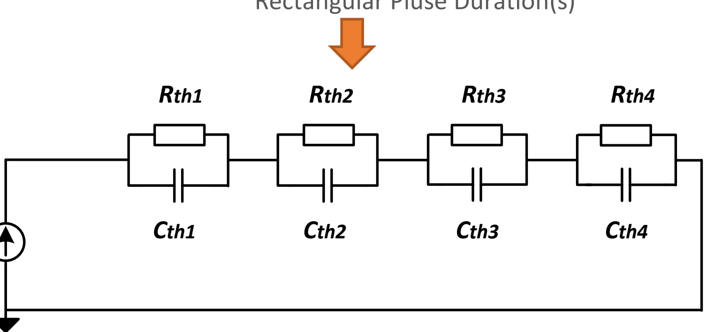
Measured Temperature and Calculated Thermal Resistance			
Device NO.	Temperature	Loss	Thermal Resistance
Q1	**56.54 ℃**	23.82 W	1.32 ℃ / W
Q2	**54.81 ℃**	23.57 W	1.26 ℃ / W

- Measured device temperature is **CASE** temperature (T_{CASE})
- Device loss is calculated by: $P = VDS \cdot Iin$
- Since the temperature of junction cannot be directly obtained during the actual test, the thermal resistance of the test is smaller than that of the simulation.

TOLL Thermal Model Available

- Transient thermal resistance





Foster model

	Rth (°C/W)	Cth(W*s/°C)	T (s)
1	7.858E-03	6.068E-03	4.77E-05
2	5.064E-02	6.609E-03	3.35E-04
3	1.000E-06	2.861E+00	2.86E-06
4	2.028E-01	1.214E-02	2.46E-03

- Transient T_j simulation for PFC stage

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Review: Bottom-Side Cooling per Package

Packaging	TOLL	PSOP-30L	SOIC-22L	D2PACK	CCPACK
Exposed Pad Area (mm^2)	60.52	96.52	37.4	49.92	60.56
Device R_j_C (°C/W)	0.174	0.203	0.113	0.816	0.146
Copper inlay (mm)	5*10	7*12	4*11.5	6.5*10.5	6*12.5
Copper inlay Area (mm^2)	50	84	46	68.25	75
Length of Pin-Fin base (mm)	62	70	70	70	70

Heating element

Heat dissipation path way

Heat Sink

Case 1 | Case 2 | Case 3 | Case 4 | Case 5

- Each packaging corresponding different thermal solution (Case1 to Case5) .

Simulation Results of T_j @ 25 W Power Loss

	TOLL	PSOP-30L	SOIC-22L	D2PACK	CCPACK
Case 1 (Solder + DBC + 0.12mm Gap-Filler)	Tj=101.8℃	Tj=96.88℃	Tj=101.1℃	Tj=112.5℃	Tj=98.66℃
Case 2 (0.12mm Gap-Filler +DBC + 0.12mm Gap-Filler)	Tj=111.8℃	Tj=103.53℃	Tj=112.74℃	Tj=121.18℃	Tj=106.5℃
Case 3 (0.8mm Gap-Filler)	Tj=129.6℃	Tj=116.7℃	Tj=129.85℃	Tj=137.51℃	Tj=121.87℃
Case 4 (0.203mm Sil-Pad)	Tj=136.6℃	Tj=122.12℃	Tj=136.62℃	Tj=144.38℃	Tj=127.89℃
Case 5 (2oz-Cu/150-micron dielectric layer/3mm-Al5052H32)		Tj=113.25℃			

- TOLL and SOIC-22L packaging have the same heat-dissipation capability.

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R_{th} Comparison (Bottom side cooling)

Case 1	Solder + DBC + 0.12mm Gap-Filler
Case 2	0.12 mm Gap-Filler +DBC + 0.12 mm Gap-Filler
Case 3	0.8 mm Gap-Filler
Case 4	0.203 mm Sil-Pad
Case 5	2 oz-Cu, 150 um dielectric layer, 3 mm-Al5052H32

- Conditions:
  - Same die size
  - Bottom-side cooling device
  - 25 W loss per device

Rth (°C/W)

	Case 1_Rth	Case 2_Rth	Case 3_Rth	Case 4_Rth	Case 5_Rth
TOLL	1.48	1.88	2.6	2.87	
PSOP-30L	1.28	1.54	2.07	2.29	1.93
SOIC-22L	1.44	1.91	2.6	2.87	
D2PACK	1.9	2.25	2.9	3.18	
CCPACK	1.35	1.66	2.28	2.52	

Different thermal treatment methods

- TOLL and SOIC-22L packaging have the same heat dissipation capability
- PSOP-30L has the best heat capability but larger PCB area

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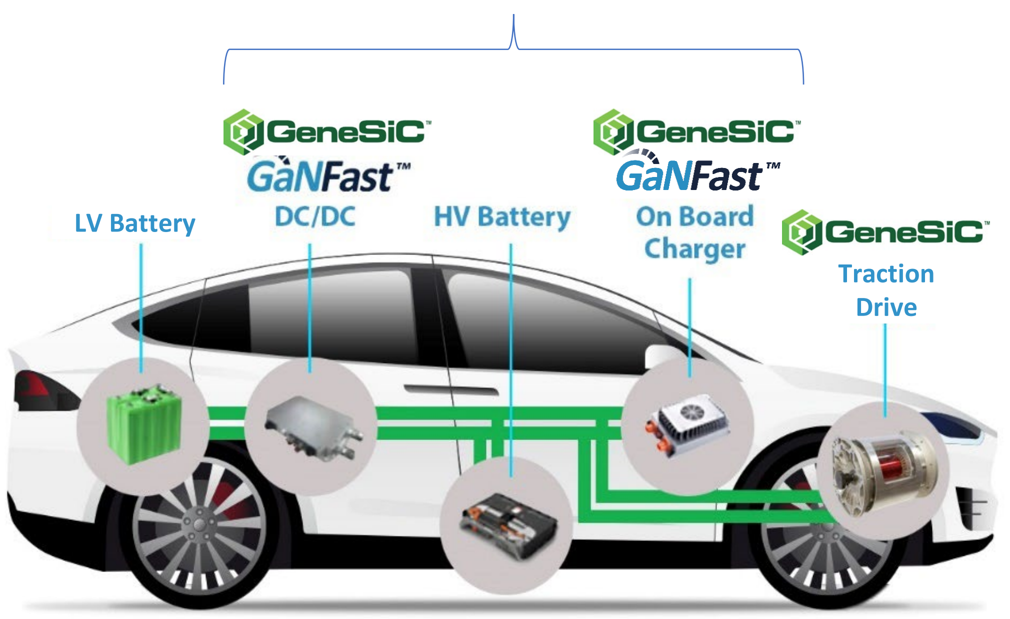
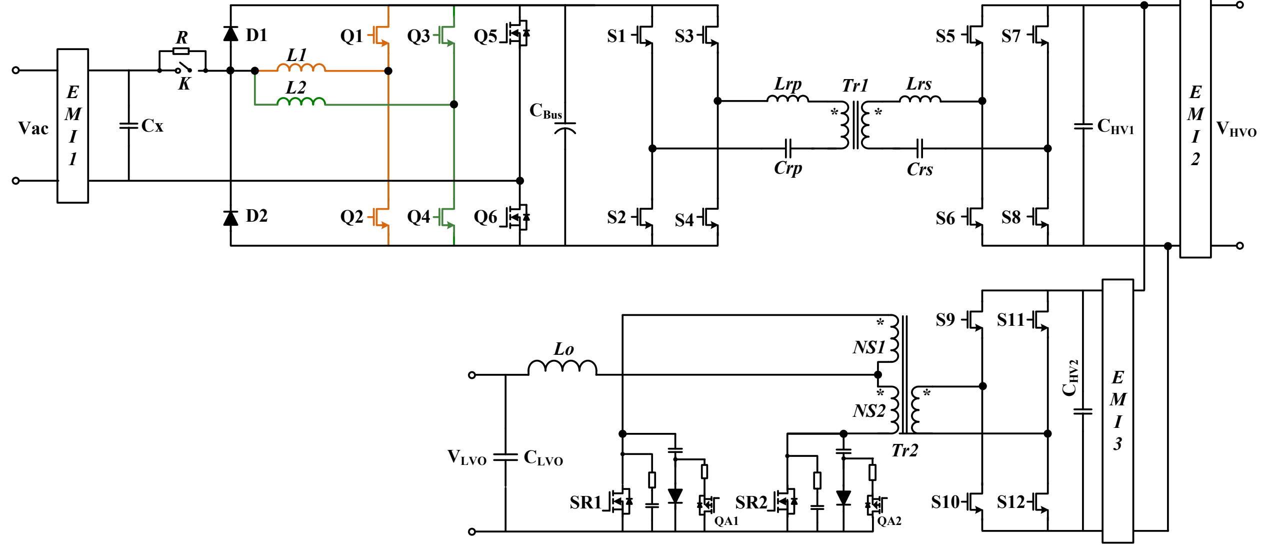
3-in-1 Bi-Directional OBC + DC-DC

- Bi-Directional 6.6kW OBC/3kW DC-DC combo
- Optimized design with 650 V GaN ***and*** 1200 V SiC





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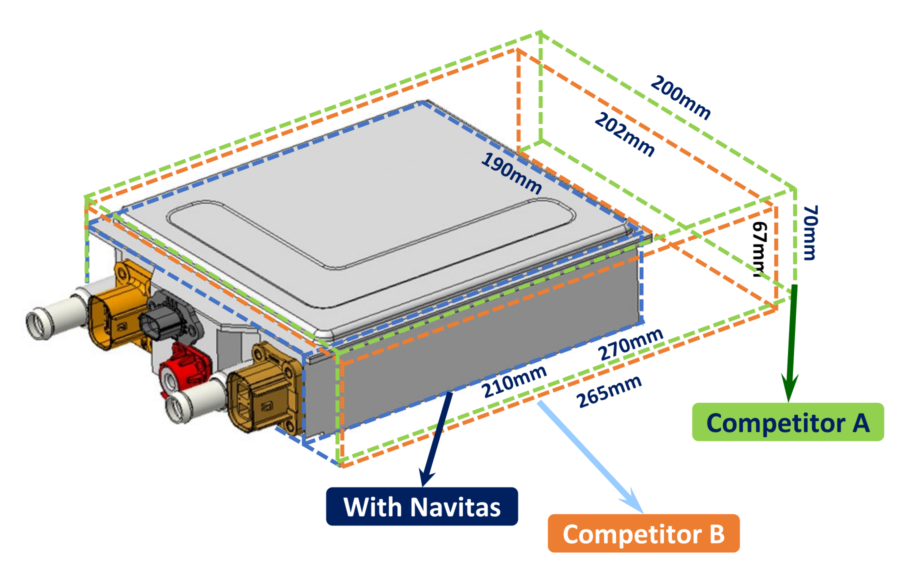
System Design Center Accelerates Customer Revenue



- Navitas' Shanghai EV System Design Center:
  - Optimized Magnetic designs, higher F_{SW}
  - Optimized system and component thermal design
- Achieves:
  - Higher efficiency
  - Higher power density
  - Lower weight
  - ***Faster time-to-market***

	Competitor A	Competitor B	Customer using Navitas
Power Density (kW/L)	2.5 kW/L	2.4 kW/L	3.9 kW/L
Efficiency (%)	>94.0%	>94.5%	>95.0%
Volume (L)	3.6L	3.8L	2.46L
Weight (kg)	6.5kg	7kg	5.5kg

Axis: 0% 20% 40% 60% 80% 100%

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Summary

- GaNFast power ICs and GeneSiC MOSFETs enable high frequency, high efficiency, higher power density
- Small die size and package size bring thermal challenges for high-power applications
- Copper inlay technology is an effective method for bottom-side cooling
- Packaging types are reviewed, and thermal designs analyzed
- Results show that DBC heat insulation technology is the best strategy
- NVTS roadmap includes TOLL and more package types for different high-power applications

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2022中国电力电子与能量转换大会
暨中国电源学会第二十五届学术年会及展览会
2022 China Power Electronics and Energy Conversion Congress
& The 25th China Power Supply Society Conference and Exhibition

"GaNFast™ and GeneSiC™: Twin Engines Drive the Future of High-Power Applications"

Minli.Jia, Zhen.Zhou, Fisher Xu, Hao.Sun

Navitas

Energy • Efficiency • Sustainability

谢谢！

Navitas GaNFast™ Power IC

Navitas GeneSiC Power

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