

GaNSense™ Power ICs Enable Next-Gen, Ultra-High-Efficiency and High-Power-Density 140 W, PD3.1 Adapter Designs

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Introduction

This article presents an ultra-high-efficiency and high-power-density design of a power factor correction (PFC) and asymmetrical half-bridge (AHB) flyback converter for 140 W PD3.1 adapter applications. GaNSense power ICs are used in the boost PFC design for higher frequency, smaller inductor, and higher efficiency. GaNSense half-bridge ICs are used to enable the ZVS AHB flyback topology to operate at higher frequencies with a smaller transformer and higher efficiency. A 140 W PD 3.1 evaluation board is presented that demonstrates the functionality and performance of the complete system design. The evaluation board achieves 94.5% efficiency at 90 V_{AC} and 95.8% at 230 V_{AC} which is at least 1% higher efficiency and with up to 20% energy savings vs. prior state-of-the-art designs. The estimated cased size is 100 cc, for power density of 1.4 W/cc.

Higher Speed + Higher Efficiency = Smaller Size

The growing demand for size reduction of power supplies has continuously challenged the industry to produce higher and higher efficiencies and power densities. The ability to improve the performance of silicon-based power supplies has slowed due to silicon devices reaching their maximum frequency limit (<100 kHz), which has prevented further optimization of circuit topologies and magnetic design. Emerging GaN wide-bandgap devices have enabled significant incremental efficiency and size improvements due to their 15x lower Q_G gate charge, 16x lower Q_{oss} output charge, and higher switching speeds. GaNSense power ICs have enabled these devices to finally exit the lab and enter actual real-world fast chargers and adapters by integrating all of the missing ingredients needed for reliable and robust designs. These include integrated gate drive, regulated gate voltage, loss-less current sensing, and protection features and are included in GaNSense power ICs and GaNSense half-bridge ICs (Figure 1). These latest products are enabling new circuit topologies, and the industry is using them to progress ahead with smaller and more efficient designs.

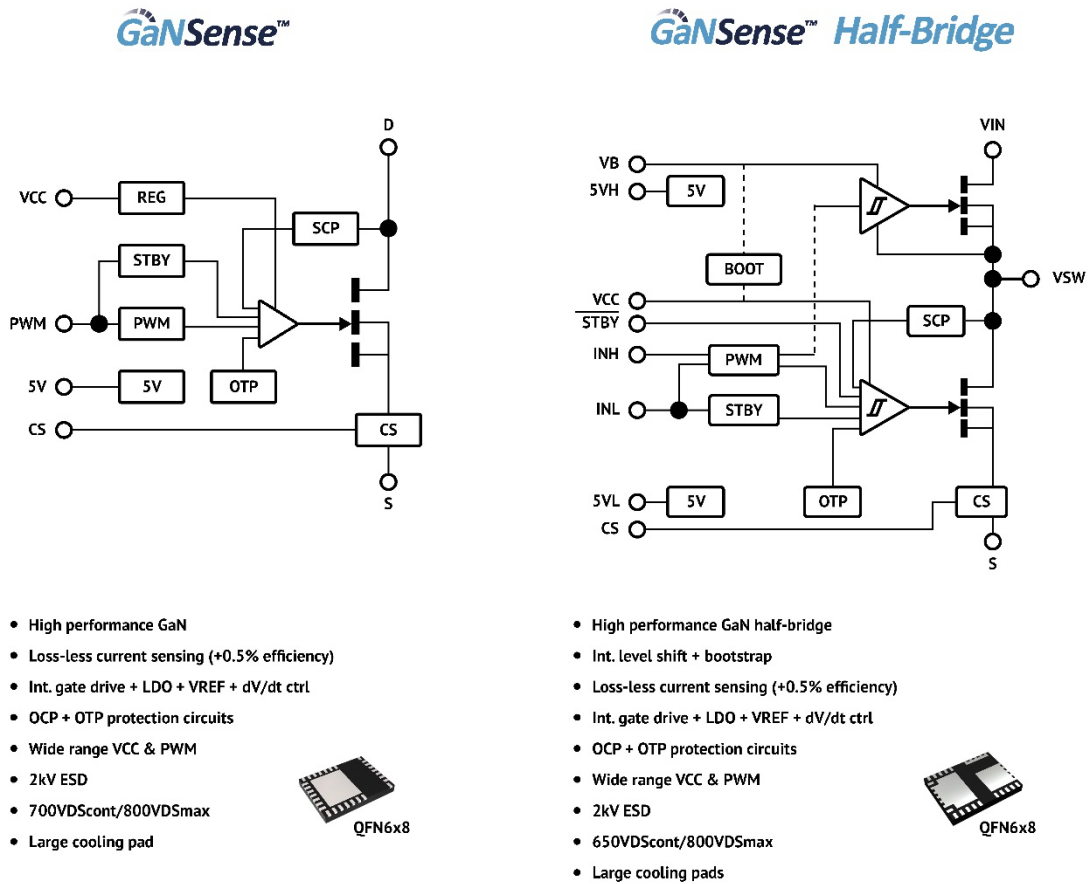


Figure 1. GaN Sense power IC and GaN Sense half-bridge IC simplified block diagrams and key features.

GaN Sense Boosts PFC Frequency and Efficiency

Power factor correction (PFC) is required for output powers greater than 75 W. The traditional boost PFC converter has dominated due to its simplicity, low harmonic current, and low cost. Many off-the-shelf PFC controllers are available that provide multi-mode CRM or DCM operation to improve system efficiency and line-current harmonics. GaN Sense power ICs improve this topology by increasing the switching frequency to reduce the inductor size and increasing efficiency to reduce losses and thermals (Figure 2). The integrated GaN FET allows the frequency to be increased easily due to the lower output-charge and lower gate-charge compared to silicon FETs. To increase the efficiency, GaN Sense power ICs integrate a loss-less current sensing method that completely eliminates the external R_{CS} current-sensing resistor and its associated hotspot and footprint.

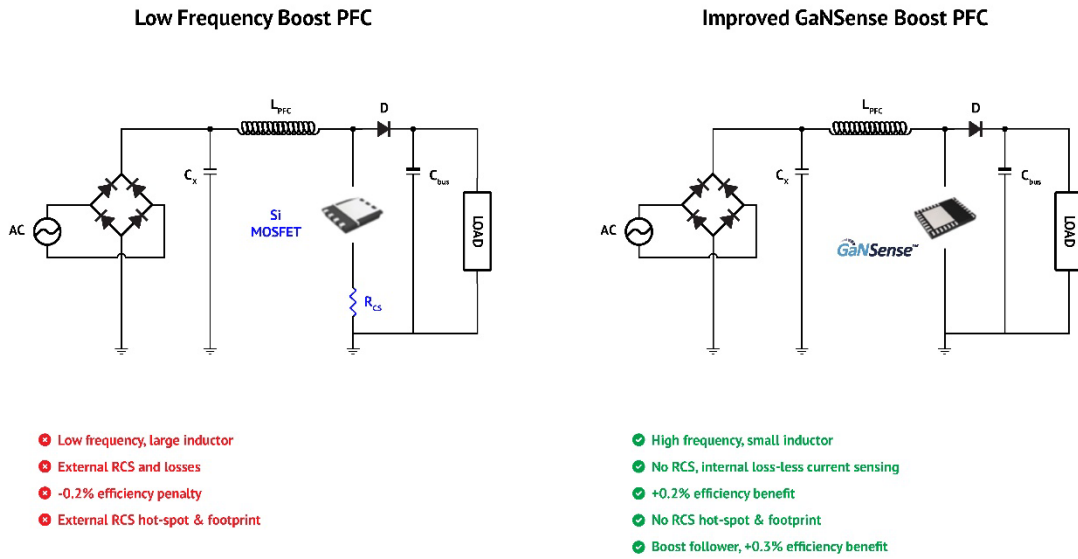


Figure 2: Si-based boost PFC (left) vs Loss-less GaNSense boost PFC (right)

To further improve efficiency, a boost-follower function can be added so that the DC bus operates at a lower voltage during low-line AC input. This gives lower peak-current levels, lower negative current and circulating energy, and lower core losses (Figure 3). All of these improvements combined give an additional +0.3% efficiency benefit.

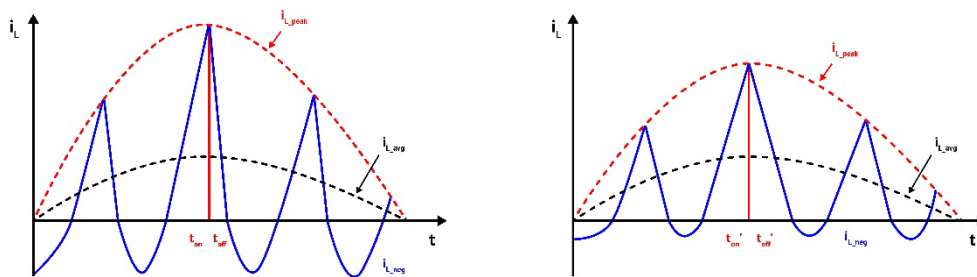


Figure 3: Boost peak-inductor currents over AC half-cycle at full-load and different DC-bus voltage levels, 90 $V_{AC}/400$ V (left) and 90 $V_{AC}/260$ V (right)

GaNSense enables AHB, and AHB enables PD 3.1

The quasi-resonant flyback is a popular topology for the downstream converter due to its wide voltage gain capability. However, as power levels increase above 100 W, the transformer leakage energy increases significantly. As the leakage energy increases, the voltage stress on the primary switch and secondary SR switch also increases, including higher voltage spikes and EMI noise. In addition, the USB Power Delivery Specification Revision 3.1 enables higher output-voltage levels, e.g., 28 V to 48 V, which makes the flyback transformer turns-ratio more difficult to design. The voltage stress on both primary and secondary is much higher than the traditional 20 V output condition. The asymmetrical half-bridge flyback converter operates with zero-voltage switching (ZVS) of the primary-side switches and zero-current switching (ZCS) of the secondary-side rectifier. Moreover, the primary switches are clamped at the PFC output voltage, typically around 400 V, so the stress and voltage ringing issues are significantly relieved. For these reasons, the AHB topology is the preferred choice for PD 3.1 applications, and GaNSense half-bridge ICs enable high-frequency operation for small transformer size and loss-less current sensing for higher efficiency (Figure 4).

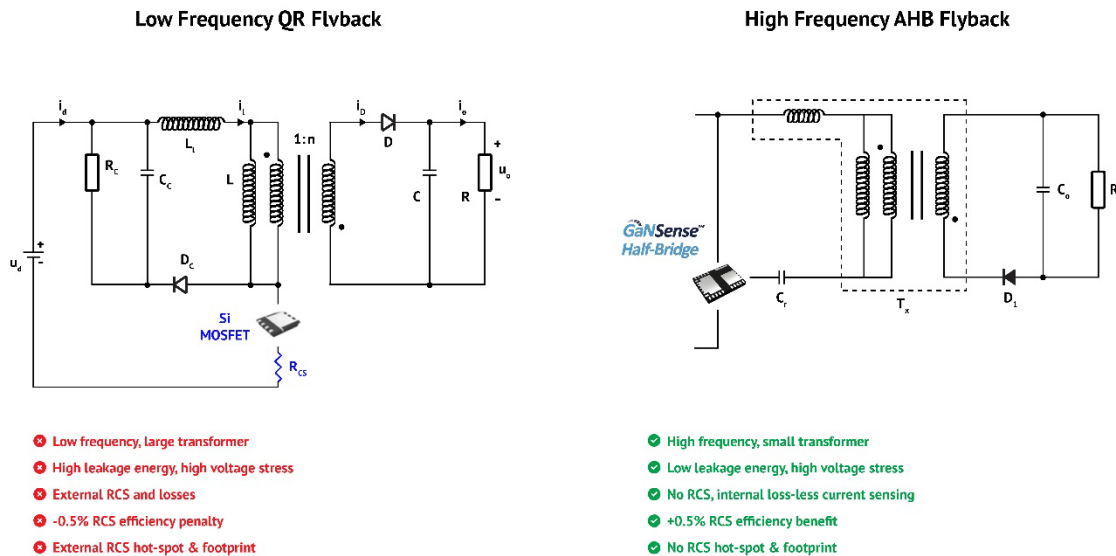


Figure 4: Si-based QR flyback (left) vs Loss-less GaNSense AHB flyback (right)

140 W, PD 3.1 Evaluation Board

A complete PFC+AHB 140 W, PD 3.1 evaluation board (EVB, Figure 5) has been built and tested for functionality and performance. The design achieves an impressive 100 cc estimated cased size, with 1.4 W/cc power density. The EVB includes optimized PFC, AHB, and SR power stages and magnetics and uses off-the-shelf controllers. The PFC and AHB power trains are designed around the NV6138A GaNSense power IC and the NV6245C GaNSense half-bridge IC. The EVB also includes EMI filtering and passes both conducted and radiated emissions.

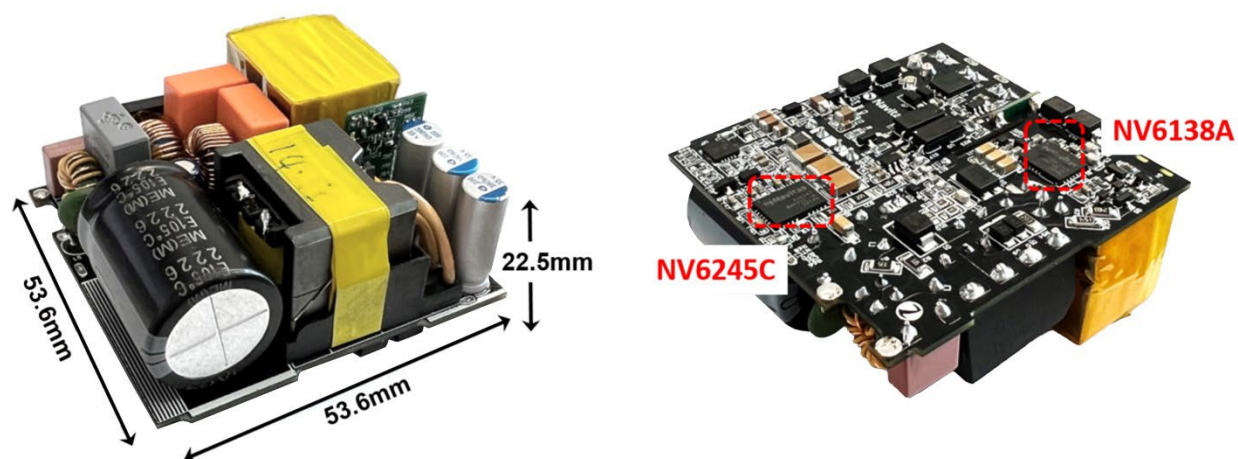


Figure 5: S140 W, PD 3.1 evaluation board, efficiency = 94.5%, estimated cased size = 100 cc

The full-load boost PFC waveforms are shown in Figure 6. During 115 V_{AC} line input, the boost circuit operates in zero-voltage switching (ZVS) conditions, where the boost-switched node-voltage (V_{SW}) slews down to zero before the GaN power FET turns on, in each switching cycle. During 230 V_{AC} line input, the boost circuit operates in partial-ZVS conditions, where V_{SW} slews down to approximately 100 V and then hard-switches from there to zero. The controller automatically detects the valley of the V_{SW} node during the off-time for turning on again each switching-cycle to optimize the turn-on point at the lowest voltage level possible to minimize hard-switching losses. Since GaN power ICs have very-low output capacitance, the drain voltage will slew quickly down to the valley each cycle. It is critical that the controller has fast valley-detection to ensure that turn-on occurs at the lowest point before the V_{SW} voltage can ring back up. The boost-follower function can also be seen working with the DC bus voltage down at 300 V_{DC} during low-line conditions and up at 400 V_{DC} during high-line conditions.



Figure 6: Boost PFC switching waveforms during full load conditions, 115 V_{AC} input (left), 230 V_{AC} input (right), I_L =blue (1 A/div), V_{DS} =yellow (100 V/div)

The AHB half-bridge switch node (V_{sw}) and tank current (I_L) waveforms during 115 V_{AC} input and full load conditions are shown in Figure 7. The resonant tank current ramps up linearly during each half-bridge low-side on-time and then resonates during each half-bridge high-side on-time. This results in clean and smooth ZVS operation at the GaNSense half-bridge IC V_{sw} output node during each switching cycle. The AHB operating frequency ranges from 125 to 300 kHz, depending on input line and output load conditions.

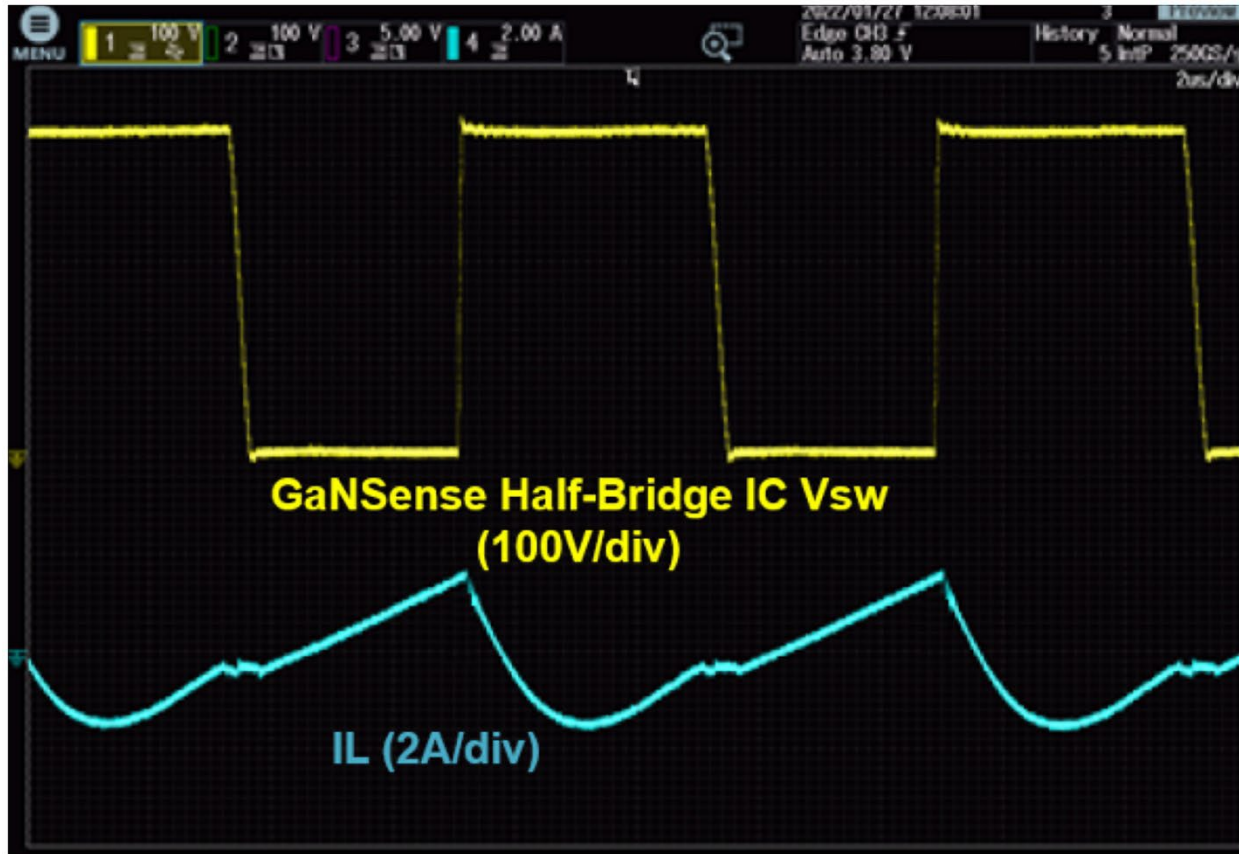


Figure 7: AHB switching waveforms during 115 V_{AC} input and full load conditions, I_L=blue (2 A/div), V_{sw}=yellow (100 V/div)

The efficiency curves (Figure 8) show both 4-point efficiency and maximum load efficiency. This design achieves amazing 94.5% full-load efficiency at 90 V_{AC} input which is at least 1% higher than the state of art product, representing up to 20% energy savings. The efficiency at 90 V_{AC} and full-load is the efficiency that determines the cased size and resulting case touch-temperature of the final adapter product.

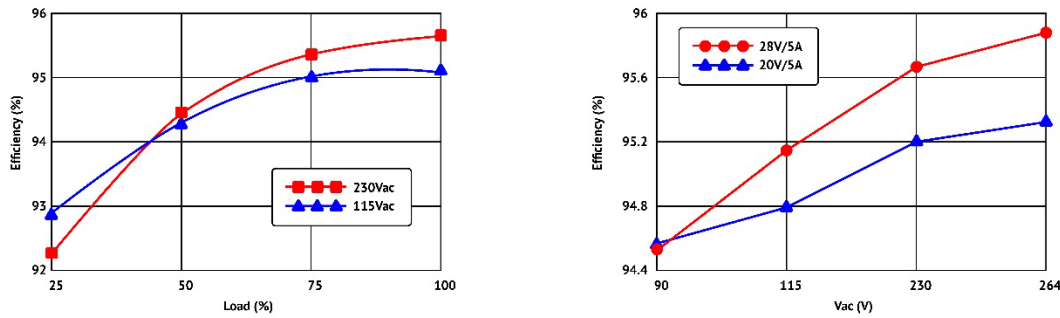


Figure 8: 4-point efficiency (left) and maximum load efficiency (right) curves

Finally, the conducted and radiated EMI are always a major concern with power supply designs. New designs with GaN continuously come into question concerning challenges with EMI due to the faster switching speeds and frequencies. Designers typically do not tackle the EMI portion of their design until it is nearing the completion phase, only to be surprised and learn that the emissions are far above the allowable limits. From the EMI scans for this design (Figure 9) it can be seen that both conducted and radiated EMI both are well below the limits with sufficient margin for manufacturing tolerances. These results are achievable by implementing proper EMI guidelines as early in the design phase as possible, and include such good practices as PCB ground planes, inductor shielding, properly designed EMI filter components, correct PCB floor planning and component locations and proximity.

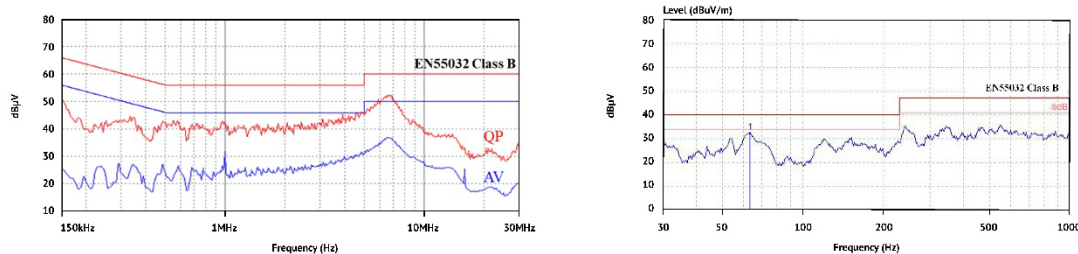


Figure 9: Conducted emissions at 115 V_{AC}/140 W (left) and radiated emissions at 230 V_{AC}/140 W (right)

Conclusion

With the industry in pursuit of higher-density designs, GaNSense power ICs and GaNSense half-bridge ICs lead the way to higher frequencies, improving existing topologies, unlocking future topologies, and ultimately achieving higher efficiencies. Next-generation, high-frequency controllers are also required, as well as new magnetic materials to enable a complete high-speed eco-system, which enables lower temperatures and smaller sizes. Improving existing PFC circuits or using new circuits such as AHB are only small examples of what is possible. More innovation is waiting around the corner as GaN continues to improve and unlock existing and new topologies.

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