Gate Reliability of Trench-Assisted Planar SiC MOSFETs

Arash Salemi, Vamsi Mulpuri, Vishank Talesara, Sumit Jadav, and Uday Vangaveti

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1.1 Introduction

Silicon Carbide (SiC) power semiconductors have emerged as a transformative technology, revolutionizing power electronics across diverse applications—from AI data centers and electric vehicles to grid infrastructure and industrial systems. Their wide bandgap properties offer significant advantages over traditional silicon (Si) devices, including higher breakdown voltages, faster switching speeds, lower on-resistance, and superior thermal conductivity. These characteristics enable the design of more compact, efficient, and robust power conversion

systems, leading to reduced energy losses, smaller form factors, and enhanced overall performance. However, the widespread adoption of SiC for mission-critical applications hinges on proven reliability and the establishment of comprehensive qualification methodologies. While SiC offers inherent material advantages, it also introduces new challenges that require rigorous characterization. This white paper delves into the critical aspects of gate oxide reliability for SiC MOSFETs and discusses how Navitas Semiconductor is pioneering qualification with new and extended stress testing.

The SiC/SiO_2 interface in SiC MOSFETs typically exhibits a higher density of interface traps compared to Si/SiO_2 in Si MOSFETs. In a non-optimized process, this elevated trap density can lead to several reliability challenges, such as time-dependent dielectric breakdown (TDDB) and bias-temperature instability (BTI), affecting the threshold voltage stability ($V_{GS,TH}$) and the long-term integrity of the gate oxide. Extrinsic defects in the gate oxide are a particular focus for improvement. This white paper will detail various DC and AC stress tests, including high, low, and room temperature gate bias (HTGB, LTGB, RTGB) and gate switching (HTGS, LTGS, RTGS), along with TDDB and BTI characterization, to model the lifetime of the gate oxide under diverse operating conditions, including specific use case scenarios for AI data center power supply units (PSU) , and solid-state transformers (SST).

1.2 Gate Reliability in SiC MOSFETs

Ensuring gate reliability oxide is so important for SiC MOSFETs, particularly as they operate at higher temperatures, frequencies, and voltages than their silicon counterparts. The gate oxide is a critical insulating layer in Metal-Oxide-Semiconductor (MOS) devices, fundamentally determining device performance and long-term stability. For SiC MOSFETs, this layer is typically silicon dioxide (SiO_2), similar to silicon devices, but the interface between SiO_2 and SiC presents unique challenges. Its reliability is paramount, especially in power applications where SiC devices operate under extreme electrical fields, higher temperatures, and faster switching speeds. Degradation of the gate oxide can lead to shifts in threshold voltage, increased leakage current, and ultimately, catastrophic gate dielectric breakdown. Understanding and characterizing these degradation mechanisms through various stress tests is essential for predicting device lifetime and ensuring robust product operation in demanding SiC applications.

1.3 Trench-Assisted Planar SiC MOSFET Technology

Navitas' GeneSiC™ trench-assisted planar (TAP) SiC MOSFET technology uses a planar gate structure. In this architecture, the conduction channel—where the current flows—is primarily created on the top surface of the SiC wafer. By leveraging a planar configuration, Navitas simplifies the fabrication process relative to traditional trench technologies; these processes are generally less complex, leading to higher manufacturing yields than those requiring deep-etched, high-aspect-ratio trenches.

While the gate remains planar, the "trench-assisted" designation refers to shallow trenches strategically integrated into the source regions of the device as shown in Fig.1. Unlike standard trench MOSFETs, these trenches are not intended to create the primary current path. Instead, they are engineered to:

- **Optimize Electric Field Distribution:** Enhances overall device reliability and structural robustness.
- **Reduce On-Resistance ($R_{DS,ON}$):** Maintains superior performance even at elevated operating temperatures.
- **Improve Switching Performance:** Minimizes parasitic losses for high-frequency applications.
- **Enhance Gate Oxide Integrity:** Protects the critical oxide layer from high-field stress.

For an in-depth exploration of **Trench-Assisted Planar SiC MOSFET Technology**, please consult the full white paper available at:https://navitassemi.com/download/trench-assisted-planar-sic-mosfet-technology/?wpdmdl=987505683&ind=987505684.

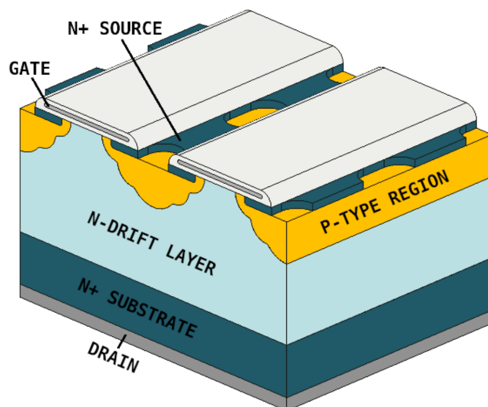

Fig. 1. Schematic cross-sectional view of Trench-Assisted Planar (TAP) technology

1.4 DC Stress

DC stress involves applying a constant voltage bias to the gate oxide for an extended period to simulate steady-state operating conditions. For SiC MOSFETs, this stress is crucial for evaluating long-term gate oxide reliability under continuous electrical fields. Such conditions can lead to phenomena like charge trapping and interface state generation, which are often exacerbated by the specific quality of the SiC/SiO_2 interface.

Fig. 2 through Fig. 5 illustrate the results of various DC stress tests performed on the gate oxide of Navitas' trench-assisted planar SiC MOSFETs. Notably, none of the stressed devices exhibited a threshold voltage ($V_{GS,TH}$) shift greater than 200 mV. This stability confirms that the devices show no signs of degradation under these conditions.

To further validate long-term reliability and identify potential failure mechanisms, extensive testing was conducted on a large statistical sample of 240 parts (3 lots x 80 parts), consistent with standard AEC-Q101 and JEDEC qualification sizes. After 3,000 hours of testing, no failures were discovered, and no significant shifts in key parameters were observed.

1.4.1 High Temperature Gate Bias (HTGB)

High Temperature Gate Bias (HTGB) testing involves applying a constant gate voltage at elevated temperatures, as illustrated in Fig. 2 and Fig. 3. This is particularly critical for SiC MOSFETs given their wide bandgap and inherent capability for high-temperature operation. These accelerated stress conditions exacerbate temperature-dependent degradation mechanisms, making HTGB a key test for predicting operational lifetimes. It also provides vital insights into the thermal activation energy of degradation, which typically differs from that of traditional Si devices.

All Navitas' SiC MOSFET technology platforms undergo extended HTGB testing prior to production release, with results documented in formal product qualification reports. To ensure reliability beyond standard requirements, HTGB tests were performed for at least 3,000 hours—far exceeding industry norms—to verify technological robustness. Fig. 2 and Fig. 3 demonstrate that all primary parameters of Navitas' SiC MOSFETs remain stable after 3,000 hours at 175°C and 200°C under both positive and negative gate bias (+22V/-10V).

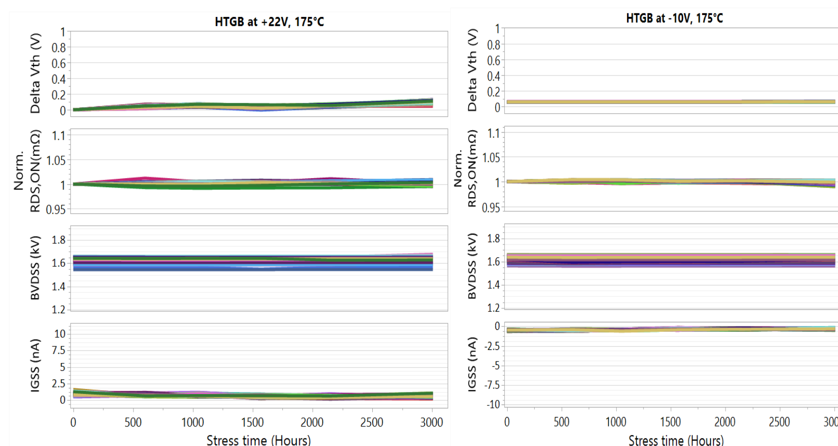

Fig. 2. 175°C HTGB test results at V_{GS}=+22V (left) and V_{GS}=-10V (right).

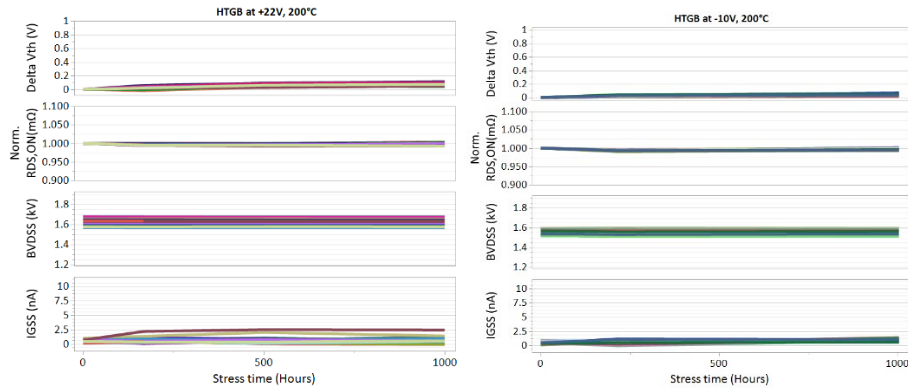

Fig. 3. 200°C HTGB test results at V_{GS}=+22V (left) and V_{GS}=-10V (right).

1.4.2 Low Temperature Gate Bias (LTGB)

Low Temperature Gate Bias (LTGB) testing involves applying a constant gate voltage at reduced temperatures, as illustrated in Fig. 4. While high-temperature testing is more common for SiC, LTGB is essential for understanding specific low-temperature charge trapping phenomena and device behavior during cold start-up in applications such as energy and grid infrastructure. This testing assesses SiC device stability under sub-ambient conditions to ensure reliable performance in extreme environments.

As shown in Figure 3, the primary device parameters of Navitas' SiC MOSFETs remain stable after 1,000 hours of testing at -60°C. This stability was maintained under both positive and negative gate bias conditions (+22V/-10V).

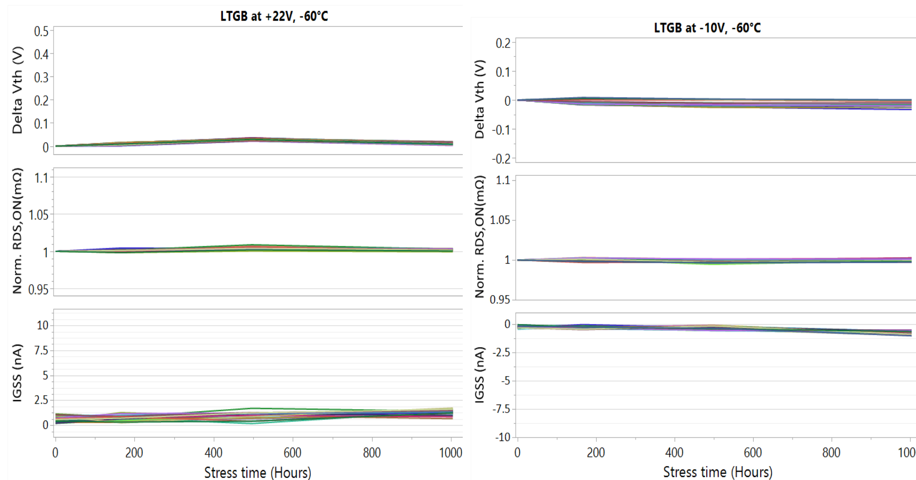

Fig. 4. -60°C LTGB test results at V_{GS}=+22V (left) and V_{GS}=-10V (right).

1.4.3 Room Temperature Gate Bias (RTGB)

Room Temperature Gate Bias (RTGB) involves applying a constant gate voltage at ambient temperature (e.g., 25°C), as illustrated in Fig. 5. This test serves as a critical baseline for comparison with accelerated stress conditions and provides direct insight into SiC gate oxide stability under standard operating environments. By testing at room temperature, it is possible to isolate degradation mechanisms that are less temperature-dependent. As shown in Fig. 5, the primary parameters of Navitas' MOSFETs remain stable after 1,000 hours at 25°C under both positive and negative gate bias (+22V/-10V).

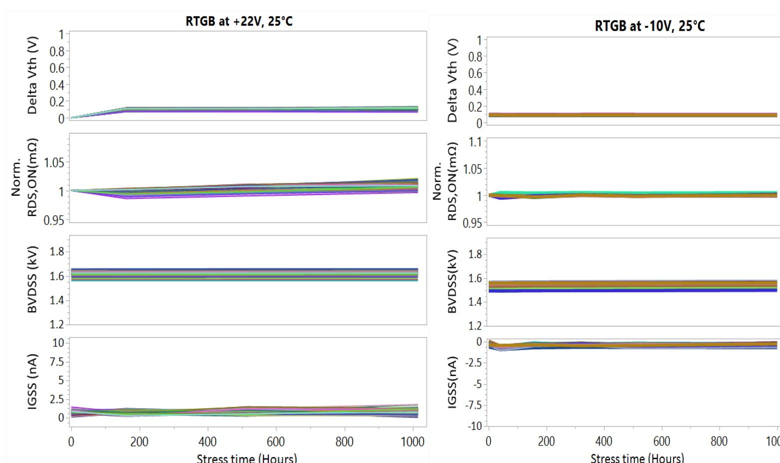

Fig. 5. 25°C RTGB test results at V_{GS}=+22V (left) and V_{GS}=-10V (right).

1.5 AC Stress

AC stress involves applying dynamic, switching voltage stress to the gate to mimic the actual operation of SiC power devices within power converters. This testing is critical as it captures degradation mechanisms unique to high-frequency, high dV/dt, and high-temperature transient operations. These include effects caused by hot carrier injection and the repeated charge-discharge cycles of the gate, which are often more severe in high-frequency SiC applications. A typical gate switching waveform used for this dynamic stress testing is illustrated in Fig. 6.

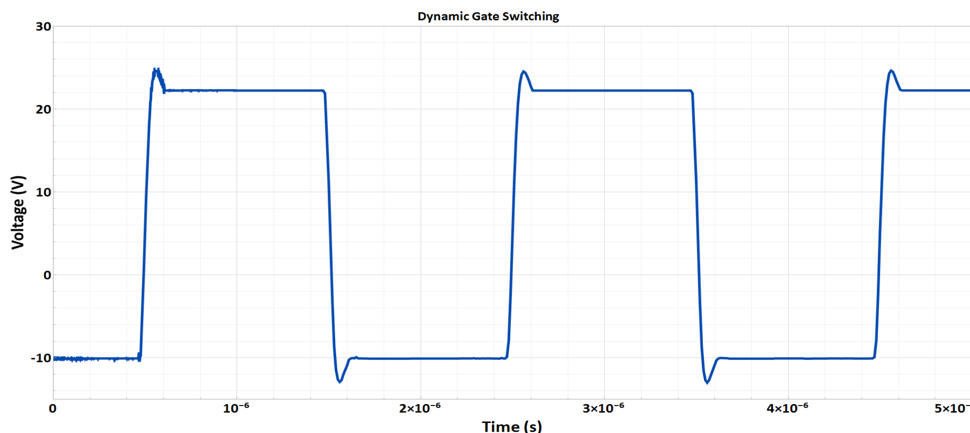

Fig. 6. A typical gate switching waveform for dynamic stress testing. The conditions for dynamic gate switching are as follows: V_{GS}: +22V/-10V ($V_{GS,pk}$: +25V/-12V); f_{sw}: 500kHz; HTGS: 175°C, RTGS: 25°C, LTGS: -40°C.

Fig. 7 through Fig. 10 illustrate the various AC stress conditions applied to the gate oxide of Navitas' trench-assisted planar SiC MOSFETs. Notably, none of the stressed devices exhibited an increase in $V_{GS,TH}$ exceeding 600 mV after 1.75 x 10^{12} cycles.

To identify potential failure mechanisms and validate long-term reliability, testing was conducted on a large statistical batch of 240 units (consistent with AEC-Q101 and JEDEC qualification standards). These tests extended beyond 1,000 hours, with no reported failures or significant shifts in key device parameters.

1.5.1 High Temperature Gate Switching (HTGS)

High Temperature Gate Switching (HTGS) involves applying dynamic gate voltage stress at elevated temperatures. This test is critical for SiC MOSFETs given their capability for high-frequency switching and operation at high junction temperatures. HTGS simulates the combined effects of thermal stress and rapid switching, which can trigger dynamic charge trapping, interface state generation, and significant hot carrier degradation.

Hot carrier injection is a particularly important consideration for SiC gate oxides, as the high electric fields present during switching can accelerate carriers to energy levels sufficient to damage the SiC/SiO_2 interface. Consequently, HTGS provides a more realistic assessment of the operational lifetime for SiC devices in high-frequency power conversion applications. As shown in Fig. 7, the primary parameters of Navitas' MOSFETs remain stable after 1,000 hours of testing at 175°C with a V_{GS} of +22V/-10V.

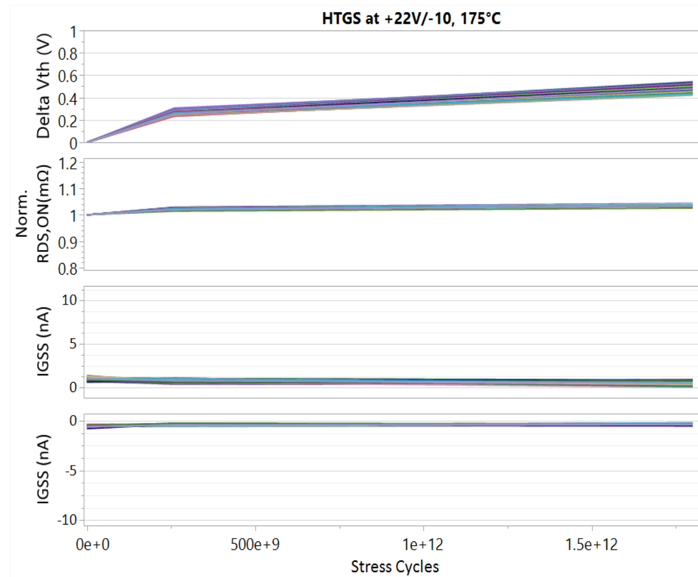

Fig. 7. 175°C HTGS test results at V_{GS}=+22V/-10V.

Fig. 8 compares the HTGS test results of Navitas' 1200V SiC MOSFETs against competing SiC MOSFET technologies currently available on the market. These results demonstrate how Navitas' unique Trench-Assisted Planar (TAP) technology achieves the lowest $V_{GS,TH}$ shift, highlighting its superior stability and performance.

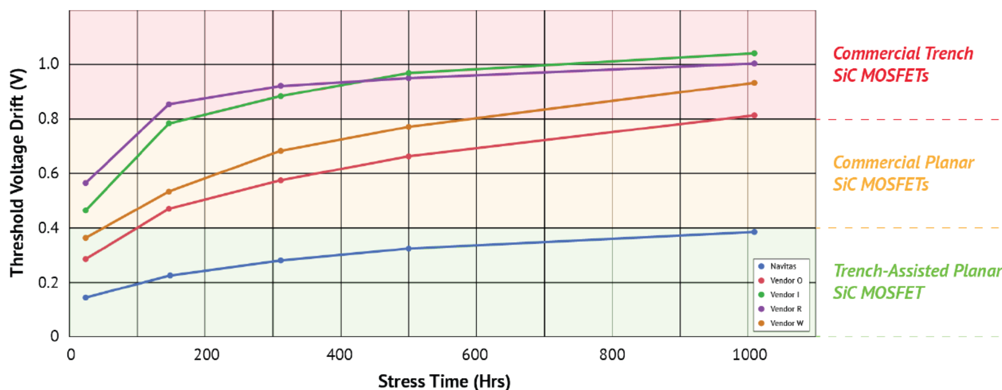

Fig. 8. Gate threshold voltage shifts after HTGS for commercially available 1200V SiC MOSFETs.

1.5.2 Low Temperature Gate Switching (LTGS)

Low Temperature Gate Switching (LTGS) involves applying dynamic gate voltage stress at reduced temperatures. This test addresses specific SiC applications where devices must operate with continuous switching in cold environments, such as in automotive or aerospace sectors. It evaluates the impact of low-temperature dynamic stress on gate oxide integrity, capturing charge trapping dynamics or hot carrier effects that may differ significantly from those

observed at high temperatures. As shown in Fig. 9, the primary parameters of Navitas' MOSFETs remain stable after 1,000 hours of testing at -40°C with a V_{GS} of +22V/-10V.

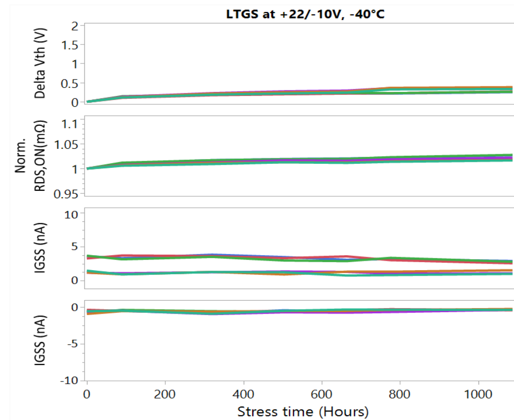

Fig. 9. -40°C LTGS test results at V_{GS}=+22V/-10V.

1.5.3 Room Temperature Gate Switching (RTGS)

Room Temperature Gate Switching (RTGS) applies a dynamic gate voltage at ambient temperature. This test provides a baseline for evaluating SiC gate oxide degradation under typical switching conditions without the added acceleration of temperature. Such testing is essential for understanding the intrinsic dynamic reliability of the gate oxide within standard operating environments. As shown in Fig. 10, the primary parameters of Navitas' MOSFETs remain stable after 1,000 hours at 25°C with a V_{GS} of +22V/-10V.

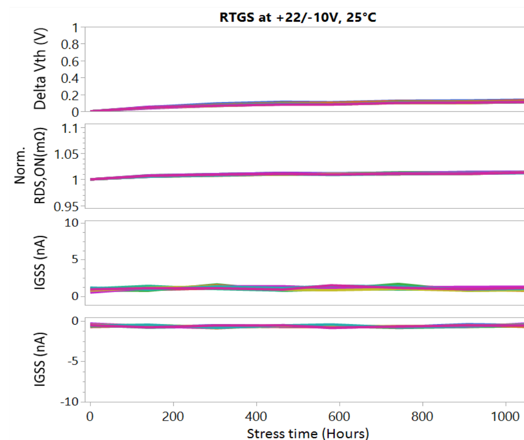

Fig. 10. 25°C RTGS test results at V_{GS}=+22V/-10V.

1.6 Time Dependent Dielectric Breakdown (TDDB)

Time-Dependent Dielectric Breakdown (TDDB) is a critical reliability test used to evaluate the

intrinsic lifetime of the gate oxide in SiC MOSFETs. The primary failure mechanism in TDDB is the loss of the oxide's insulating properties, which results in a permanent short circuit between the gate and the channel. This failure occurs due to the gradual accumulation of defects within the oxide under electrical stress, eventually forming a conductive percolation path. Because the SiC/SiO_2 interface inherently possesses a higher defect density than the Si/SiO_2 interface, TDDB presents a significant challenge for SiC device design and process optimization.

To perform this evaluation, SiC MOSFETs are subjected to a combination of gate bias and temperature while their times-to-failure (TTF) are recorded. Weibull statistical distributions are then employed to extract and predict operational lifetimes. Fig. 11 presents constant-voltage TDDB data for production SiC MOSFETs stressed at 175°C, with oxide fields ranging from 8.5 MV/cm to 9.5 MV/cm.

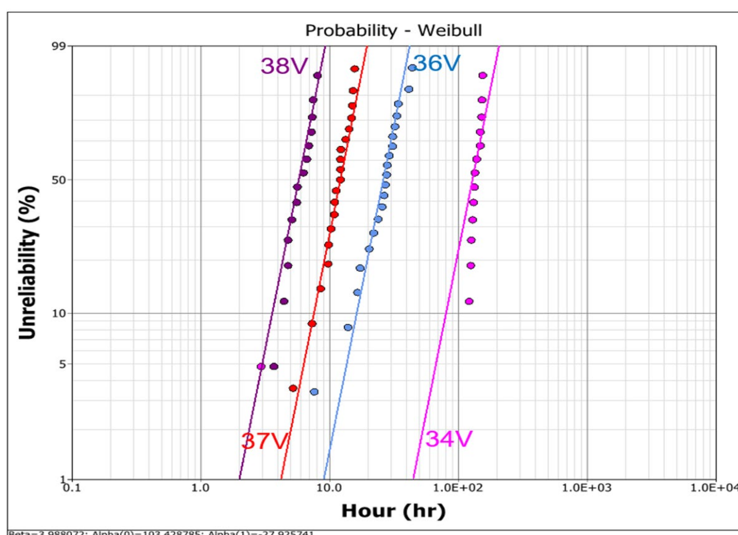

Fig. 11. 175°C TDDB data of Navitas' 4th generation high-voltage SiC TAP MOSFETs stressed at oxide fields ranging from 8.5 MV/cm to 9.5 MV/cm

1.6.1 Lifetime Modeling

Lifetime modeling for TDDB involves accelerating breakdown through high electric fields and temperatures to predict the time-to-failure under normal operating conditions. Common frameworks such as the E-model and 1/E model are frequently applied to SiC MOSFETs. However, the specific parameters and activation energies for these models can differ significantly from silicon due to the unique SiC/SiO_2 interface properties and defect generation mechanisms.

By combining these models with temperature acceleration, short-term test data can be extrapolated to predict device longevity over several decades. This provides essential data for assessing SiC power semiconductors in mission-critical applications. Fig. 12 compares Navitas'

SiC MOSFETs with those of two other manufacturers. The data shows that Navitas reaches a 20-year lifetime at a V_{GS} of 27 V, which is well above the recommended operating voltage (+15 V or +18 V) and the maximum rated operating voltage (+22 V). Consequently, Navitas' Trench-Assisted Planar (TAP) SiC MOSFETs demonstrate a significantly higher lifetime than the competing technologies.

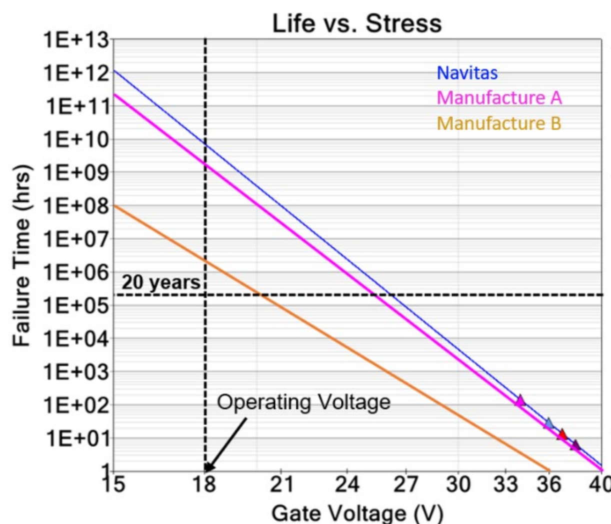

Fig. 12. 175°C failure time vs. gate voltage.

1.7 Bias Temperature Instability (BTI)

Bias Temperature Instability (BTI) refers to a shift in a SiC MOSFET's gate $V_{GS,TH}$ when subjected to a constant gate bias at elevated temperatures. BTI is a particularly prominent reliability concern for SiC MOSFETs because the SiC/SiO_2 interface inherently contains a higher density of interface and border traps compared to the Si/SiO_2 interface.

These characteristics make non-optimized SiC devices more susceptible to $V_{GS,TH}$ shifts caused by the trapping and de-trapping of charges. Such instability can significantly impact circuit performance and long-term reliability by altering the device's switching characteristics and $R_{DS(ON)}$.

1.7.1 Positive Bias Temperature Instability (PBTI)

Positive Bias Temperature Instability (PBTI) occurs when a positive gate voltage is applied to an n-type SiC MOSFET at elevated temperatures. This stress typically leads to electron trapping within the oxide or the creation of donor-like interface states at the SiC/SiO_2 interface, resulting in a positive shift in the $V_{GS,TH}$.

PBTI is a significant concern for non-optimized SiC MOSFETs, as its magnitude is strongly influenced by the quality of the gate oxide processing and the SiC/SiO_2 interface. Fig. 13 displays the PBTI results for Navitas' SiC TAP MOSFETs under high stress voltages at 175°C. The data demonstrates that $V_{GS,TH}$ increases by only approximately 0.2 V after 3,000 seconds of stress at V_{GS}=+25V.

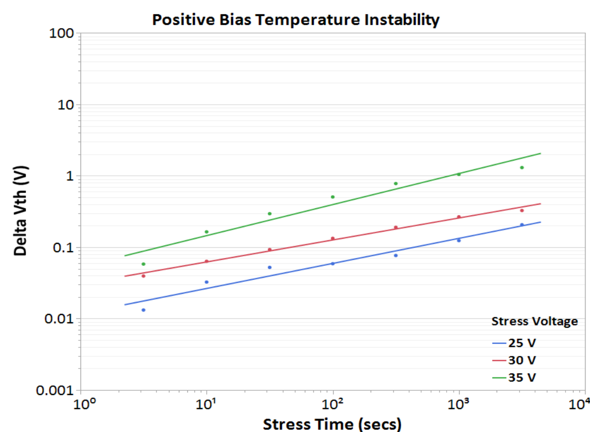

Fig. 13. 175°C PBTI results at accelerated gate voltages.

1.7.2 Negative Bias Temperature Instability (NBTI)

Negative Bias Temperature Instability (NBTI) occurs when a negative gate voltage is applied to a SiC MOSFET at elevated temperatures, often during the off-state of an n-channel device. This stress leads to the generation of acceptor-like interface states and hole trapping within the oxide, causing a negative shift in the $V_{GS,TH}$.

While traditionally associated with p-MOSFETs, NBTI-like phenomena are also observed in SiC n-MOSFETs under negative gate bias. This poses a critical reliability challenge for non-optimized SiC devices due to the specific nature of defects at the SiC/SiO_2 interface. Fig. 14 illustrates the NBTI results for Navitas' MOSFETs under high stress voltages at 175°C. The data shows that the $V_{GS,TH}$ shift remains exceptionally stable, increasing by only a few tens of millivolts after 3,000 seconds of stress.

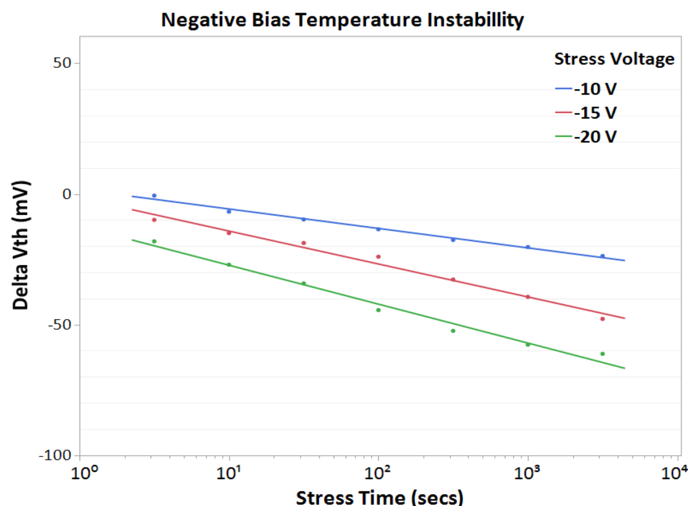

Fig. 14. 175°C NBTI results at accelerated gate voltages.

1.8 Use Case Scenarios - Lifetime Validation

Reliability testing and lifetime modeling are directly tied to the specific operating conditions and requirements of the end application. For SiC MOSFETs, lifetime validation involves tailoring reliability tests to mimic real-world stress profiles and environments. This approach leverages the performance advantages of SiC while rigorously ensuring long-term stability against gate oxide degradation mechanisms.

1.8.1 Solid State Transformer (SST) Applications: AI Data Center Power Delivery and Battery Energy Storage Systems (BESS)

Solid-state transformers (SST) are gaining traction as practical replacements for bulky line-frequency transformers in medium-voltage grid applications. These topologies typically combine an active front-end (AFE) converter with a dual active bridge (DAB) converter, featuring switching frequencies of 1–10 kHz for the hard-switched AFE stage and 50–150 kHz for the soft-switched DAB stage. SSTs are particularly demanding on SiC MOSFETs due to the combination of high blocking voltages, high junction temperatures, and duty cycles spanning several decades. Under these conditions, gate oxide stability is a critical requirement for long-term reliability.

In Battery Energy Storage System (BESS) deployments, an SST replaces the conventional inverter-plus-transformer stack, providing superior power density and end-to-end efficiency. A BESS unit operating at 120 kHz for eight hours a day over 20 years undergoes approximately 2.5 x 10^{12} total switching cycles. Throughout this period, devices endure long stretches of medium-voltage bias and significant thermal cycling. Accelerated test data, fitted to a power-law degradation model,

confirms that $V_{GS,TH}$ drift remains comfortably below 0.5 V at these cycle counts, provided the gate is driven within recommended limits.

Data center power delivery represents an even harsher environment, as systems operate continuously and face additional stress variations from dynamic AI workload profiles. The shift toward higher distribution voltages—stepping 13.8 kV or 34.5 kV AC down to 800 V DC at the rack—places SSTs in 24/7 service. Operating at 120 kHz for 15 years results in approximately 1.6 x 10^{13} switching cycles. At this scale, even a gradual $V_{GS,TH}$ creep can erode conduction loss margins and thermal headroom.

The degradation model derived from our 1,000-hour stress characterization confirms that drift stays within design limits for properly gate-driven devices. Navitas' Trench-Assisted Planar (TAP) gate architecture is central to this robustness; it distributes the electric field across the oxide more evenly than pure trench designs, directly improving breakdown margins and long-term threshold voltage stability.

1.8.2 Power Conversion System (PCS) Applications: Solar Inverter and Power Optimizer

In energy and grid infrastructure applications, such as solar inverters and power optimizers, Power Conversion Systems (PCS) must withstand harsh outdoor environments for decades—typically 15 to 25 years. These systems endure significant daily and seasonal temperature swings, high humidity, and frequent power fluctuations. To maximize conversion efficiency, these systems increasingly utilize SiC MOSFETs, making the long-term stability of the semiconductor under prolonged thermal and electrical loads paramount to economic viability.

Applications operating at high switching frequencies (e.g., 100 kHz) for over 20 years present a unique challenge for reliability testing. A true End-of-Life (EoL) test would require prohibitively long durations, even when using an accelerated stress frequency of 500 kHz. To overcome this, an extrapolation method is used to predict EoL performance:

- **Test Duration:** An accelerated 1,000-hour stress test is conducted with intermediate readouts of critical device parameters.
- **Extrapolation:** A power-law-based fitting is applied to extrapolate the $V_{GS,TH}$ shift according to the specific application mission profile and lifetime requirements.

As shown in Fig. 15, this fitted power law allows for the calculation of the $V_{GS,TH}$ shift for any application, provided the typical switching frequency and total operational time are known. For a typical solar inverter operating 12 hours per day over 20 years at a switching frequency of 100 kHz, the total number of switching cycles is approximately 3.15 x 10^{13} (as indicated in Fig. 15).

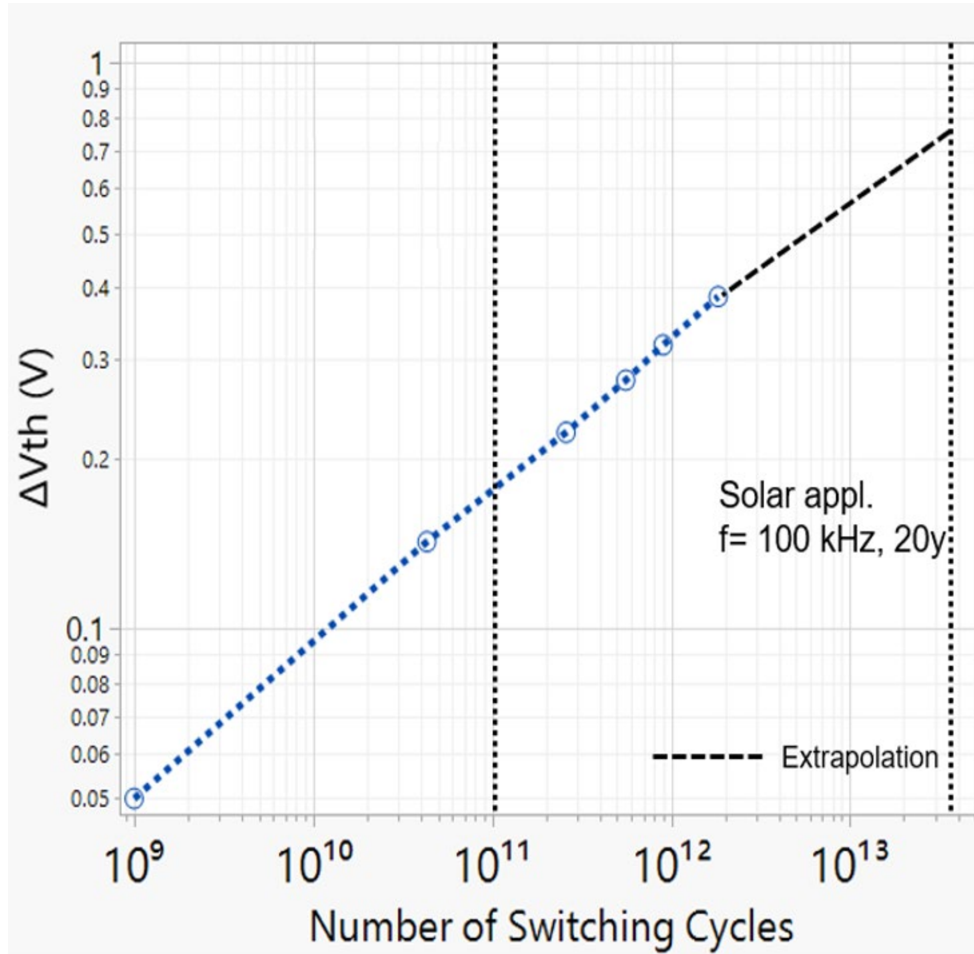

Fig. 15. ΔV_{TH} drift as a function of switching cycles in Navitas's SiC MOSFETS.

Extrapolation of the measurement data suggests a maximum $V_{GS,TH}$ shift of up to 0.7 V. This is considered a realistic, conservative estimate, as it assumes the power-law degradation factor remains constant and does not decelerate beyond the initial 1,000 hours of stress.

1.9 Conclusion

The SiC/SiO_2 interface in SiC MOSFETs typically exhibits a higher density of interface traps compared to the Si/SiO_2 interface in traditional Si MOSFETs. In non-optimized process architectures, this elevated trap density can lead to significant reliability challenges, such as Time-Dependent Dielectric Breakdown (TDDB) and Bias Temperature Instability (BTI). These

phenomena directly affect gate threshold voltage ($V_{GS,TH}$) stability and the long-term integrity of the gate oxide.

To accurately model and mitigate these concerns, this white paper has detailed a comprehensive suite of DC and AC stress tests—including high, low, and room-temperature gate bias and switching evaluations—alongside rigorous TDDB and BTI characterization. These models enable precise lifetime predictions for gate oxides in high-stress, mission-critical applications, such as Solid-State Transformers (SST) and Power Conversion Systems (PCS).

Navitas' robust qualification methodology and proven performance demonstrate that its SiC MOSFETs reliably deliver the advantages of high efficiency and stable operation required for demanding AI data centers, grid infrastructure, and energy applications.

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