中国电源学会第二十三届学术年会
The 23rd China Power Supply Society Conference (CPSSC'2019)
2019年11月1日至4日
地点：深圳

Navitas

Let's go GaNFast™

基于氮化镓IC的150W高效率高功率密度适配器设计

150W PFC+LLC using GaNFast Power ICs

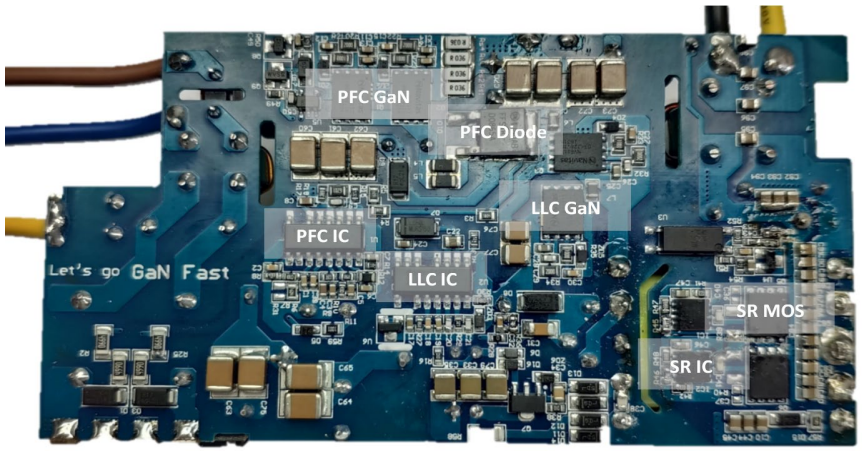
Wenhang.lu, AE, wenhang.lu@navitassemi.com

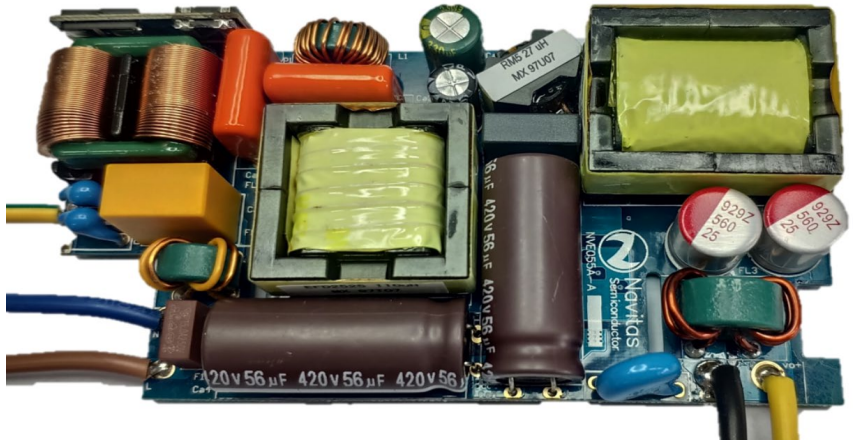
Agenda

- Appearance Review
- Test Result Review
- Key Waveform
- Controller Selection
- Layout notes
- GaN vs. Si (CoolMOS)

150W/19V adaptor

尺寸	Dimensions		103 x 55 x 17	mm
			96.3	cc
功率密度	Power Density	(uncased)	1.56	W/cc
			25.6	W/in^3
效率	Efficiency (full load)	230 V_{AC}	95.2	%
		115 V_{AC}	94.5	%
	Efficiency (4–pt. ave.)	230 V_{AC}	95.5	%
		115 V_{AC}	93.9	%





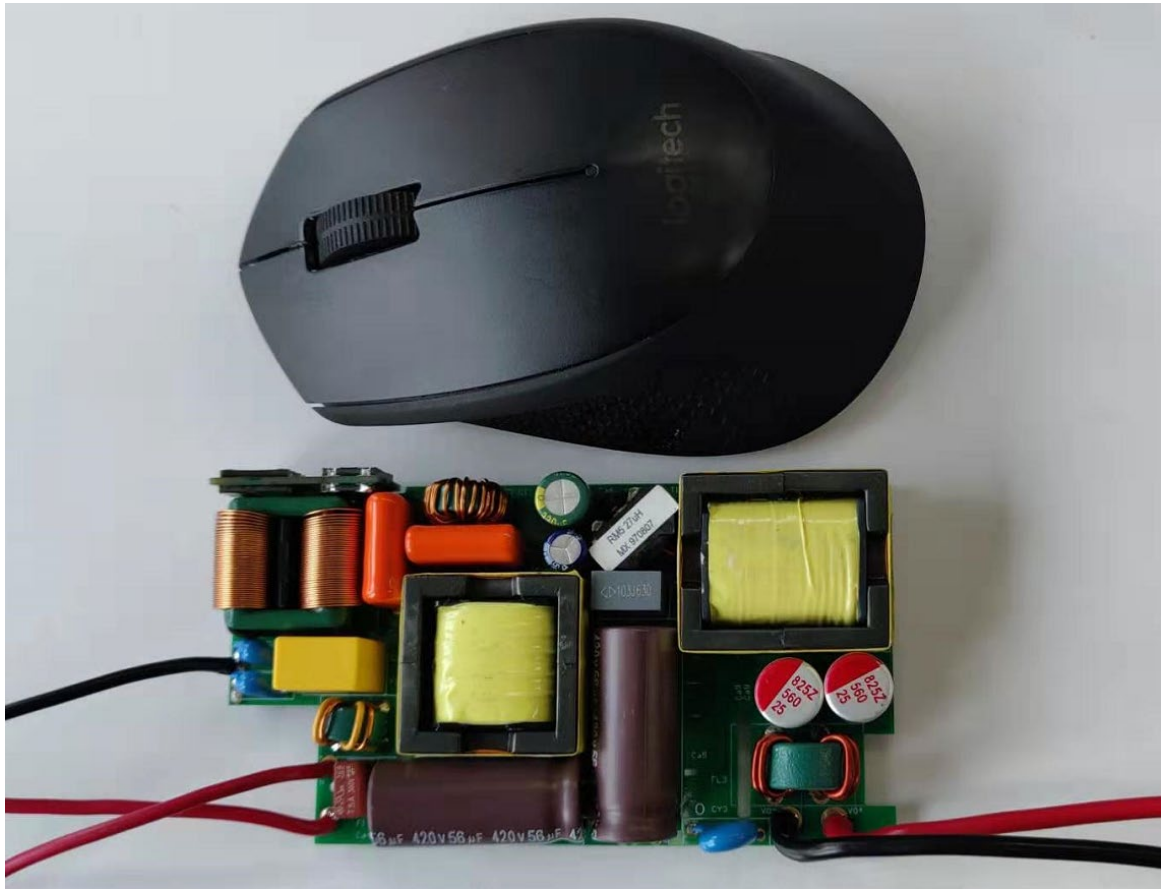
40% Size Reduction

HP 65W Adaptor

HP 65W Adaptor

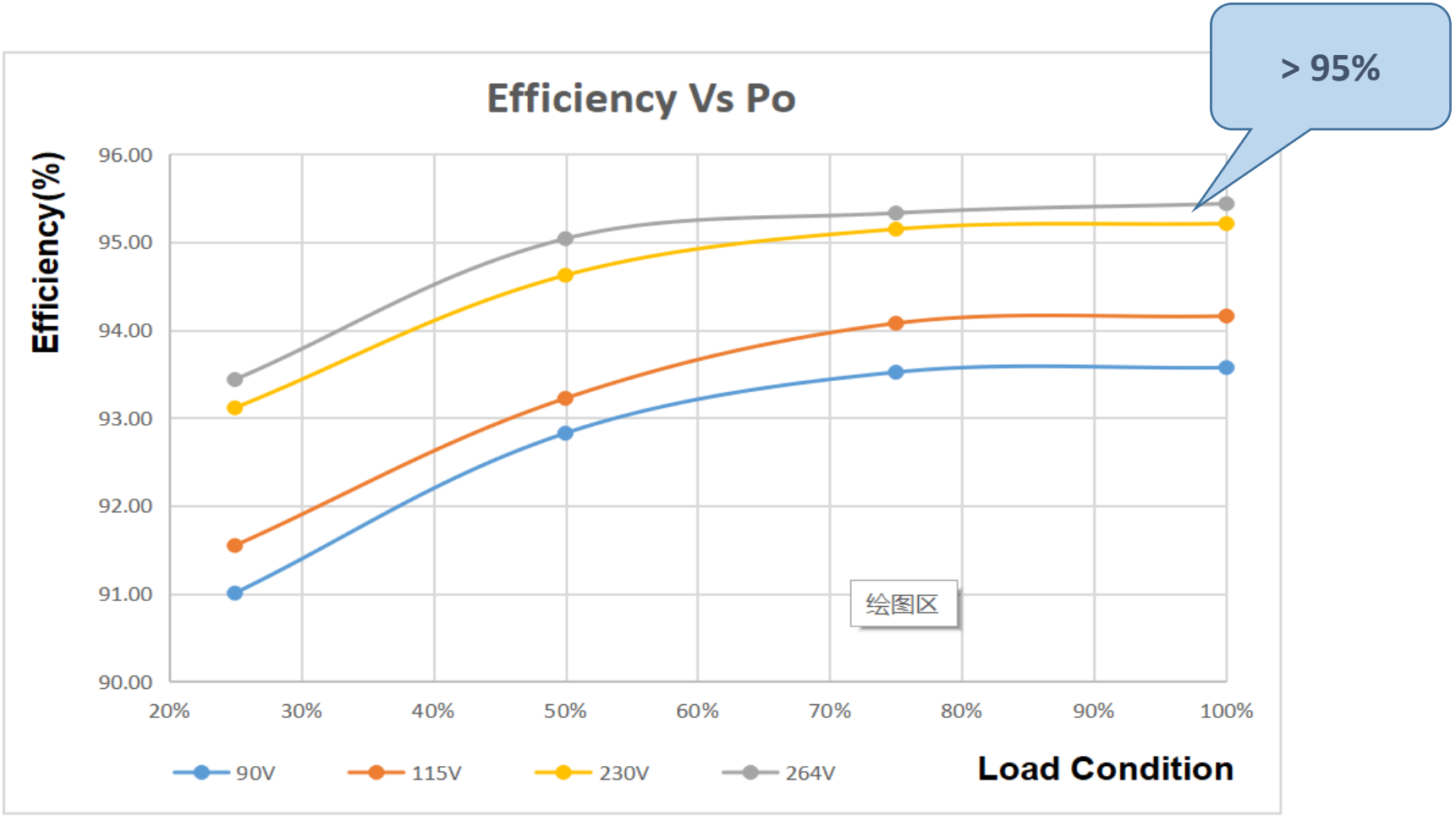
High Power-Density PCBA (96 cc)= 103 x 55 x 17mm

HP mouse



小米8

High Efficiency >93.5% @ 90 V_{AC}，Full Load



150W Thermal

- Test condition: Ambient Temp: 30 degree C ;
- full load Io=7.8A

P1:	PFC IC	——	80℃
P2:	LLC IC	——	82℃
P3:	PFC GaN	——	84℃
P4:	PFC CS	——	84℃
P5:	PFC Diode	——	86℃
P6:	LLC GaN	——	85℃
P7:	SR IC	——	85℃
P8:	SR MOS	——	90℃

150W Thermal

- Test condition: Ambient Temp: 30 degree C ;
- full load Io=7.8A

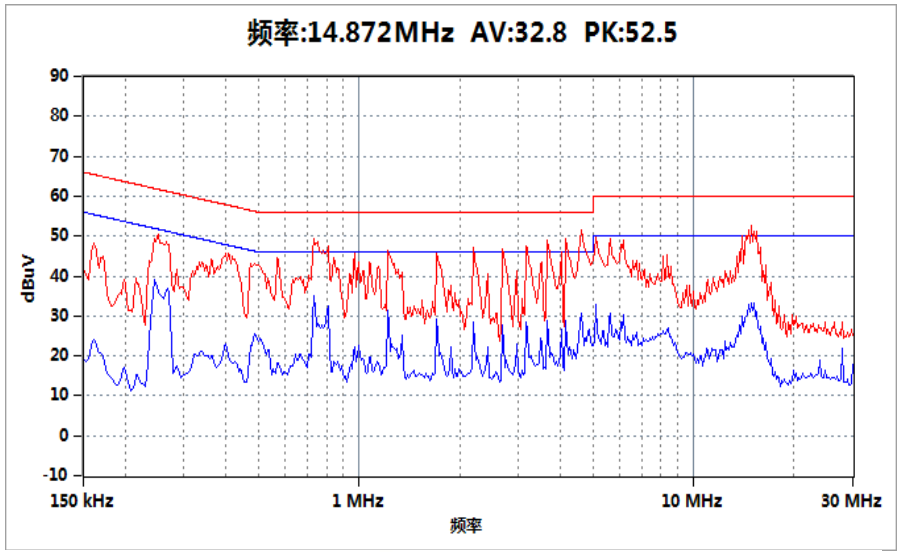
P1:	CMC	——82℃
P2:	Bridge	——117℃
P3:	DMC	——78℃
P4:	Inductor	——92℃
P5:	BUS E-CAP	——76℃
P6:	Resonant Inductor	——79℃
P7:	Transformer	——88℃
P8:	Secondary E-CAP	——65℃

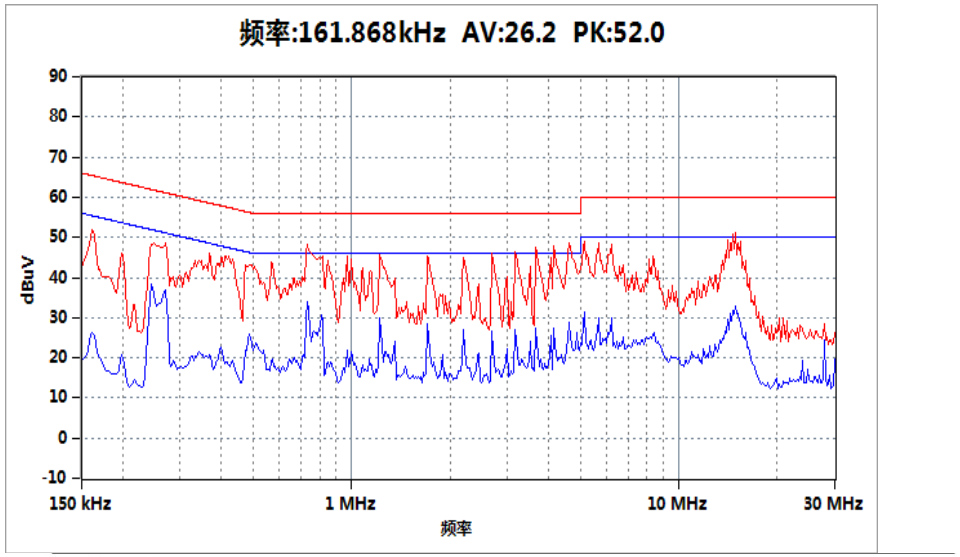
150W Thermal

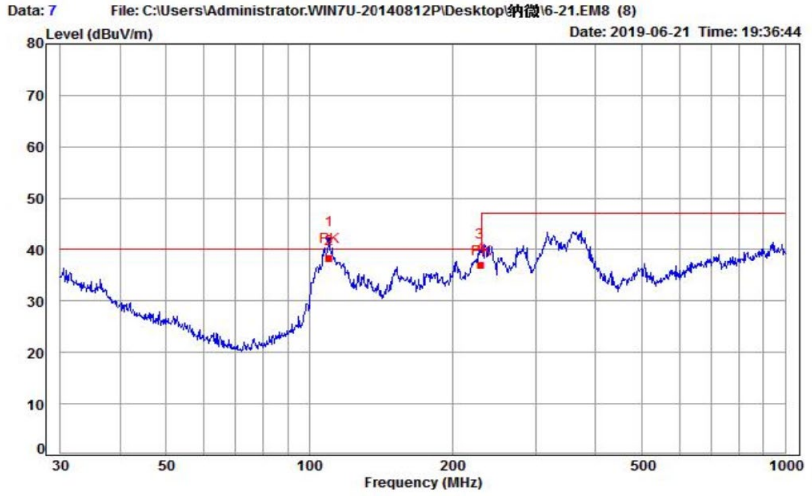
- Test condition: Ambient Temp: 30 degree C ;
- full load Io=7.8A

Test Conditions	Bridge	PFC GAN	LLC GAN	PFC diode	Inductor	Transformer	Resonant Inductor	BUS E-CAP	Secondray E-CAP	SR MOS
Vin=90Vac	117	84	85	86	92	88	79	76	65	**90**

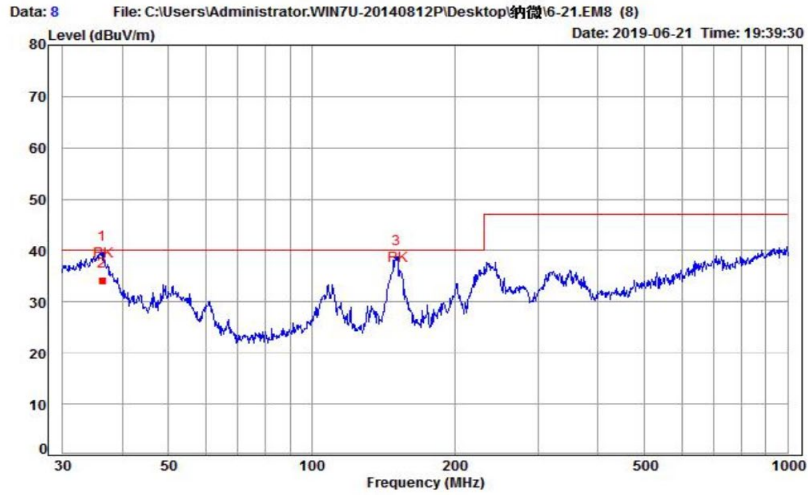
150W EMC





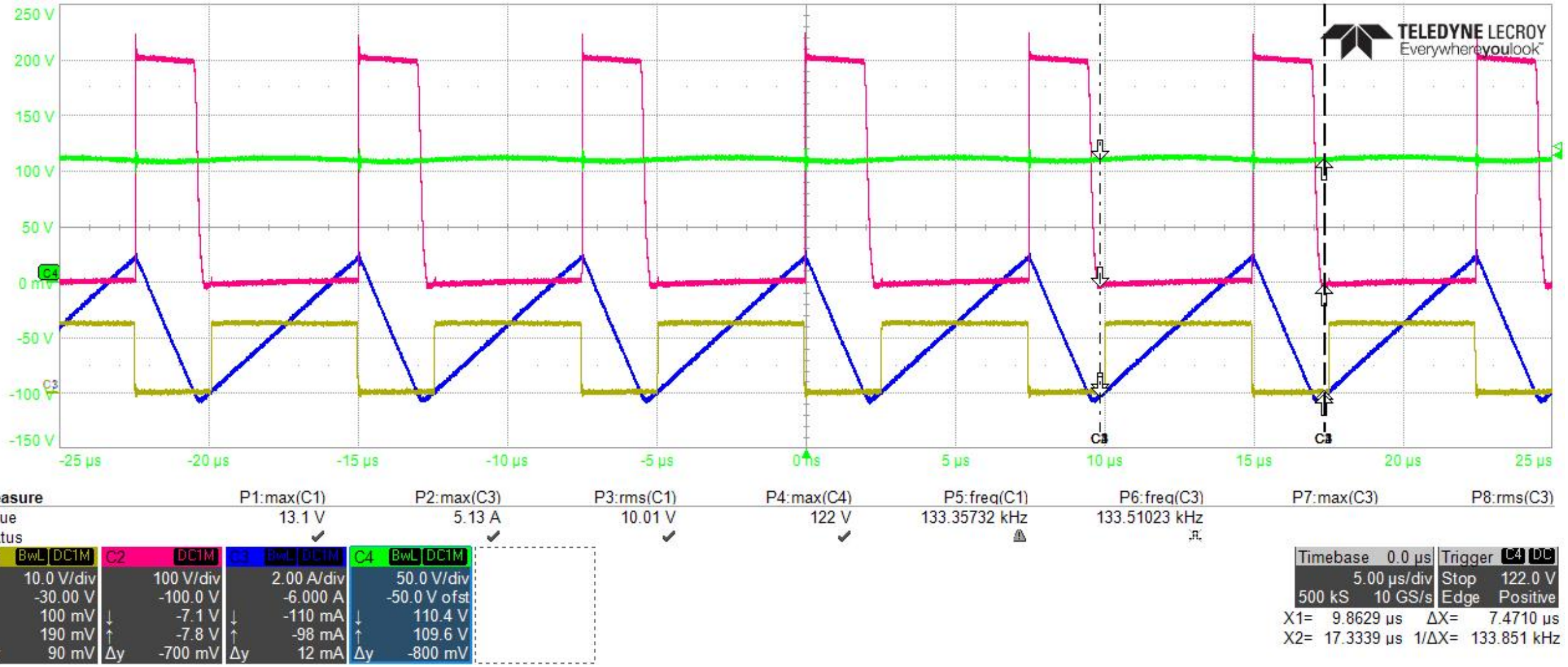


Condition :
EUT : 150W-pinbi-115V-H
Power : AC 115V/50Hz
Env. : 23.5℃ , 49%RH , 100.2KPa



Condition :
EUT : 150W-pinbi-115V-V
Power : AC 115V/50Hz
Env. : 23.5℃ , 49%RH , 100.2KPa

Key Waveform， PFC



Measure	P1:max(C1)	P2:max(C3)	P3:rms(C1)	P4:max(C4)	P5:freq(C1)	P6:freq(C3)	P7:max(C3)	P8:rms(C3)
value	13.1 V	5.13 A	10.01 V	122 V	133.35732 kHz	133.51023 kHz		
status	✔	✔	✔	✔	⚠	⚠		

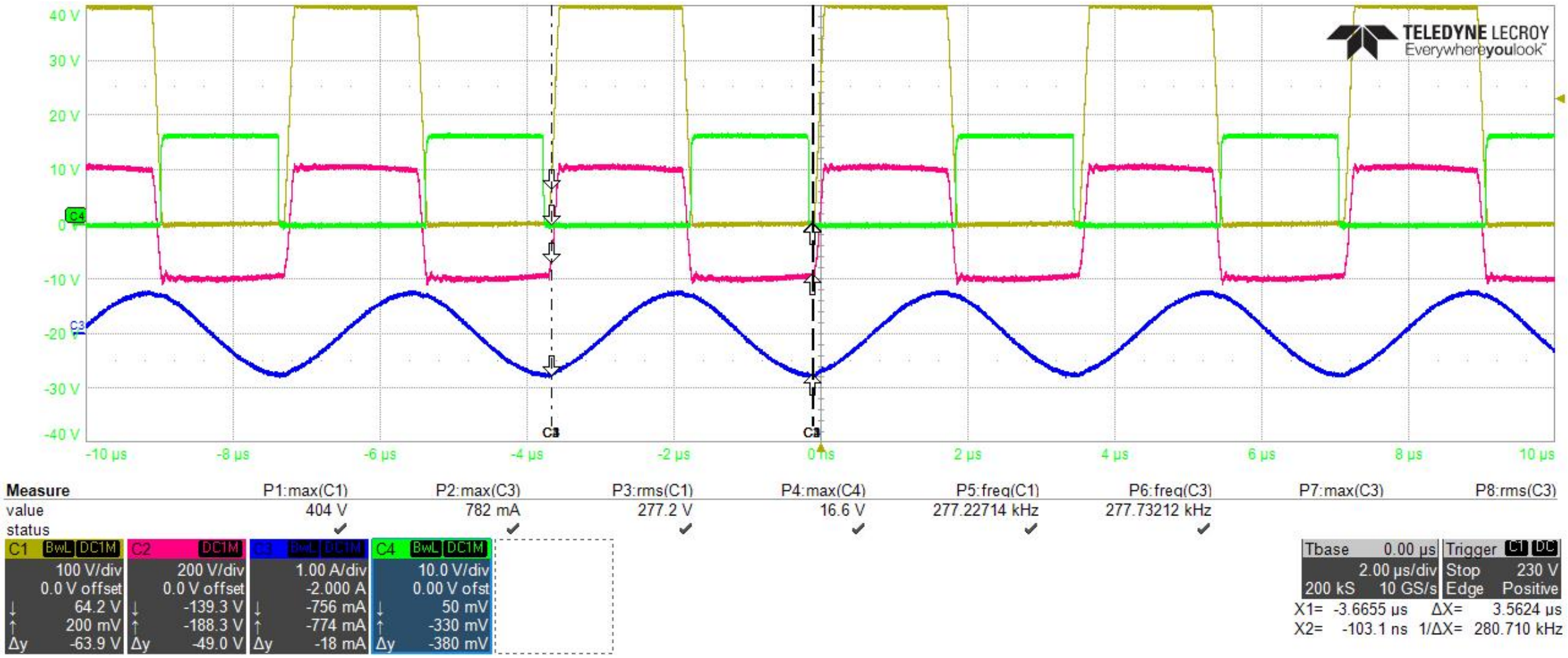
C1 BwL DC1M	C2 DC1M	C3 BwL DC1M	C4 BwL DC1M
10.0 V/div	100 V/div	2.00 A/div	50.0 V/div
-30.00 V	-100.0 V	-6.000 A	-50.0 V ofst
↓ 100 mV	↓ -7.1 V	↓ -110 mA	↓ 110.4 V
↑ 190 mV	↑ -7.8 V	↑ -98 mA	↑ 109.6 V
Δy 90 mV	Δy -700 mV	Δy 12 mA	Δy -800 mV

Timebase 0.0 µs	Trigger C4 DC
5.00 µs/div	Stop 122.0 V
500 kS 10 GS/s	Edge Positive

X1= 9.8629 µs ΔX= 7.4710 µs
X2= 17.3339 µs 1/ΔX= 133.851 kHz

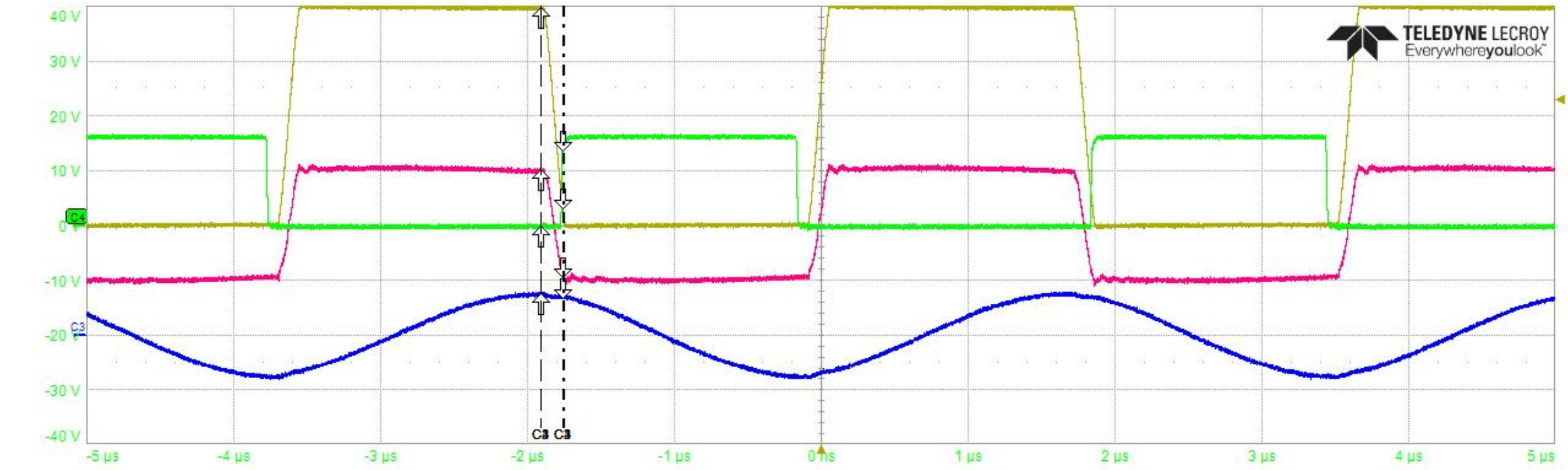
1：PFC DRIVER 2：PFC MOS VDS 3：PFC IL 4：VOLTAGE AFTER BRIDGE

Key Waveform, LLC



1：LLC SW 2：VTP 3：IR 4：DRIVER

Key Waveform, LLC



Measure	P1:max(C1)	P2:max(C3)	P3:rms(C1)	P4:max(C4)	P5:freq(C1)	P6:freq(C3)	P7:max(C3)	P8:rms(C3)
value	404 V	774 mA	278.1 V	16.5 V	277.27550 kHz	276.90159 kHz		
status	✔	✔	✔	✔	✔	✔		

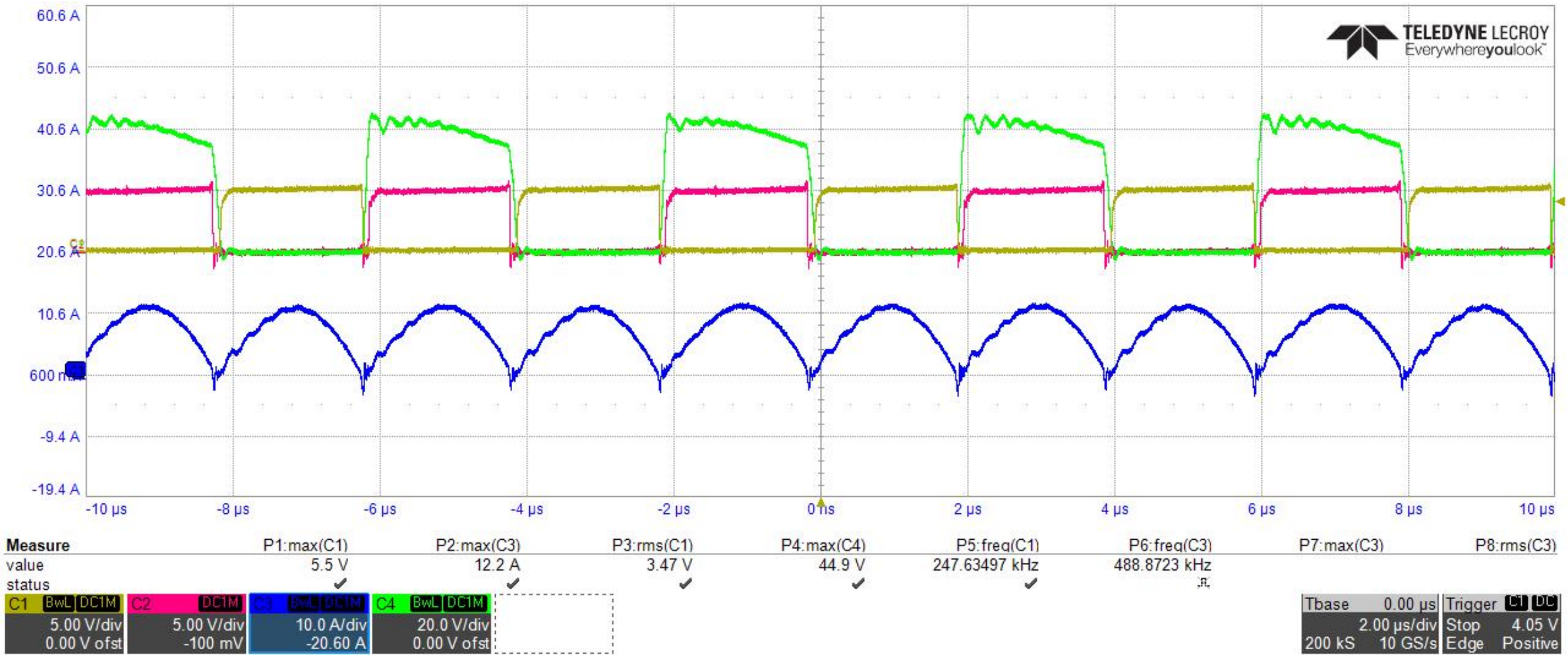
C1 BwL DC1M	C2 DC1M	C3 BwL DC1M	C4 BwL DC1M
100 V/div	200 V/div	1.00 A/div	10.0 V/div
0.0 V offset	0.0 V offset	-2.000 A	0.00 V ofst
↓ 31.7 V	↓ -187.5 V	↓ 681 mA	↓ 13.72 V
↑ 393.5 V	↑ 196.6 V	↑ 726 mA	↑ -470 mV
Δy 361.9 V	Δy 384.1 V	Δy 44 mA	Δy -14.19 V

Tbase 0.00 µs	Trigger C1 DC
1.00 µs/div	Stop 230 V
100 kS 10 GS/s	Edge Positive

X1= -1.7568 µs ΔX= -151.4 ns
X2= -1.9082 µs 1/ΔX= -6.605 MHz

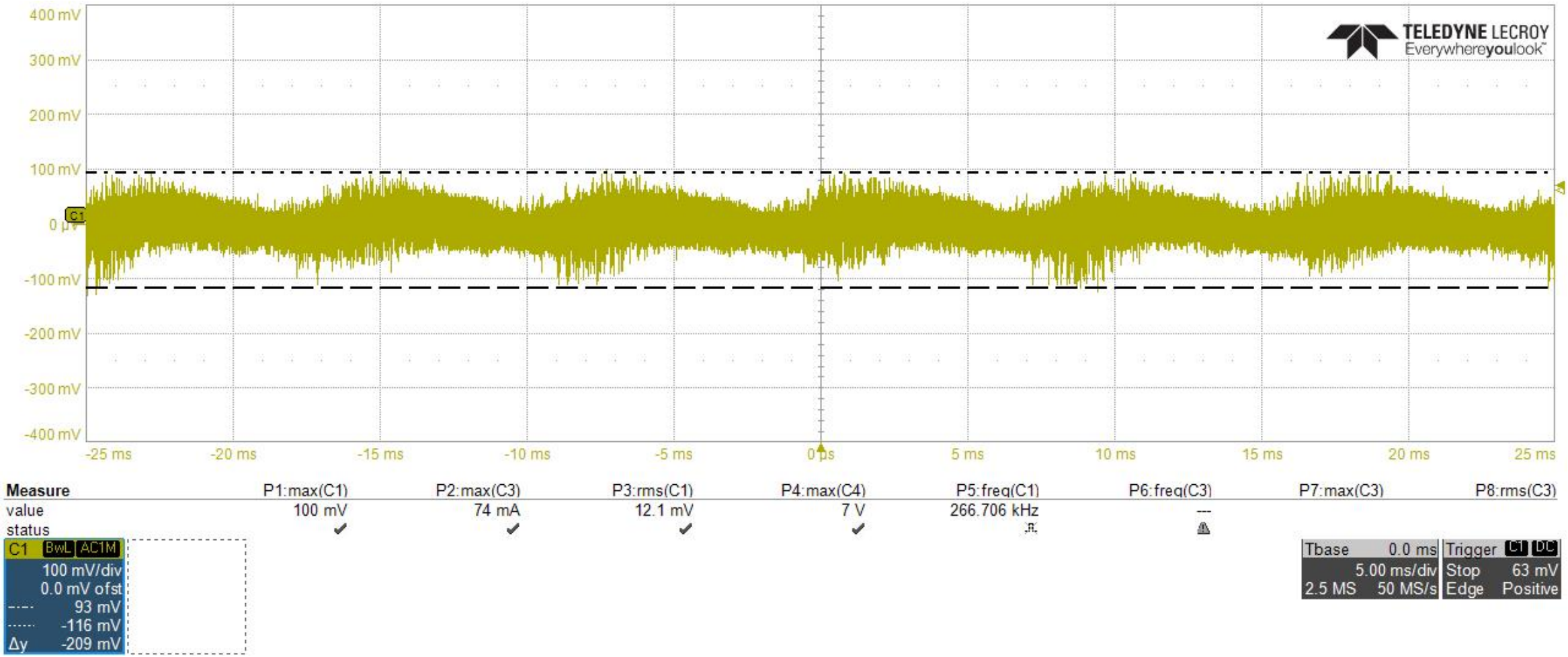
1：LLC SW 2：VTP 3：IR 4：DRIVER

Key Waveform, SR



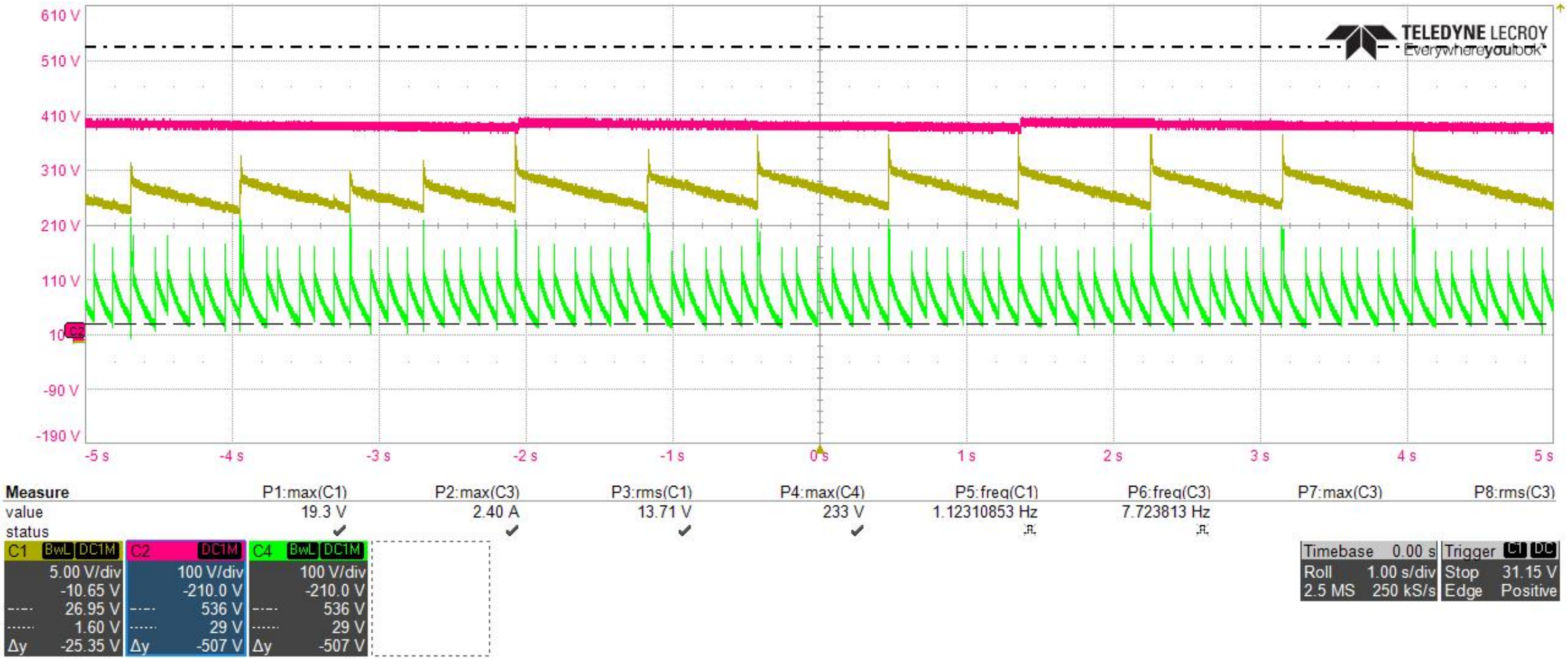
1：H-DRIVER 2：LOW-DRIVER 3：I 4：VDS

Key Waveform, Ripple



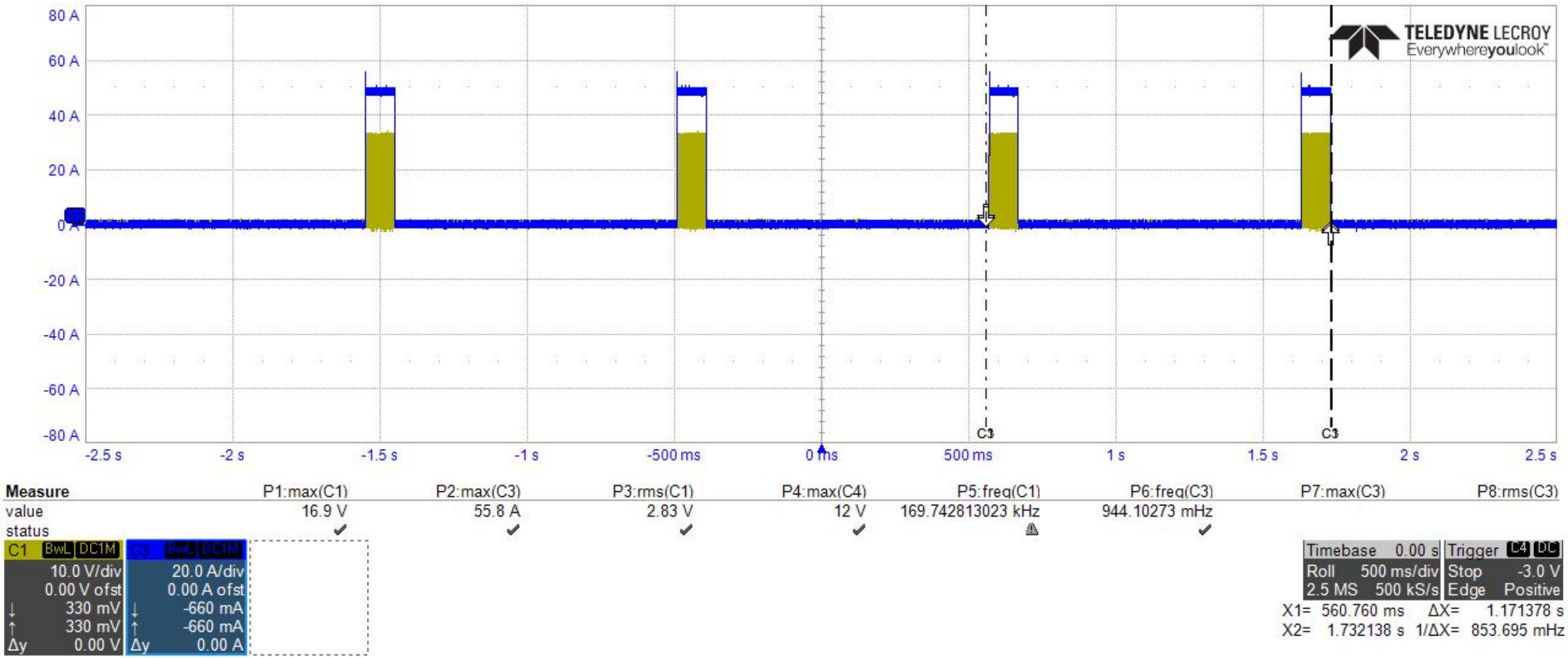
1：VO

Key Waveform, Standby



1：VCC 2：VBUS 3：VC

Key Waveform, SCP

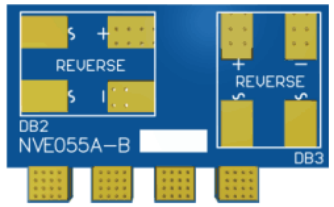


1：LLC DRIVER 2：IO

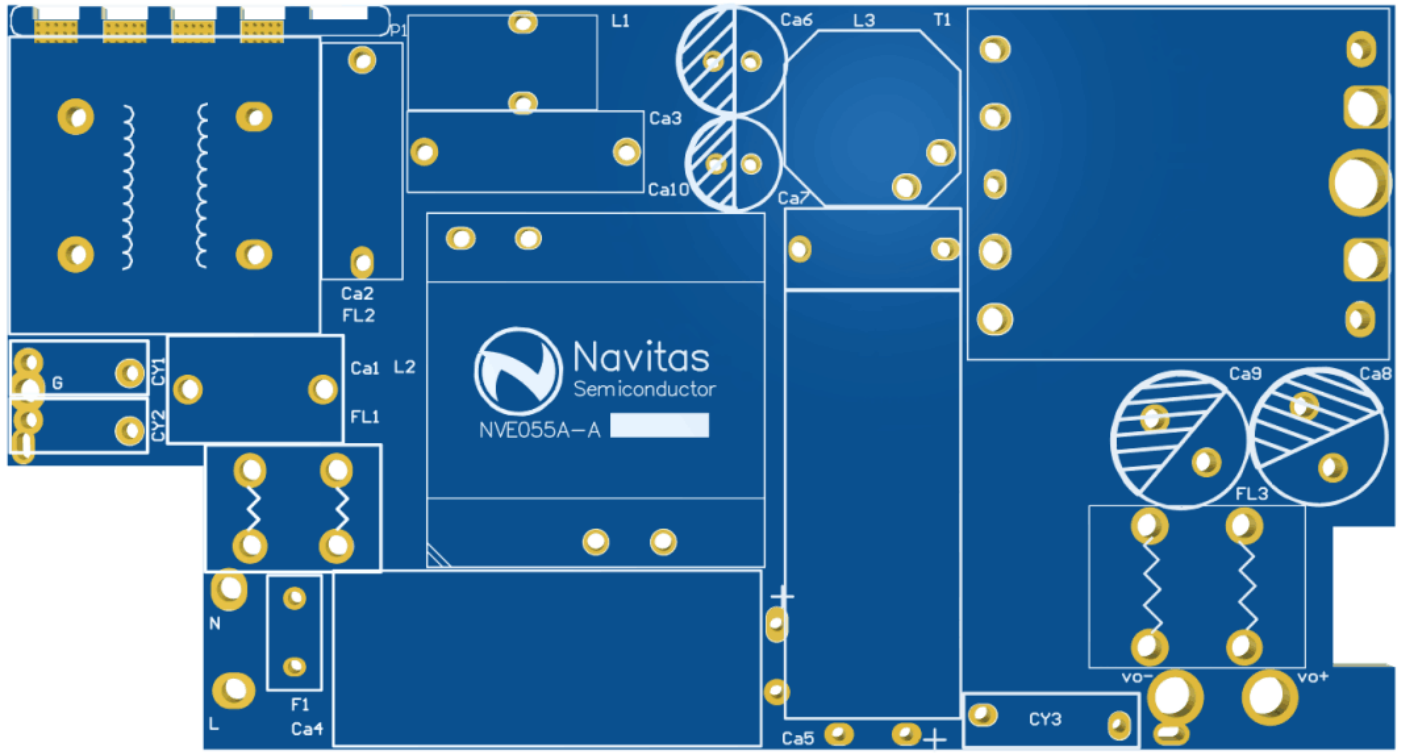
Easy-to-Build

- 2 PCBs

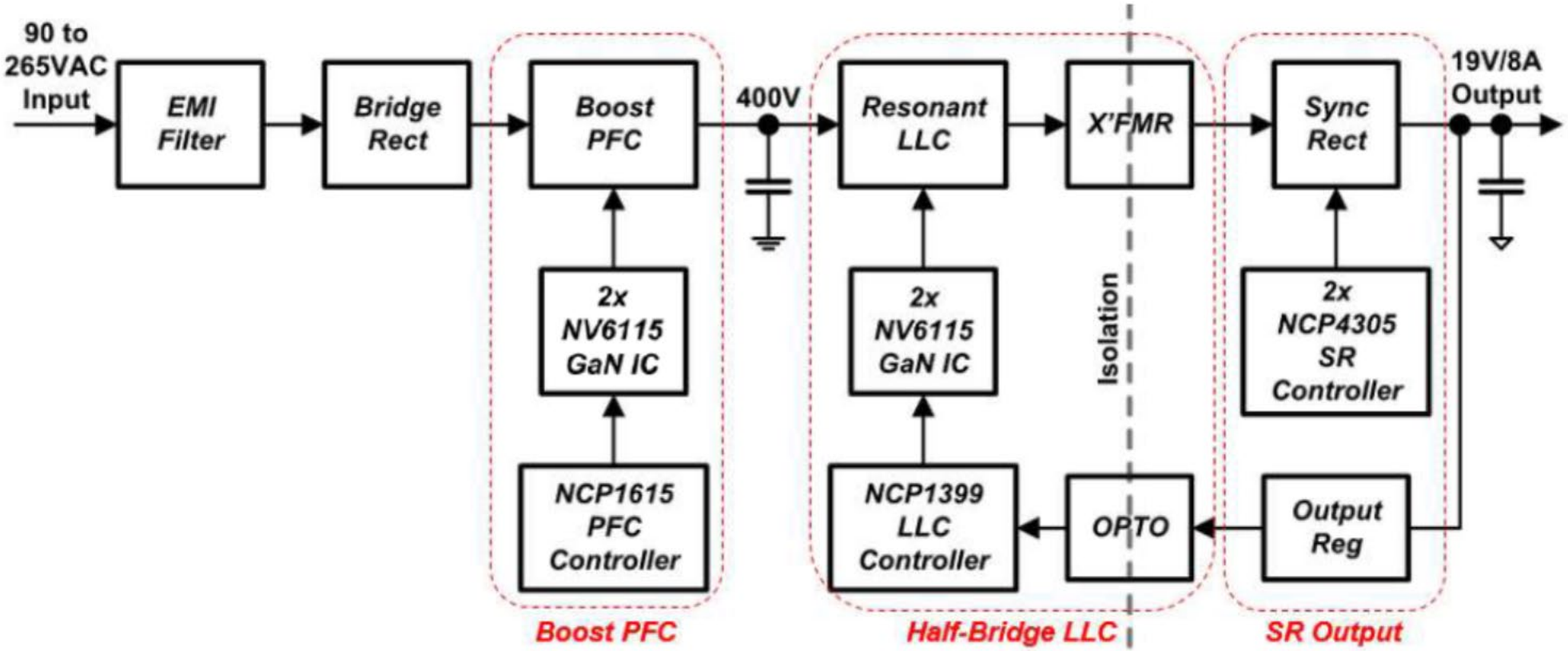
AC Bridge



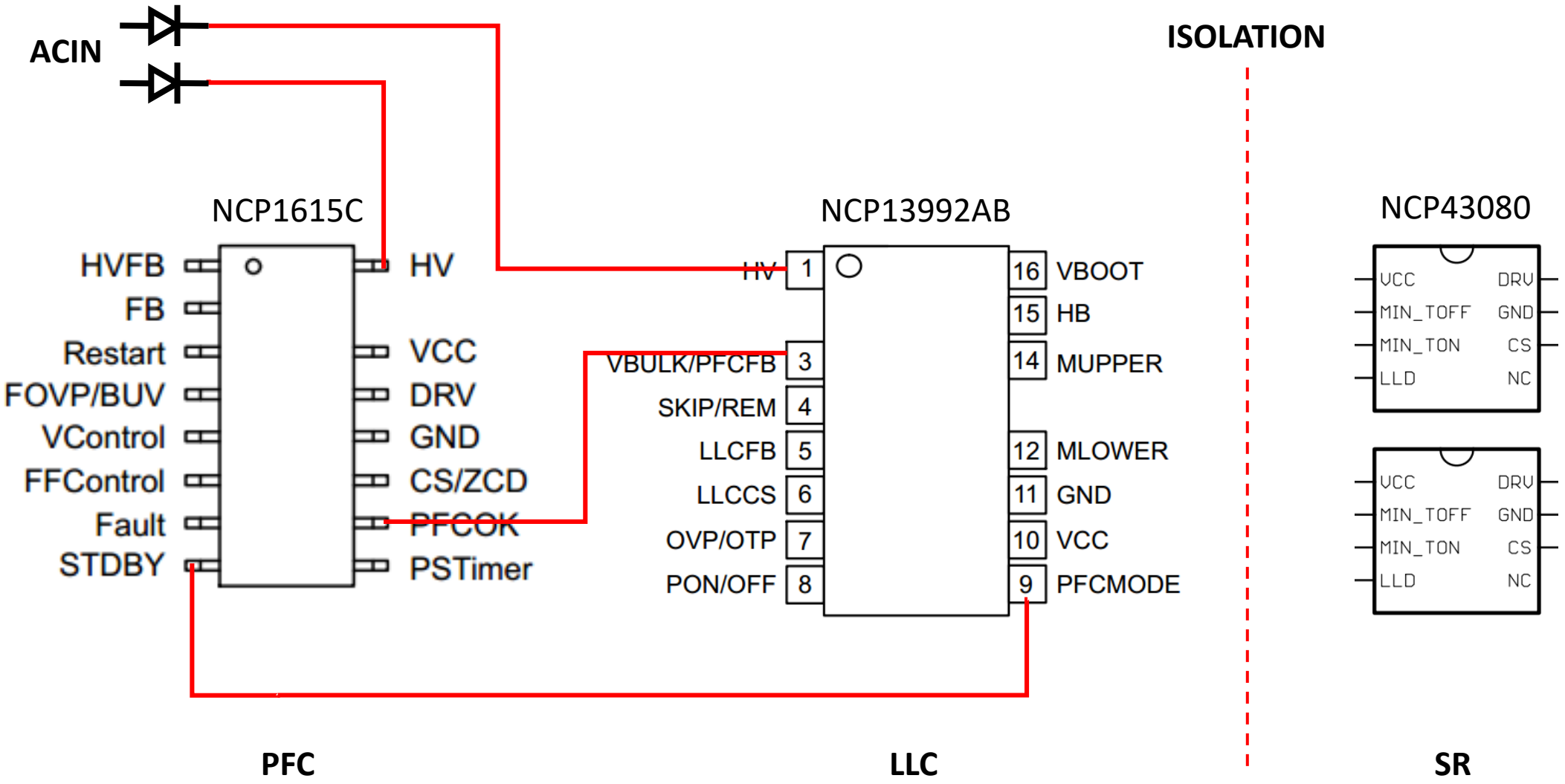
Main board



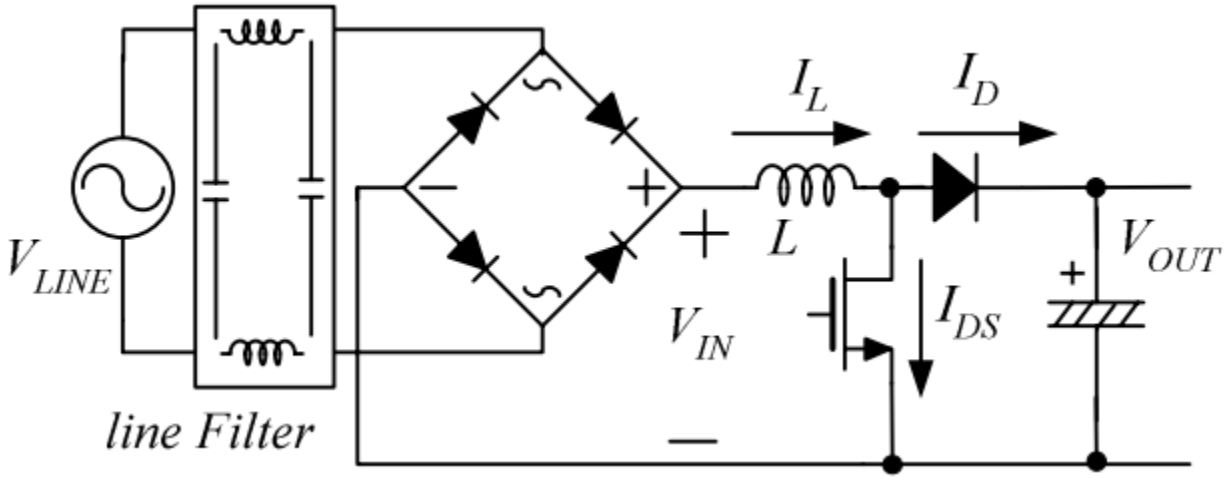
Schematic Architecture

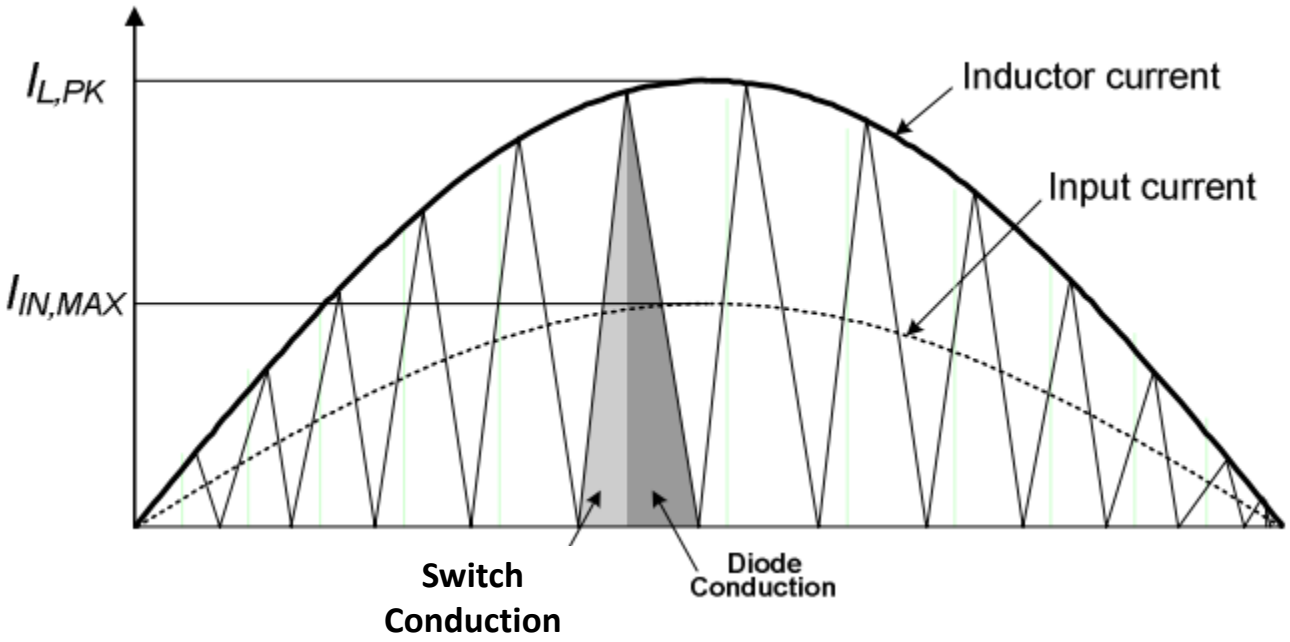


ON Semi PFC/LLC/SR Chip Set

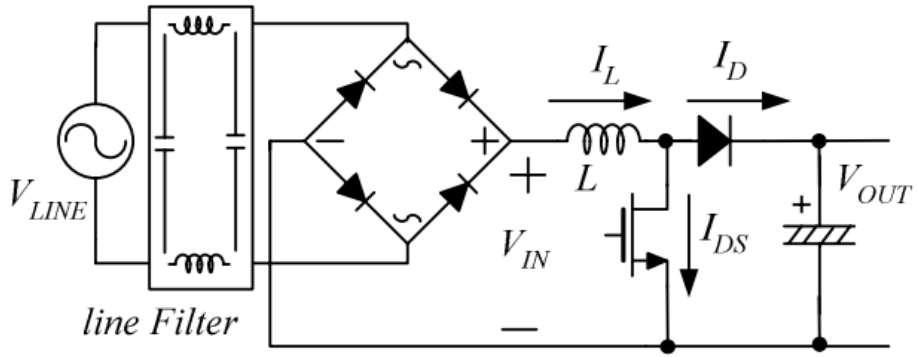


Boost PFC Circuit

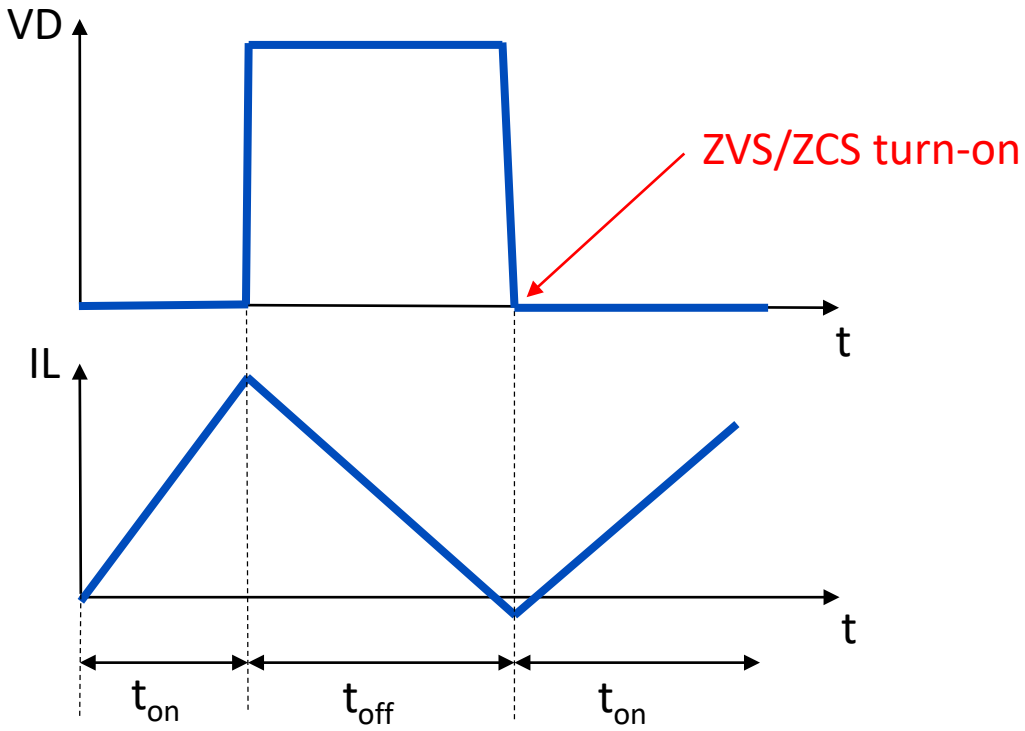




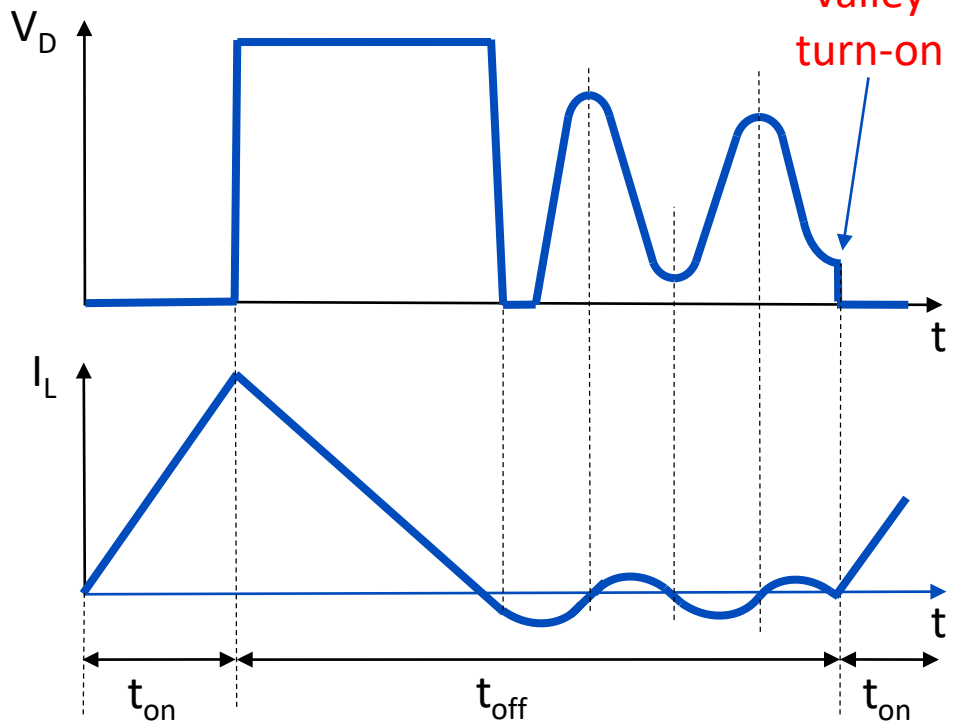
Boost PFC Circuit Modes



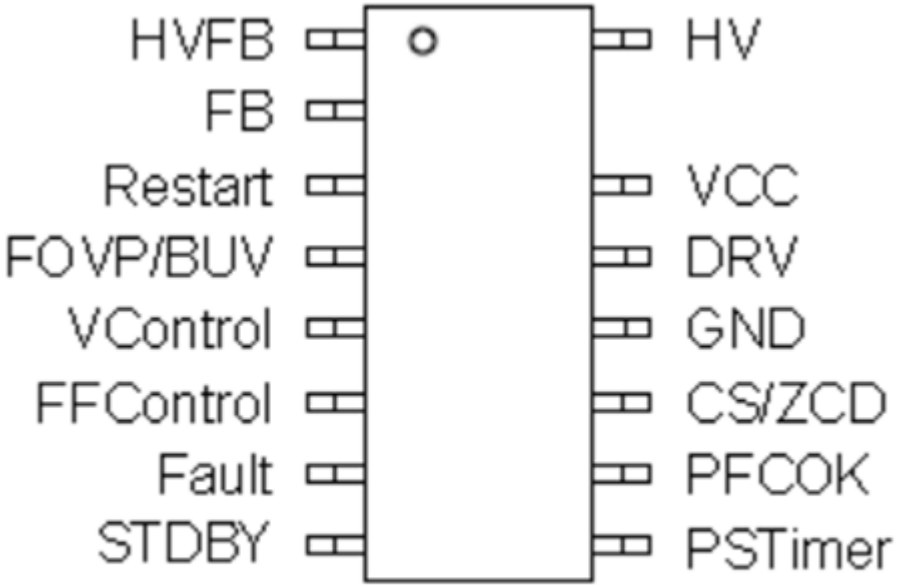
CrCM (BCM) Mode



DCM Mode

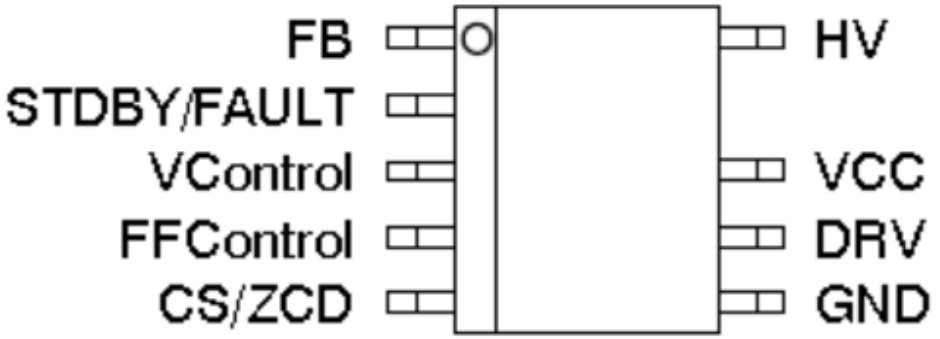


PFC: F_{SW}(MIN) = 200 kHz



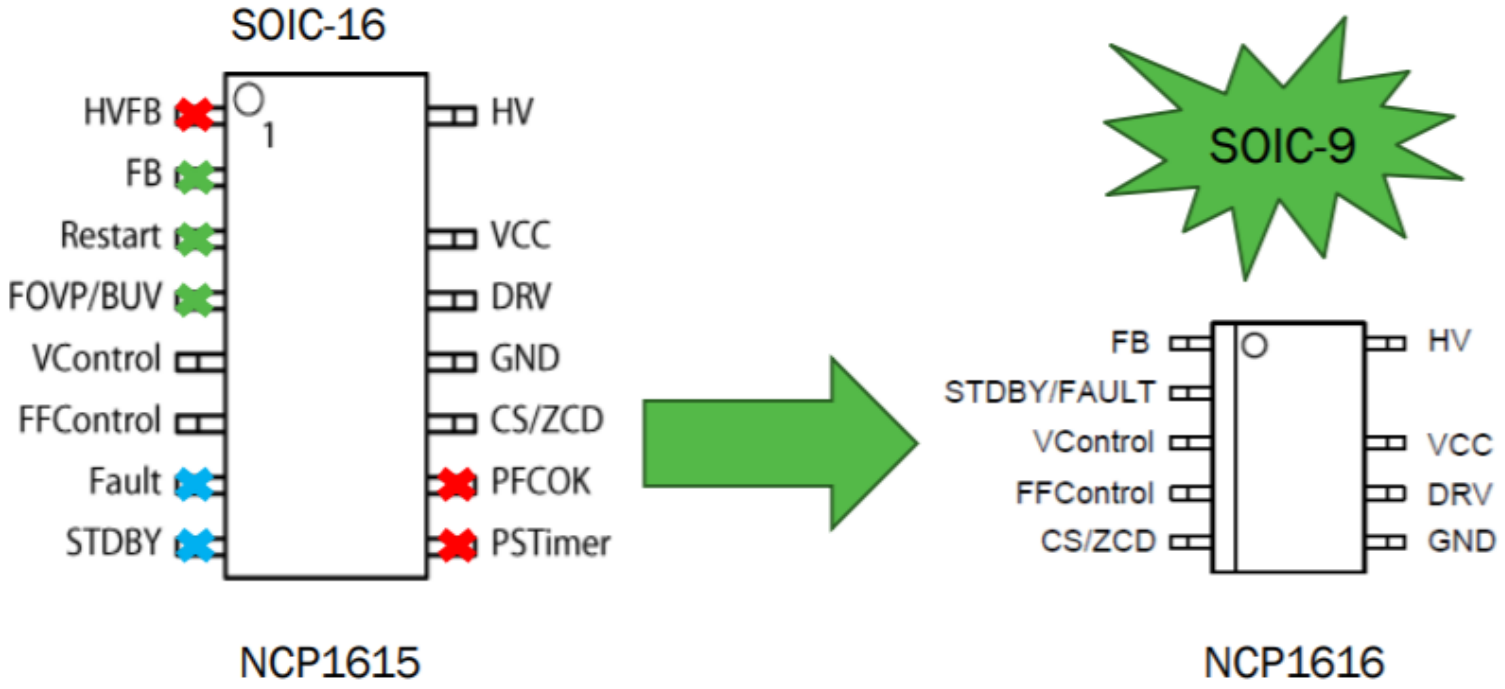
NCP1615 16 Pins (Top View)

PIN CONNECTIONS



NCP1616 9 Pins (Top View)

NCP1615 → NCP1616



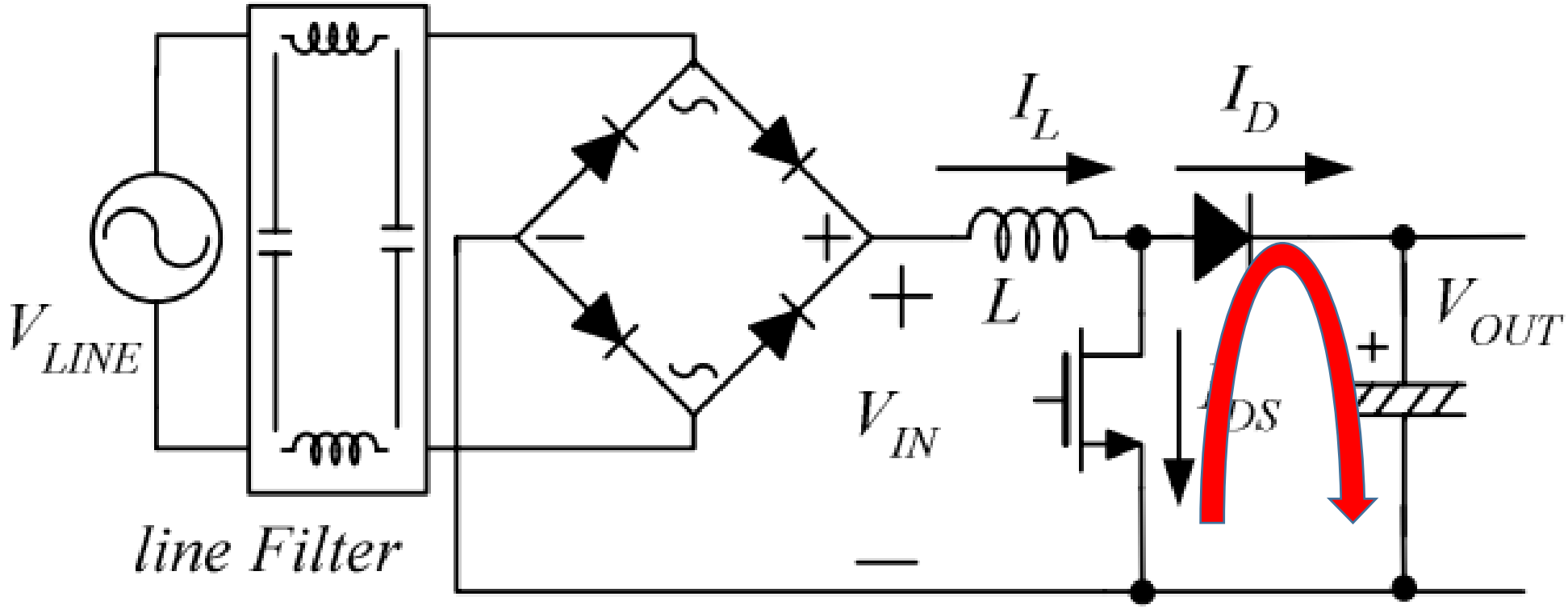
✖ Pins removed

✖ Pins combined

✖ Pins combined

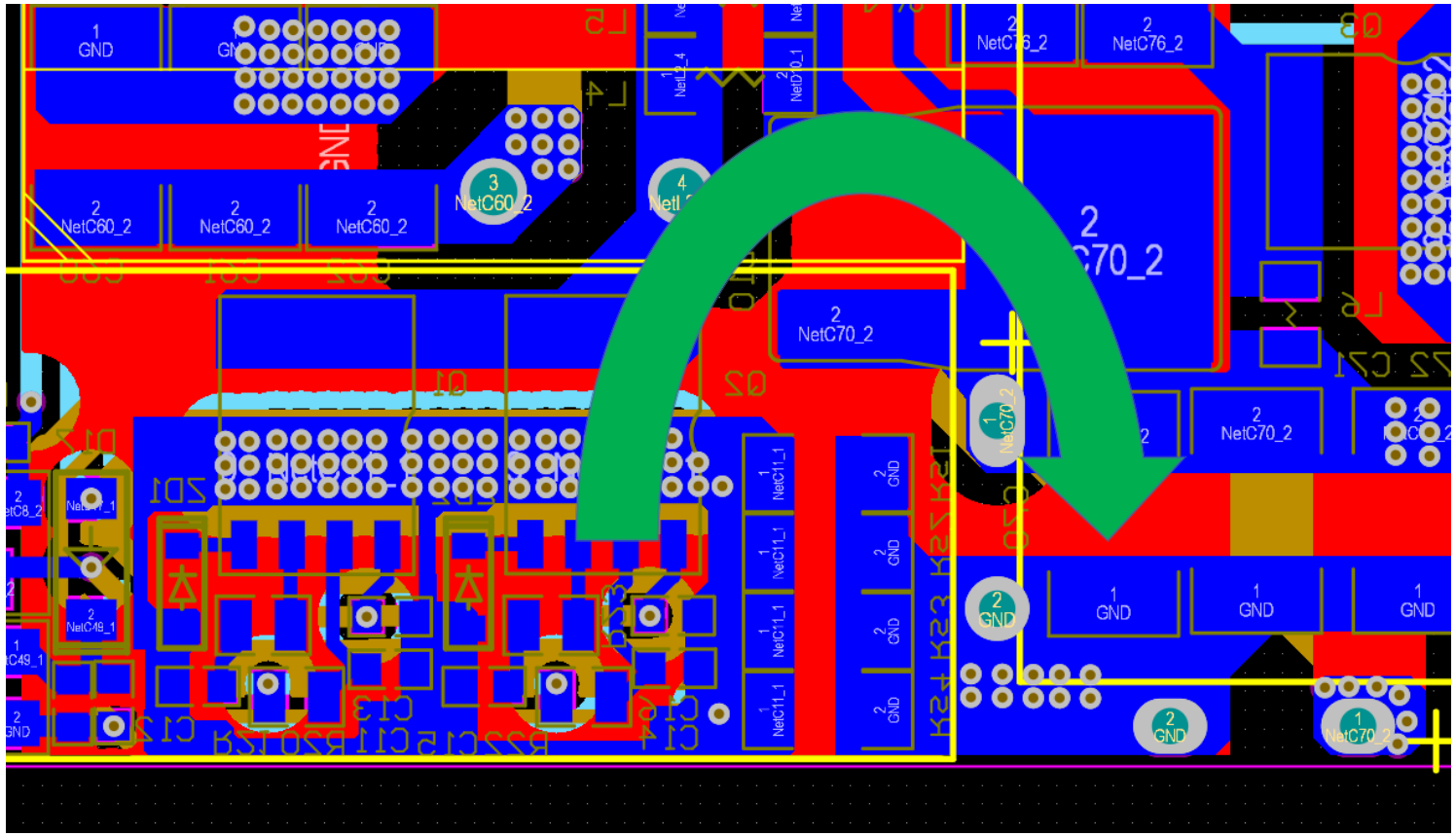
- Current controlled frequency foldback (CCFF) scheme for high efficiency across line and load.
- Integrated high voltage start-up.

Layout Guideline



- When the FET is turned off, the current transferred into the diode instantly, which creates huge di/dt, so the loop must be minimized.

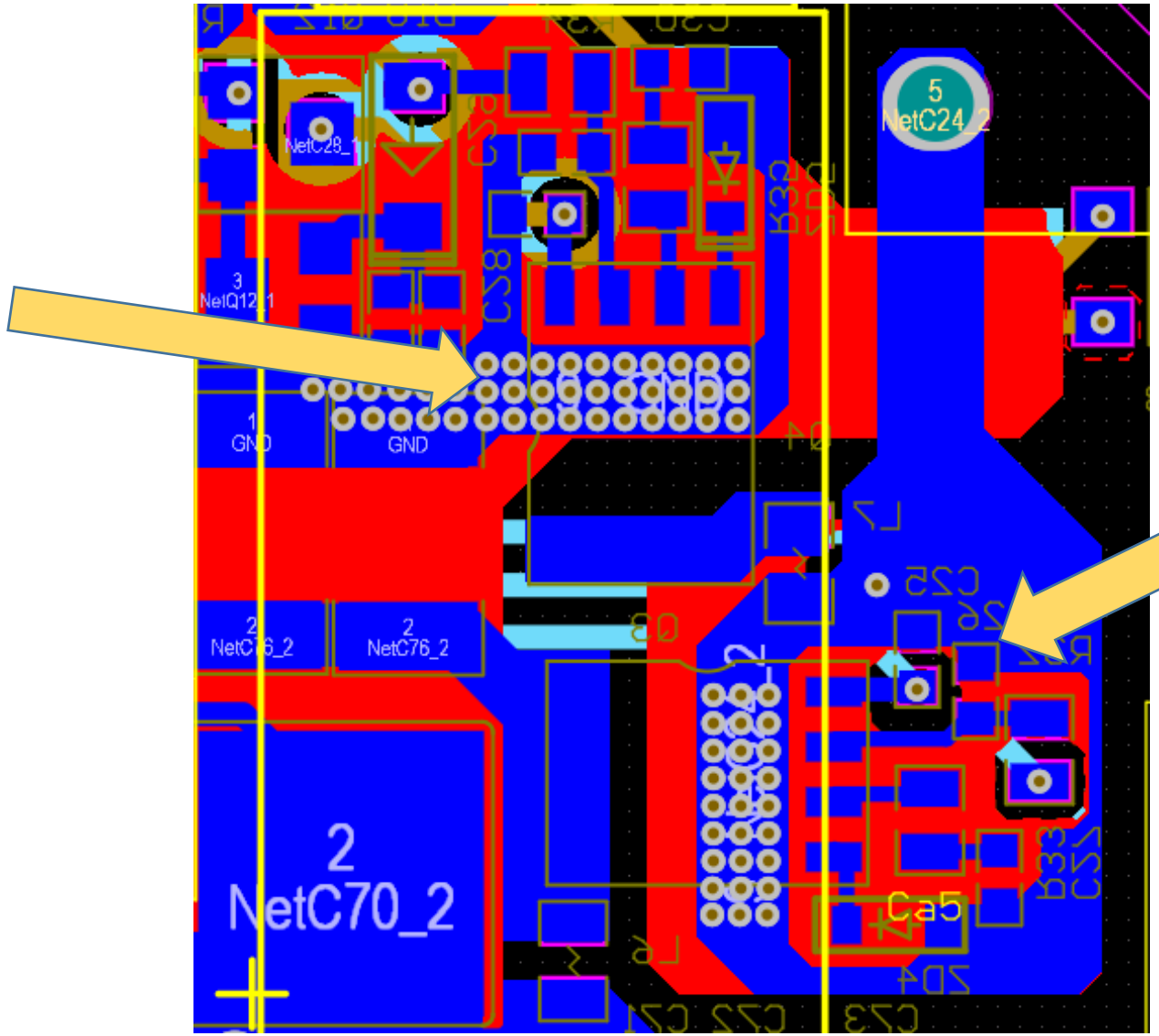
Layout Guideline



- When the FET is turned off, the current transferred into the diode instantly, which creates huge di/dt, so the loop must be minimized.

Layout Guideline

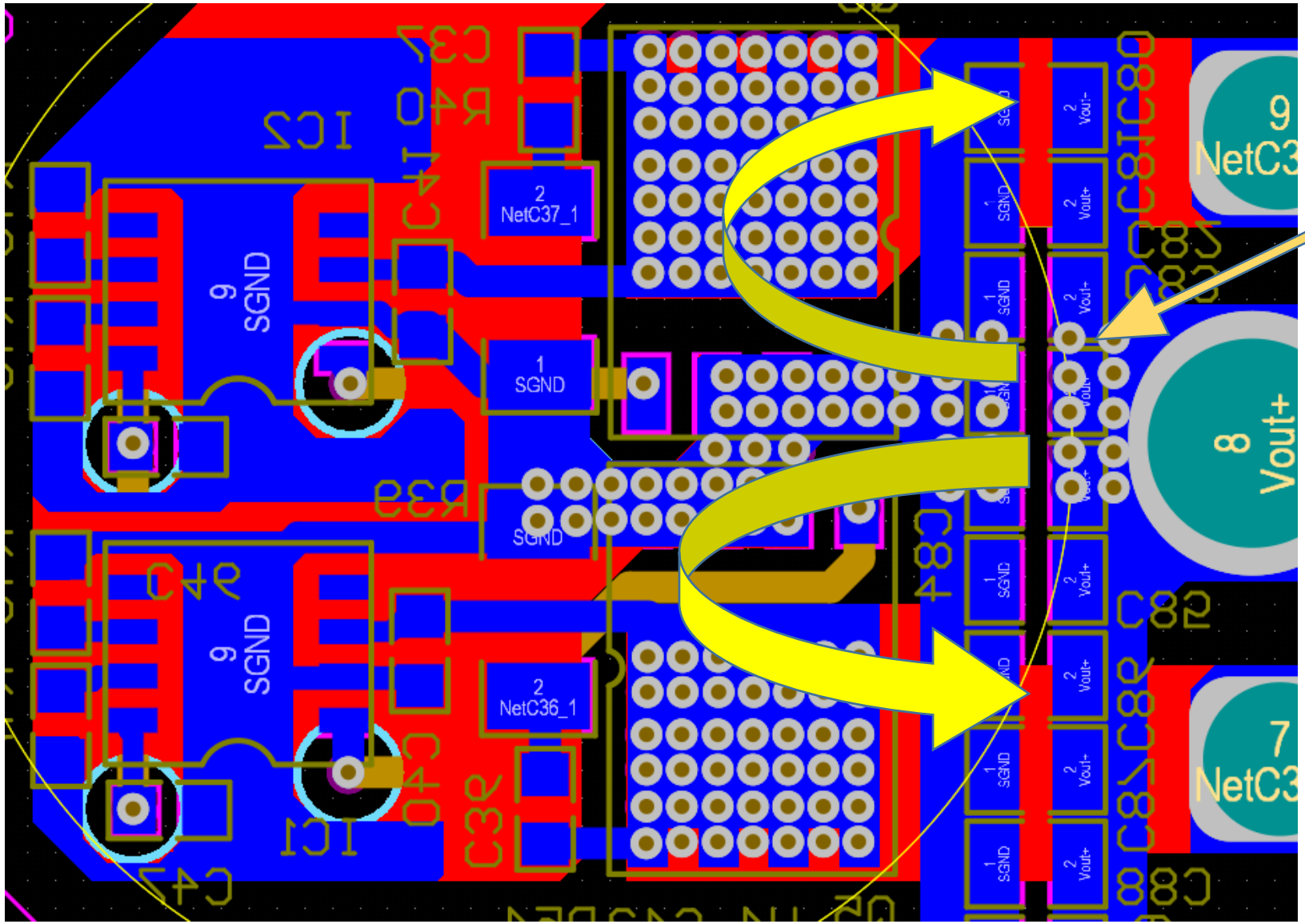
Low-side GaN



High-side GaN

Should have no any overlap between high-side node and low-side node.

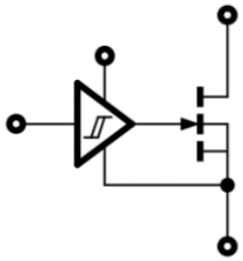
Layout Guideline



Minimum power loop is important for efficiency

NV6115/7 (650V GaNFast™ Power IC)

QFN 5 x 6 mm



Simplified schematic

Features

- Monolithically-integrated gate drive
- Wide logic input range with hysteresis
- 5 V / 15 V input-compatible
- Wide V_{CC} range (10 to 24 V)
- Programmable turn-on dV/dt
- 200 V/ns dV/dt immunity
- 650 V eMode GaN FET
- Low 170 mΩ resistance
- Zero reverse recovery charge
- 2 MHz operation

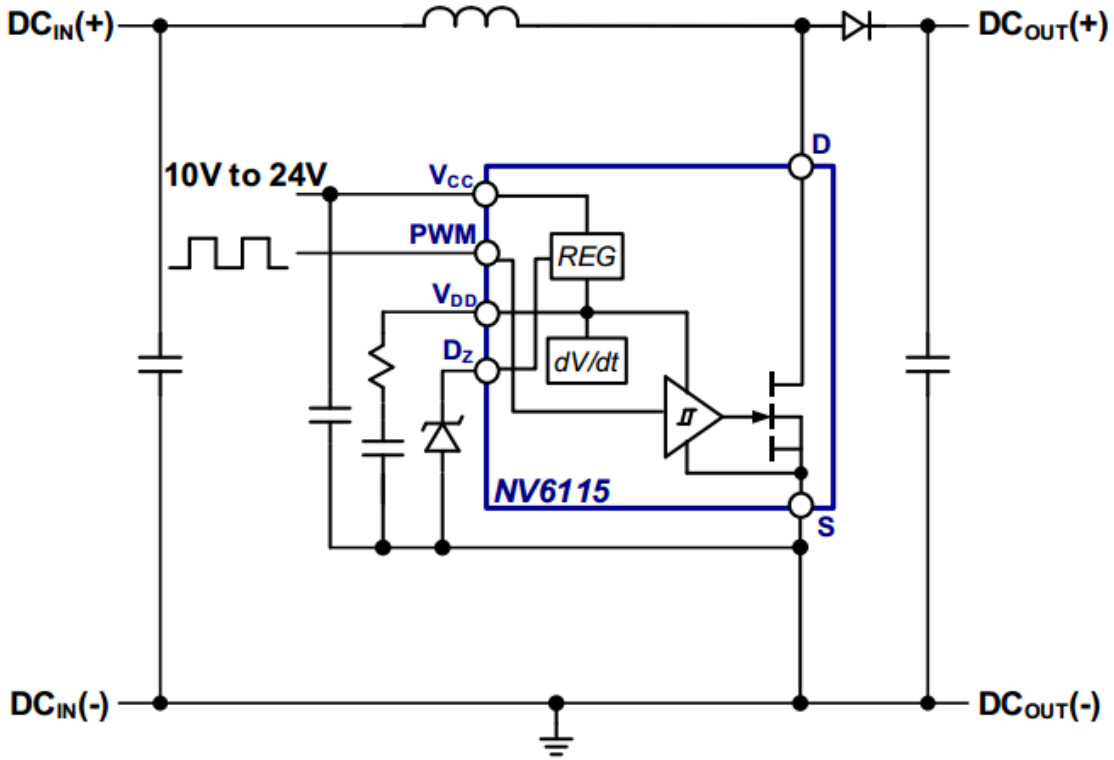


Fig 1. Boost application diagram

NV6115 (Connection, Components)

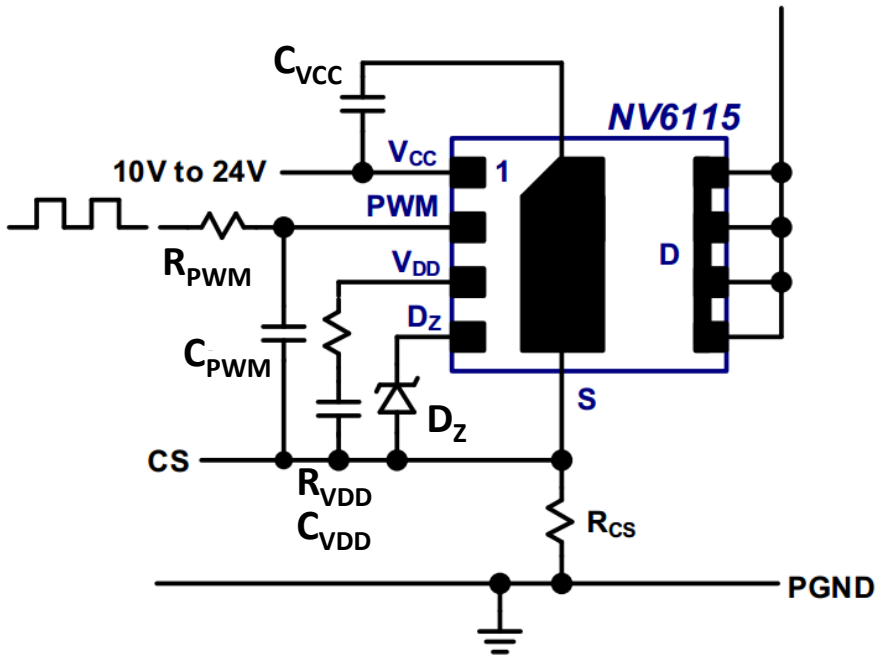


Fig 1. GaN Power IC connection diagram

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} supply filter capacitor	0.1	µF
C_{VDD}	V_{DD} supply capacitors	0.01	µF
R_{VDD}	Gate drive turn-on current set resistor	25 (range 10 to 400)	Ω
R_{PWM}	PWM filter resistor	100	Ω
C_{PWM}	PWM filter capacitor	100	pF

Table I. Recommended component values (typical only).

SYM	DESCRIPTION	PART NO.	SUPPLIER	TYP	UNITS
D_Z	V_{DD} set Zener diode (D_Z pin)	BZT52B6V2 RHG	Taiwan Semiconductor Corporation	6.2	V
		MM3Z6V2ST1G	ON-Semiconductor		
		PDZ6.2B.115	Nexperia (NXP)		
		PLVA662A.215	Nexperia (NXP)		
		LM3Z6V2T1	Leshan Radio Company		

Table II. Qualified Zener diode components to be used with this GaN Power IC.

NV6115 (Timing Diagram)

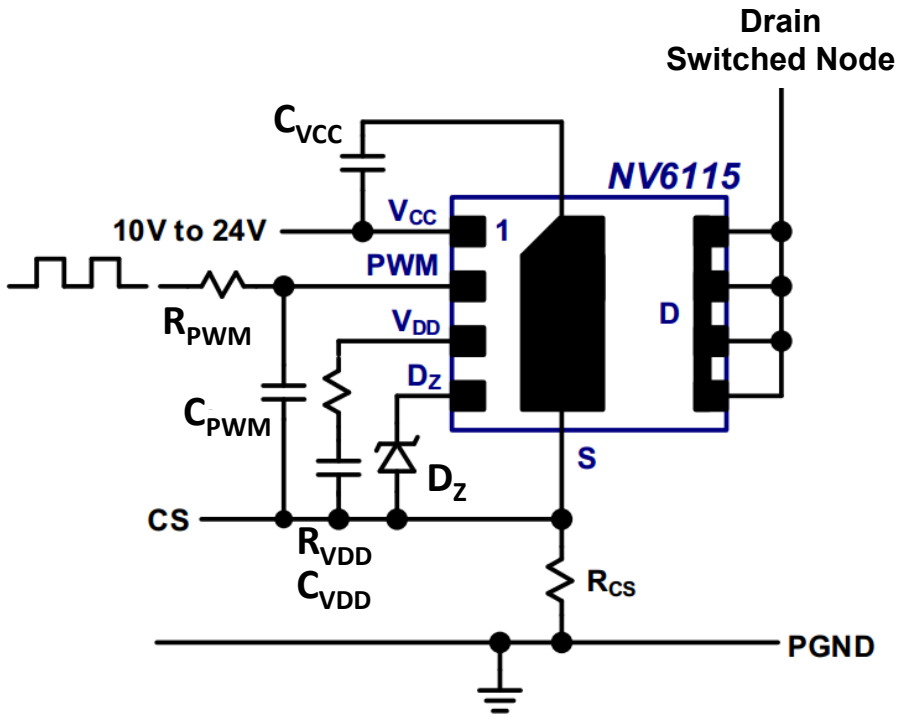


Fig 1. GaN Power IC connection diagram

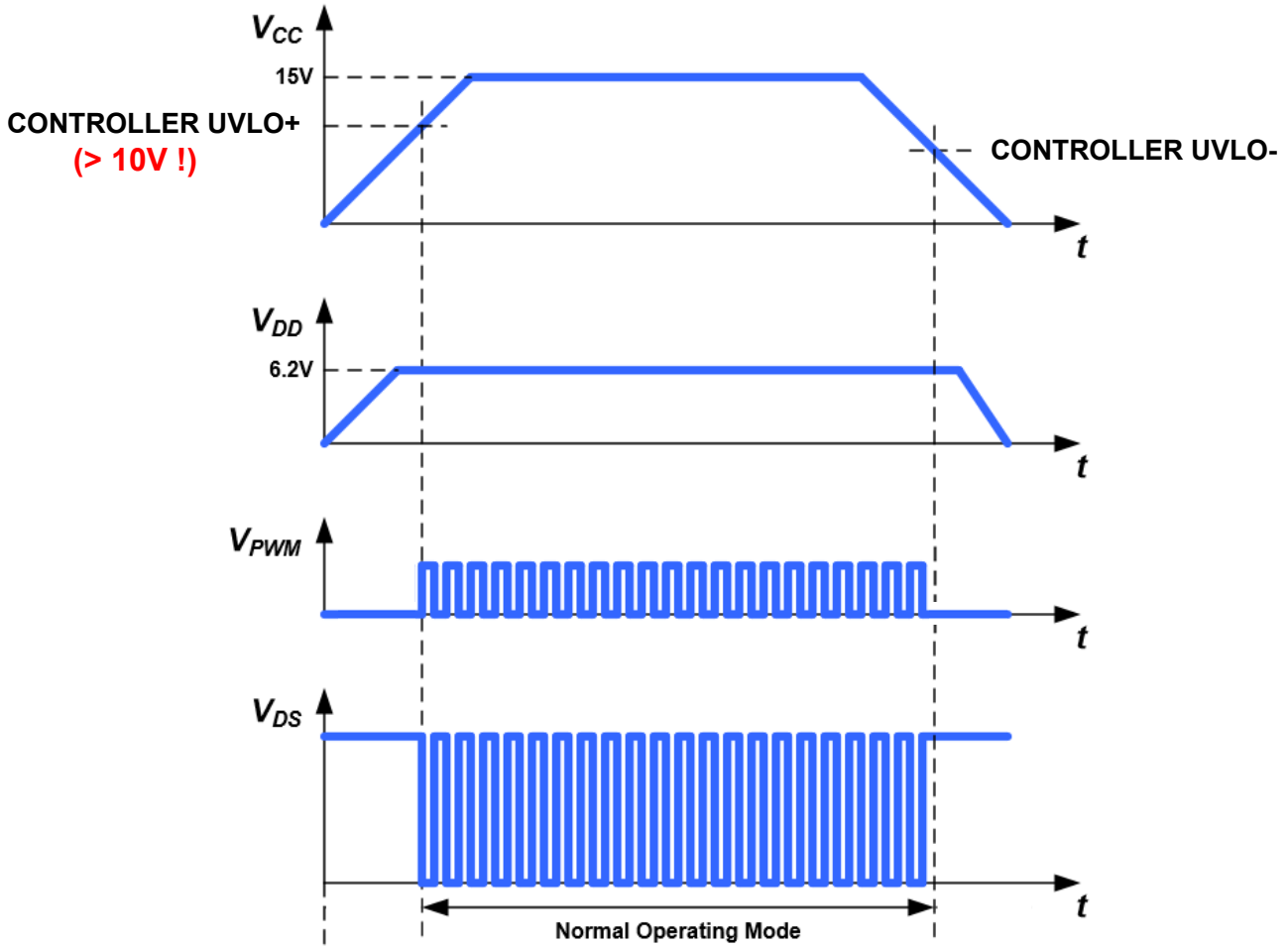


Fig 2. Normal operating mode timing diagram

NV6115 (Turn-on Slew Rate Control)

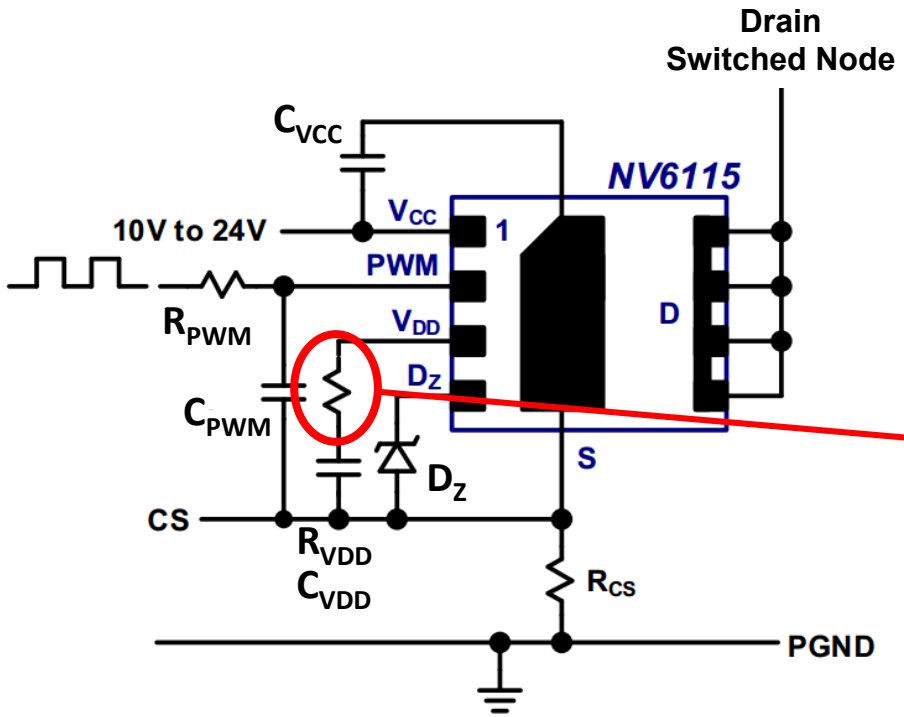


Fig 1. GaN Power IC connection diagram

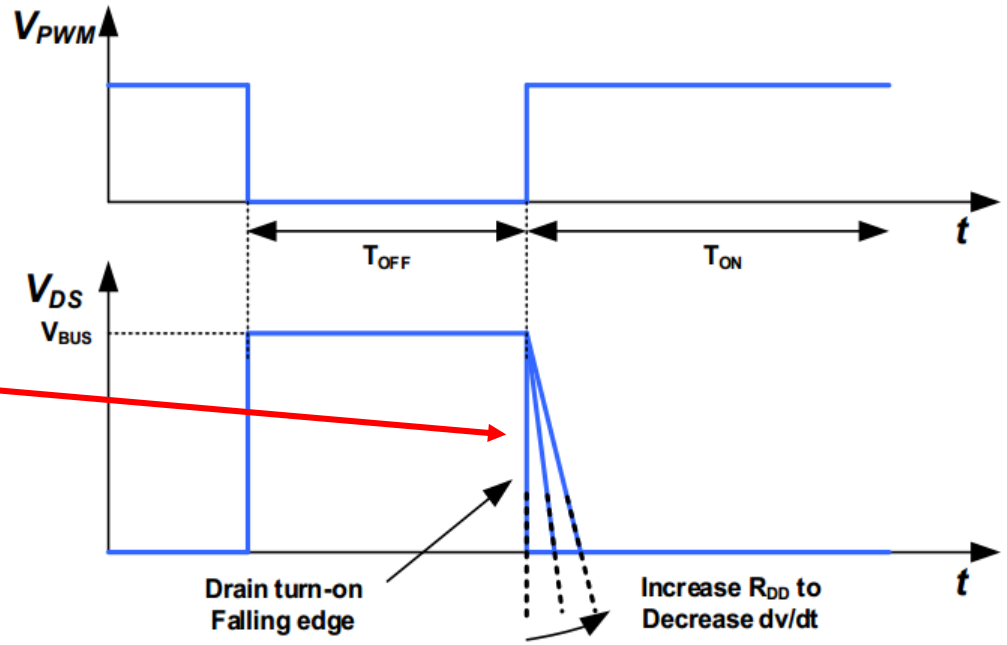
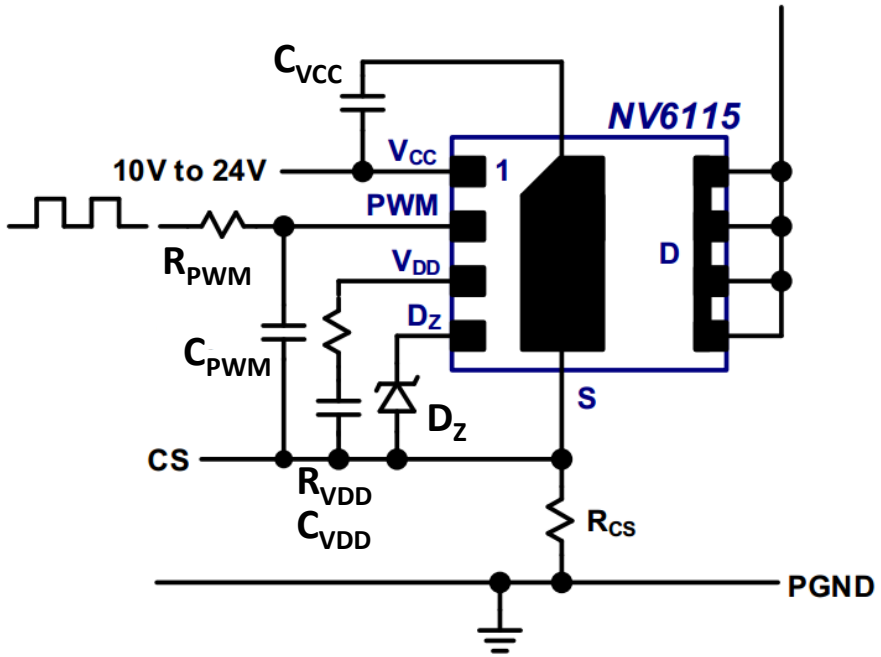
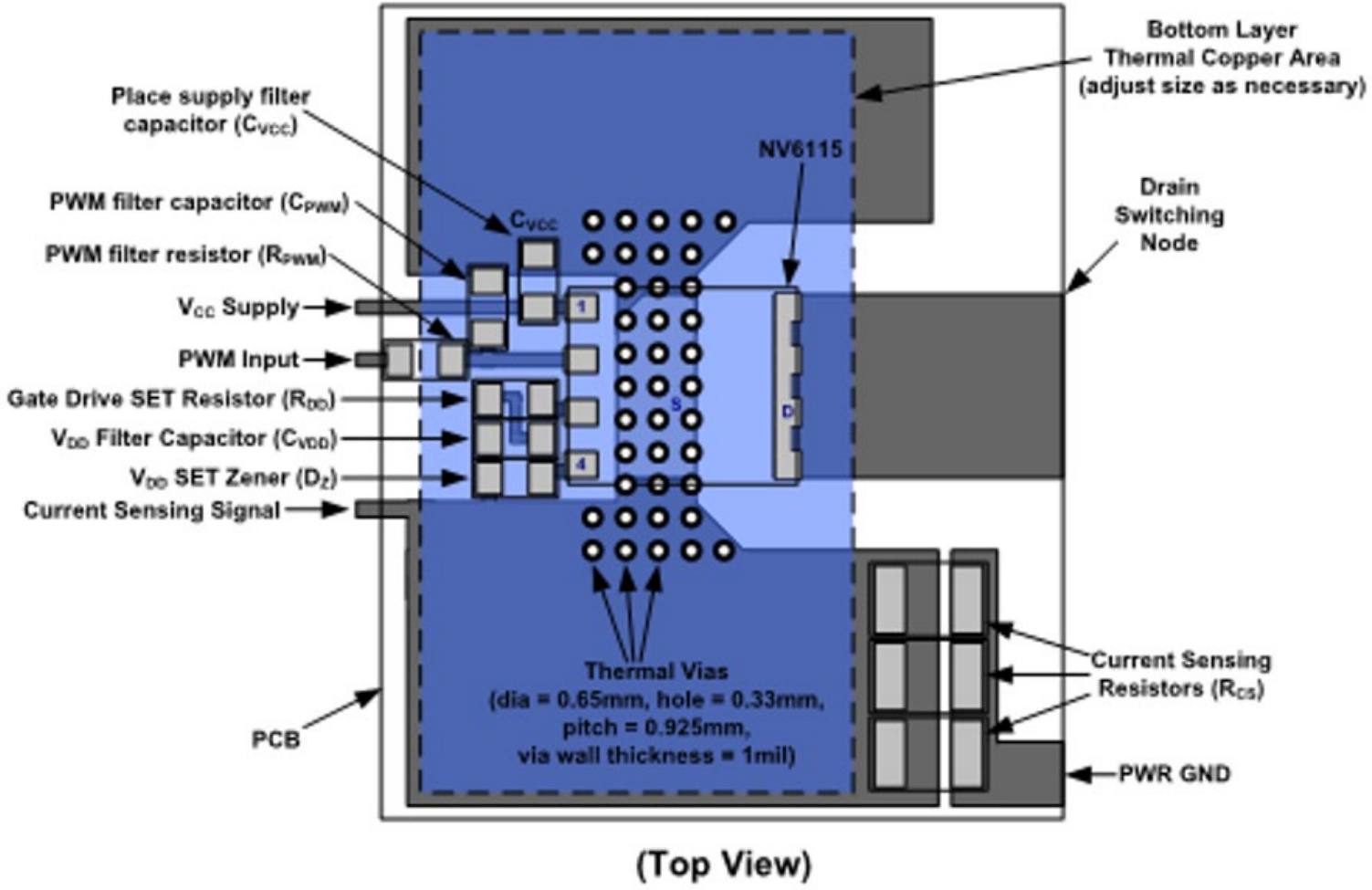


Fig 2. Turn-on Slew rate control timing diagram

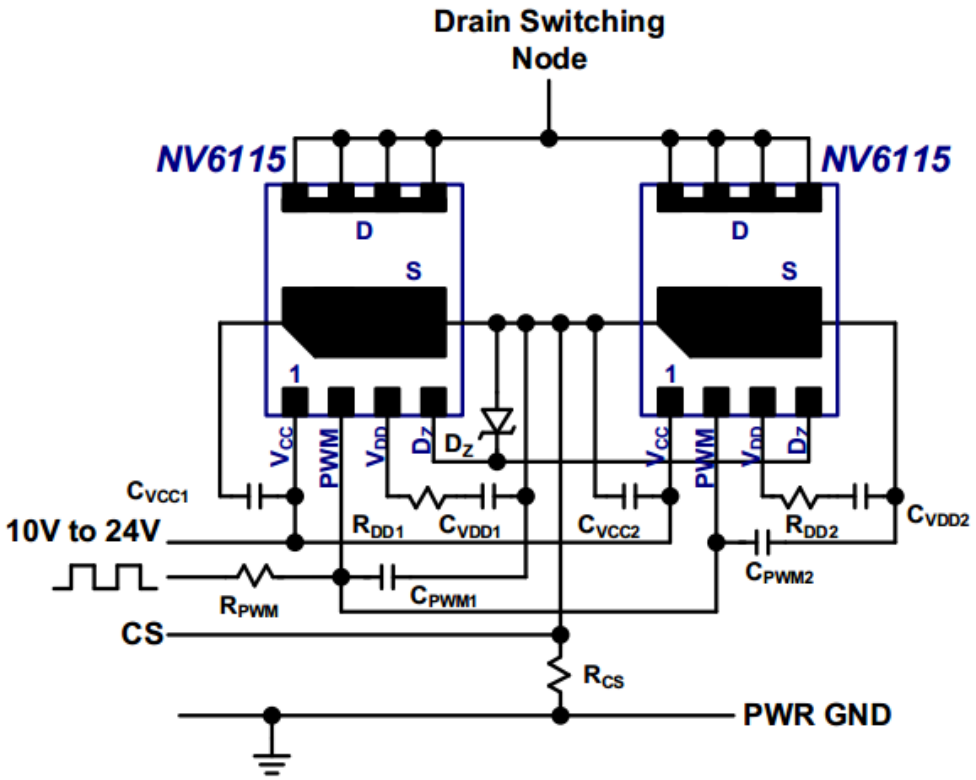
NV6115 (PCB Layout)

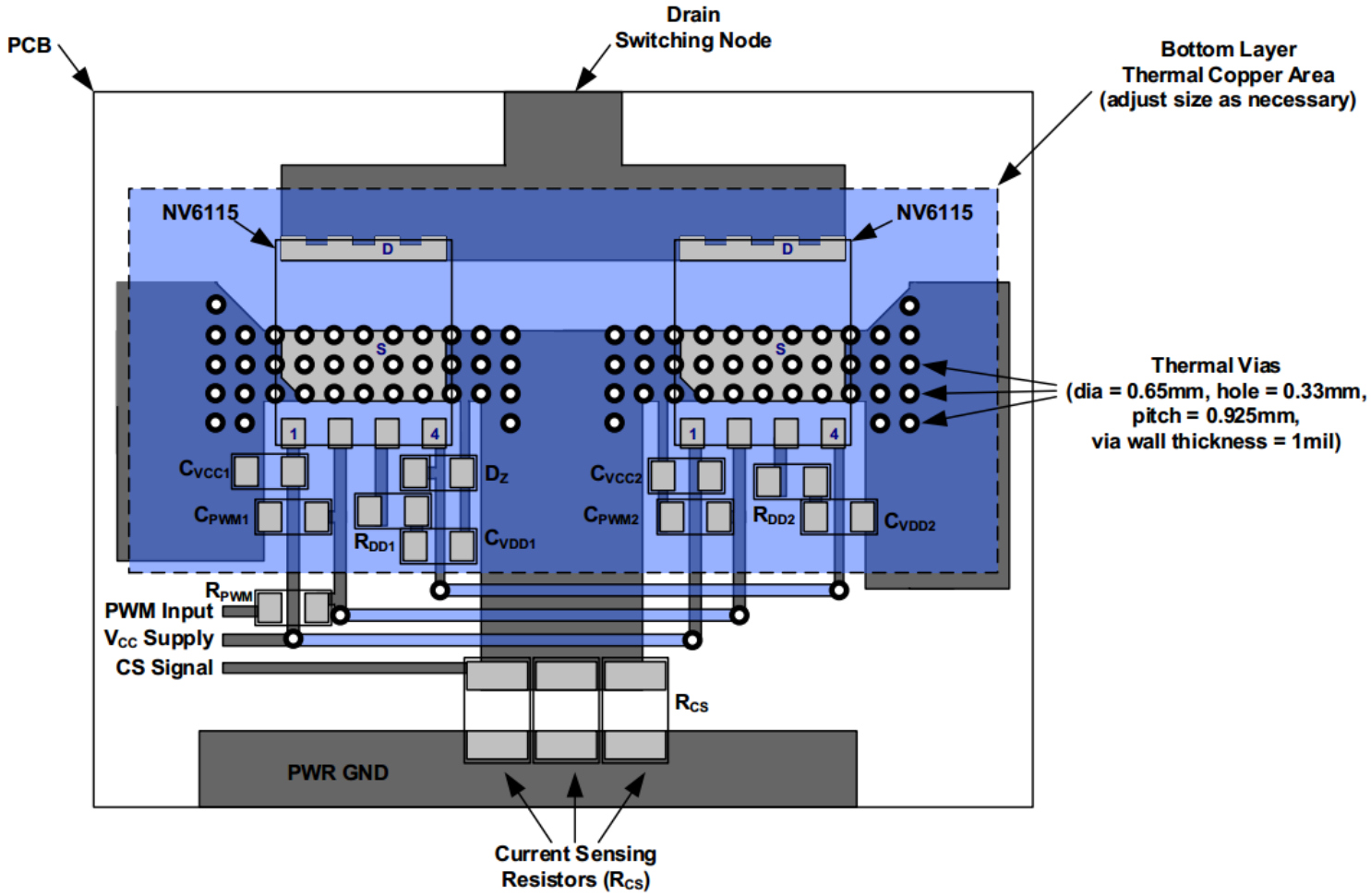




NV6115 (Parallel Configuration)

See datasheet for details and conditions



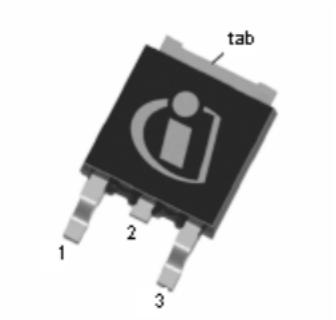


(Top View)

Powertrain GaN vs. Si

GaNFast™

DPAK



IPD60R180P7

Table 1 Key Performance Parameters

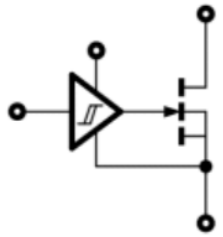
Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	180	mΩ
$Q_{g,typ}$	25	nC
$I_{D,pulse}$	53	A
E_{oss} @ 400V	2.9	µJ
Body diode di_F/dt	900	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPD60R180P7	PG-TO 252-3	60R180P7	see Appendix A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1081	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	19	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	36	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	381	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V

QFN 5 x 6 mm



Simplified schematic

NV6117

GaN FET Characteristics						
I_{DSS}	Drain-Source Leakage Current		0.3	25	µA	V_{DS} = 650 V, V_{PWM} = 0 V
I_{DSS}	Drain-Source Leakage Current		10		µA	V_{DS} = 650 V, V_{PWM} = 0 V, T_C = 125 °C
$R_{DS(ON)}$	Drain-Source Resistance		120	170	mΩ	V_{PWM} = 6 V, I_D = 6 A
V_{SD}	Source-Drain Reverse Voltage		3.2	5	V	V_{PWM} = 0 V, I_{SD} = 6 A
Q_{OSS}	Output Charge		27		nC	V_{DS} = 400 V, V_{PWM} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	
C_{OSS}	Output Capacitance		27		pF	V_{DS} = 400 V, V_{PWM} = 0 V
$C_{O(E)}$	Effective Output Capacitance, Energy Related		41		pF	V_{DS} = 400 V, V_{PWM} = 0 V
$C_{O(T)}$	Effective Output Capacitance, Time Related		67		pF	V_{DS} = 400 V, V_{PWM} = 0 V

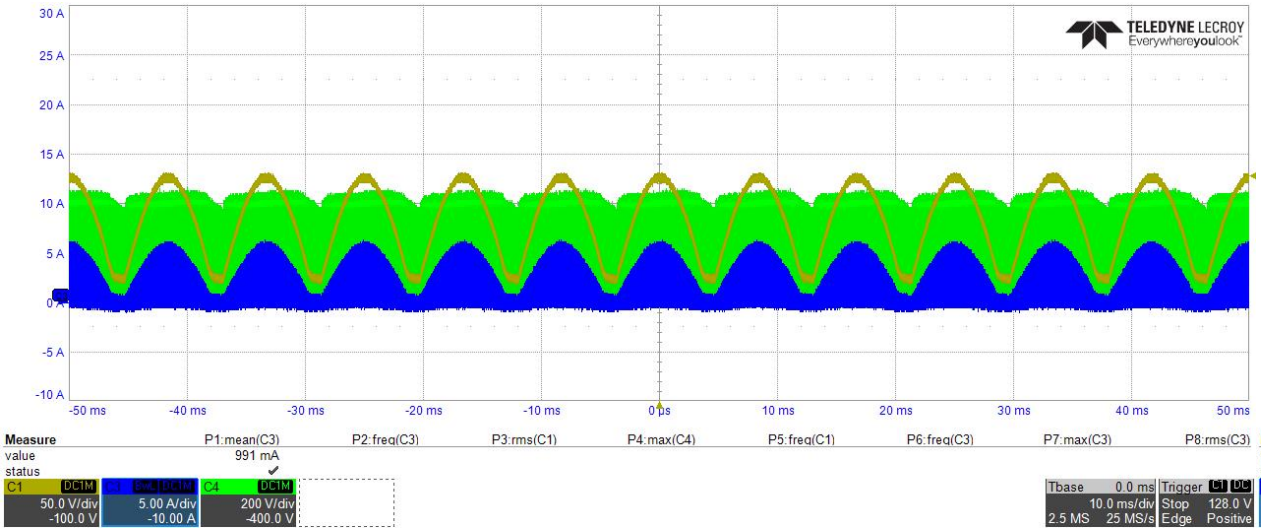
Total Gate Charge	Q_G		1.5		nC	V_{GS} = 0 to 6 V V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		0.55		nC	
Gate-to-Drain Charge	Q_{GD}		0.40		nC	

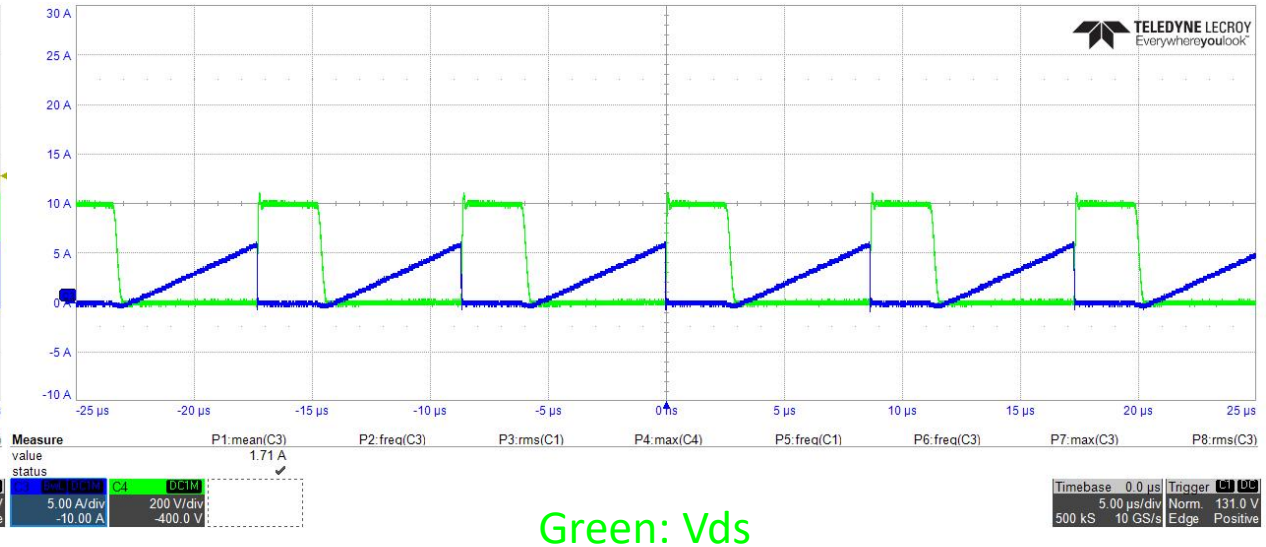
PFC Waveform Comparison

Test condition:

Input: 90 VAC, Output Voltage: 19.5V, Output Current 7.69 A

Zoom In





Green: Vds

Blue: Id

Green: Vds

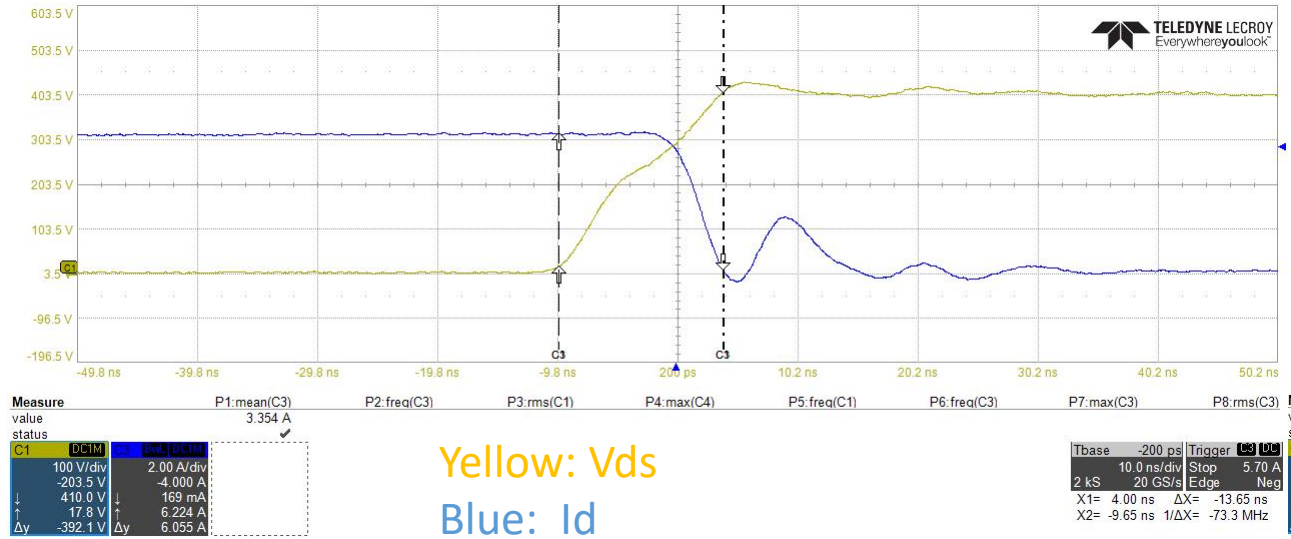
Blue: Id

Yellow: Voltage after the bridge

PFC Waveform Comparison

Test condition:

Input: 90 V_{AC}, Output Voltage: 19.5 V, Output Current 7.69 A

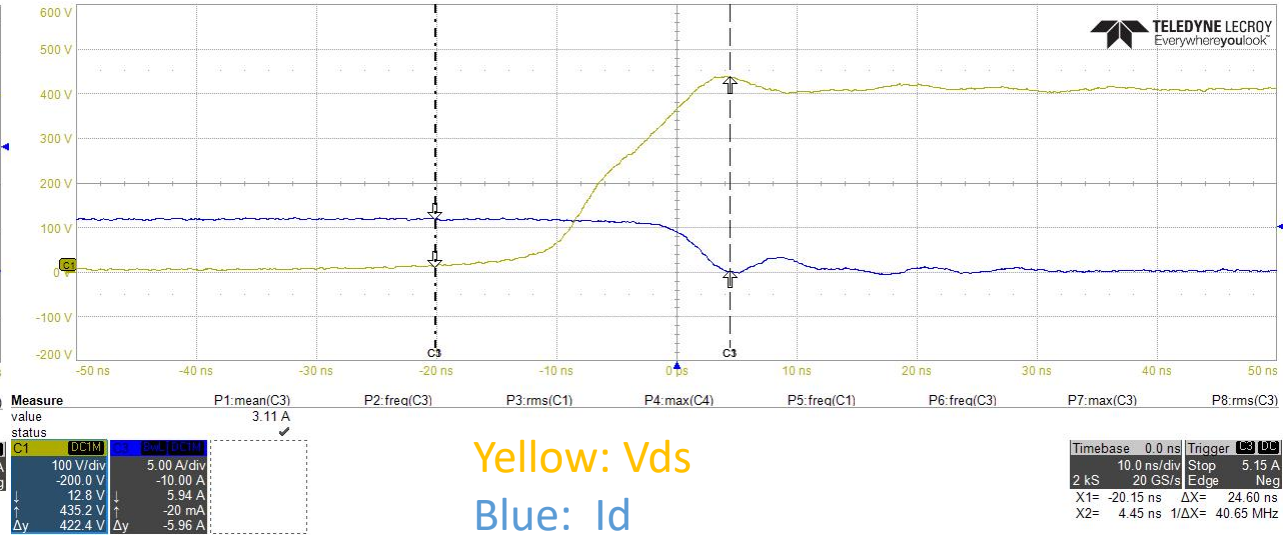


Yellow: Vds

Blue: Id

NV6117

13.65 ns



Yellow: Vds

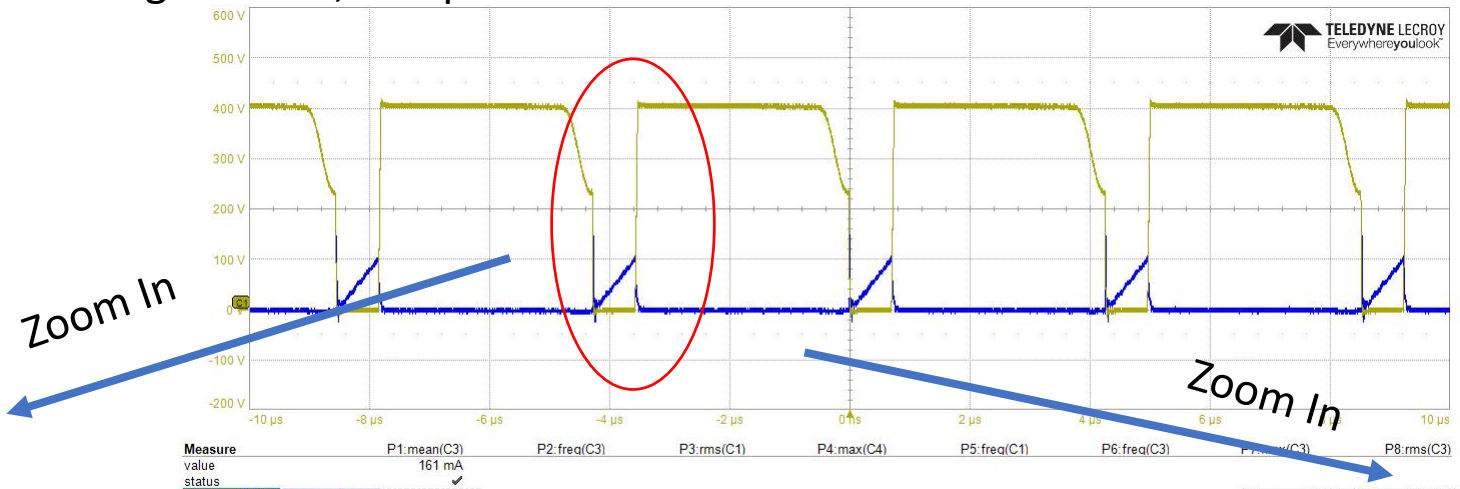
Blue: Id

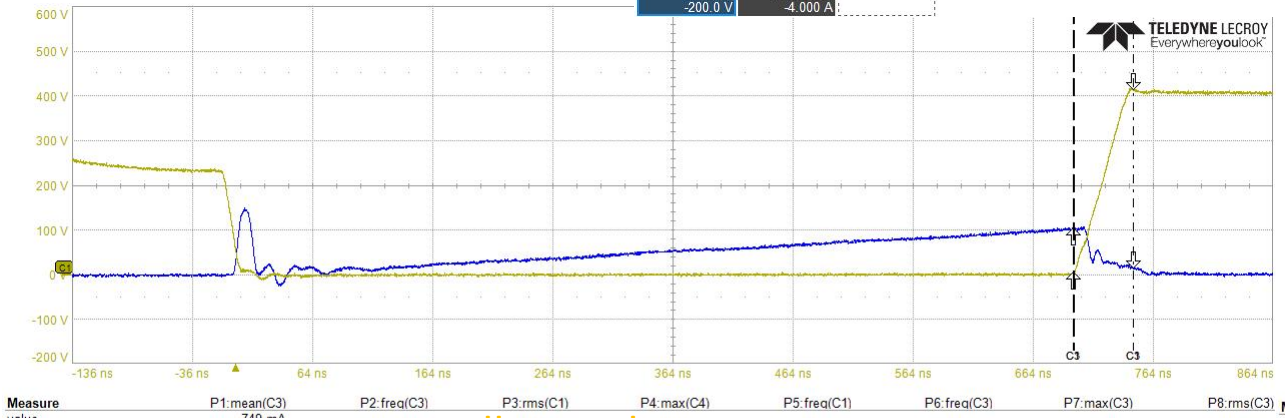
IPD60R180P7

24.6 ns

PFC Waveform Comparison

Input: 230 V_{AC}, Output Voltage: 19.5 V, Output Current 7.69 A



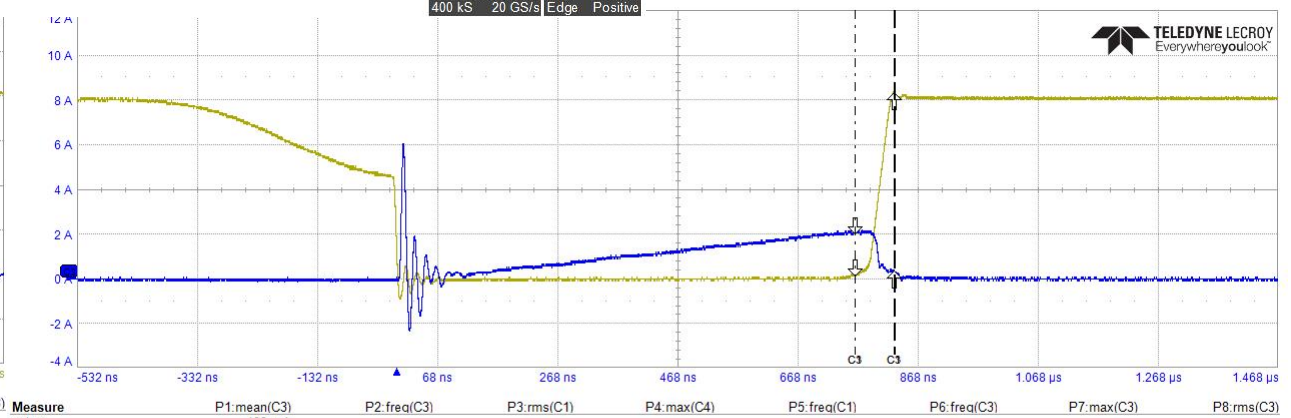


Yellow: Vds

Blue: Id

NV6117

49.8 ns



Yellow: Vds

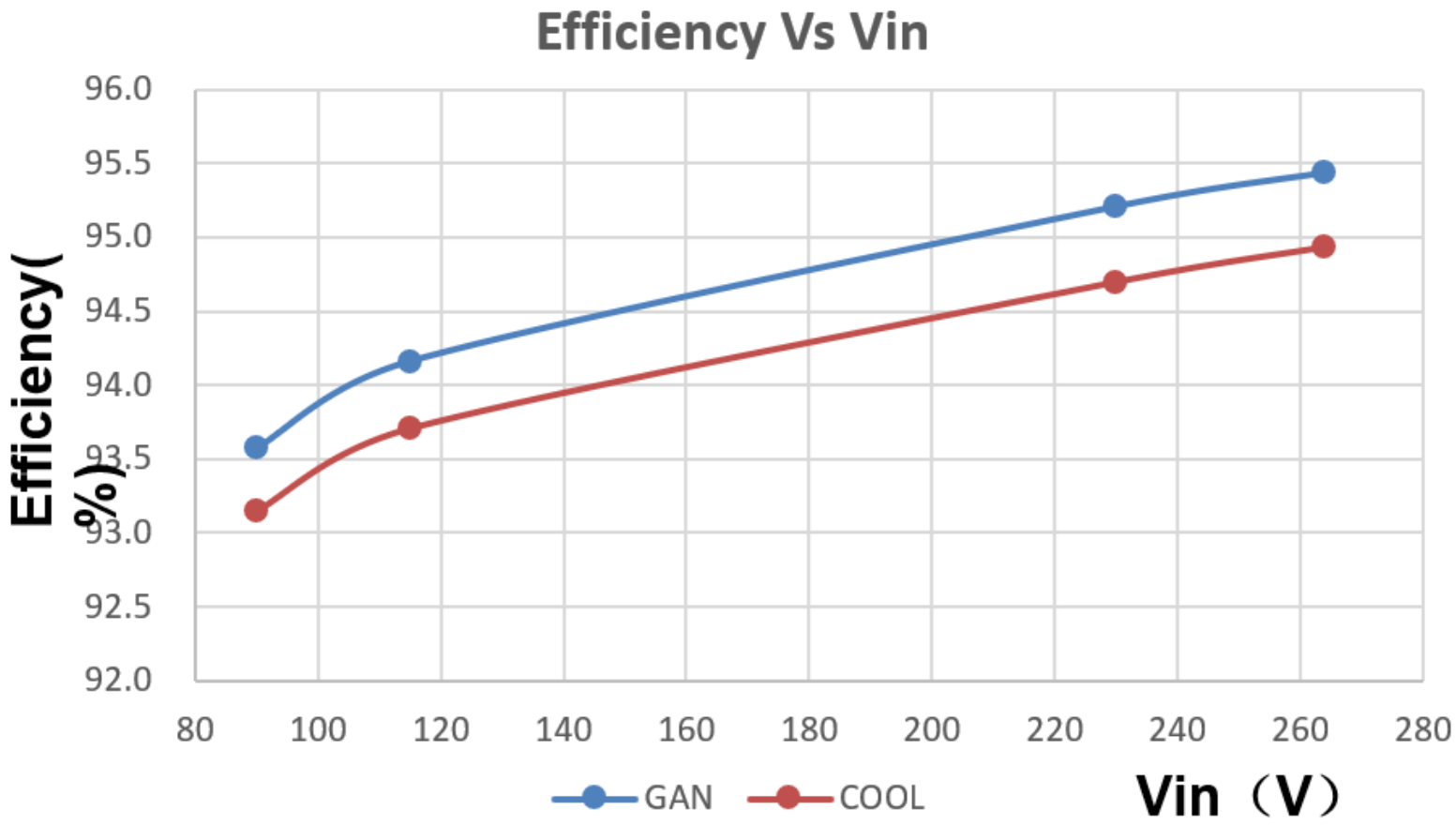
Blue: Id

IPD60R180P7

65.8 ns

PFC Efficiency: GaN vs. Si

Room ambient , Ta=25℃：

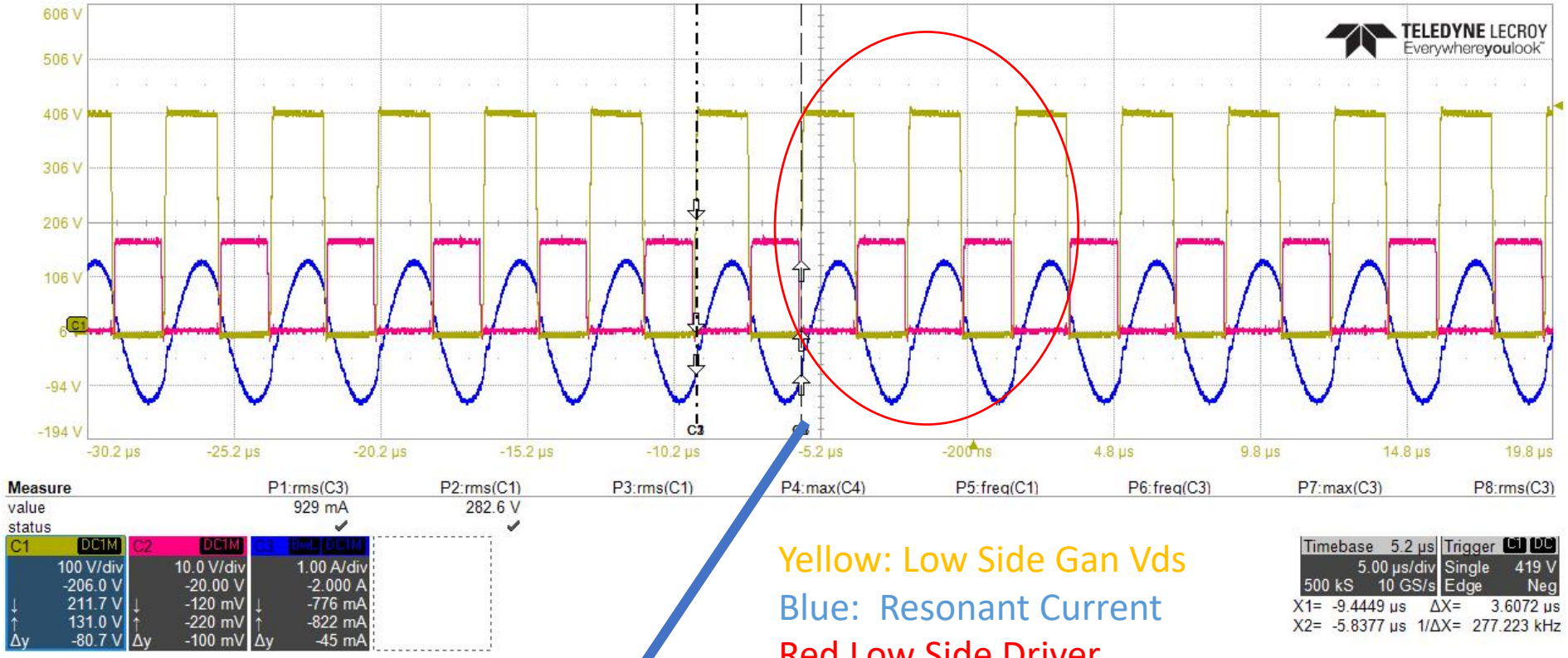


Conclusion: GaN Power IC has much lower C_{OSS}, and faster turn-off, for higher efficiency

LLC Waveform Comparison

Test condition:

Input: 230 V_{AC}, Output Voltage: 19.5 V, Output Current 7.69 A



Yellow: Low Side Gan Vds

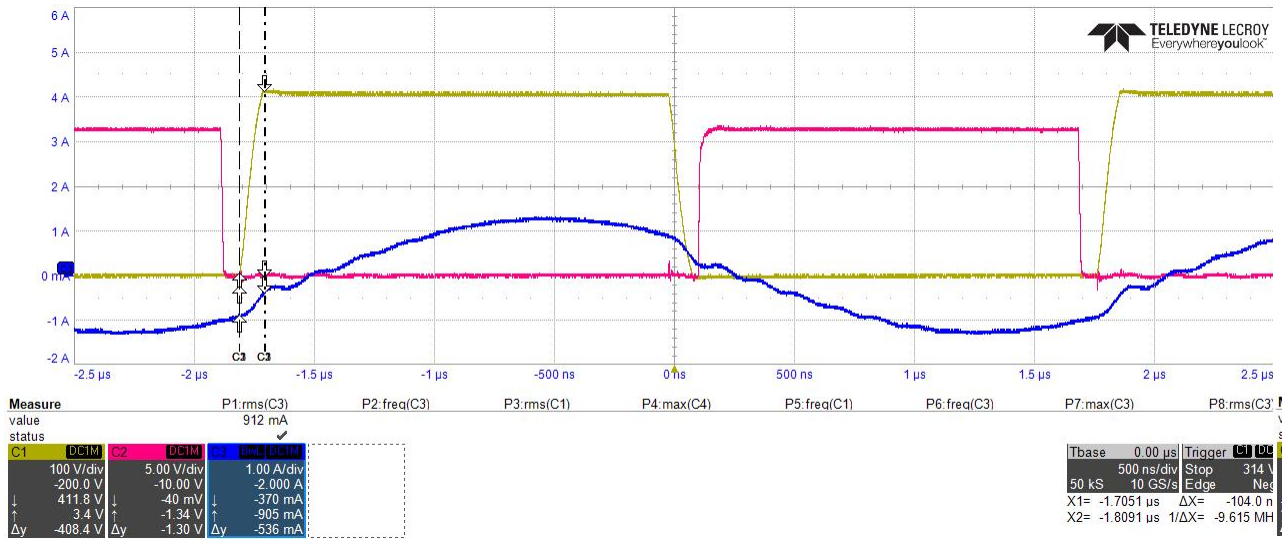
Blue: Resonant Current

Red Low Side Driver

Zoom In on next page

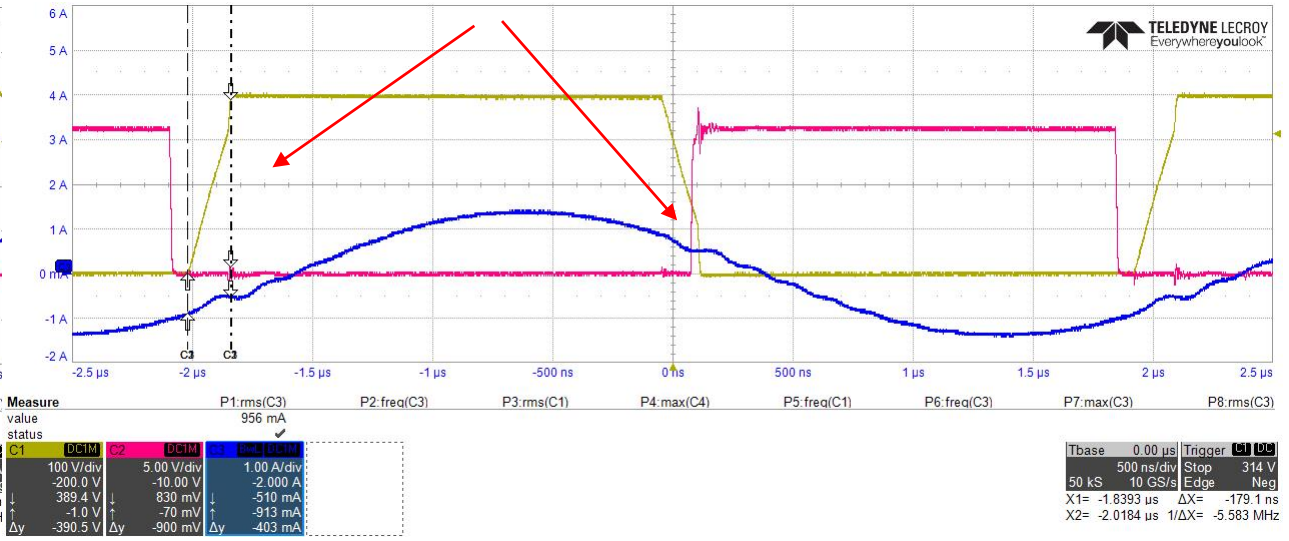
LLC Waveform Comparison

Test condition: Input: 230 V_{AC}, Output Voltage: 19.5 V, Output Current 7.69 A



GaN Power IC

Losing ZVS



Si FET paralleled *with 100pF* added drain-source

Original (left) waveform uses GaN power IC (C_{OSS} = 61 pF)

If a Si FET is used (C_{OSS} = 381 pF), the board blows up immediately.
To capture a waveform, an extra 100pF was added (drain-source) to the FET.

Conclusion: For LLC, very big Si C_{OSS} result in losing ZVS in high-frequency application

Here come the GaN chargers