

High-Speed Gen3 Fast GeneSiC MOSFETs Deliver Best-In-Class Performance

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***Bodo's
Wide Bandgap
Event 2023***

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Silicon Carbide / SiC



Trench-Assisted Planar Gate

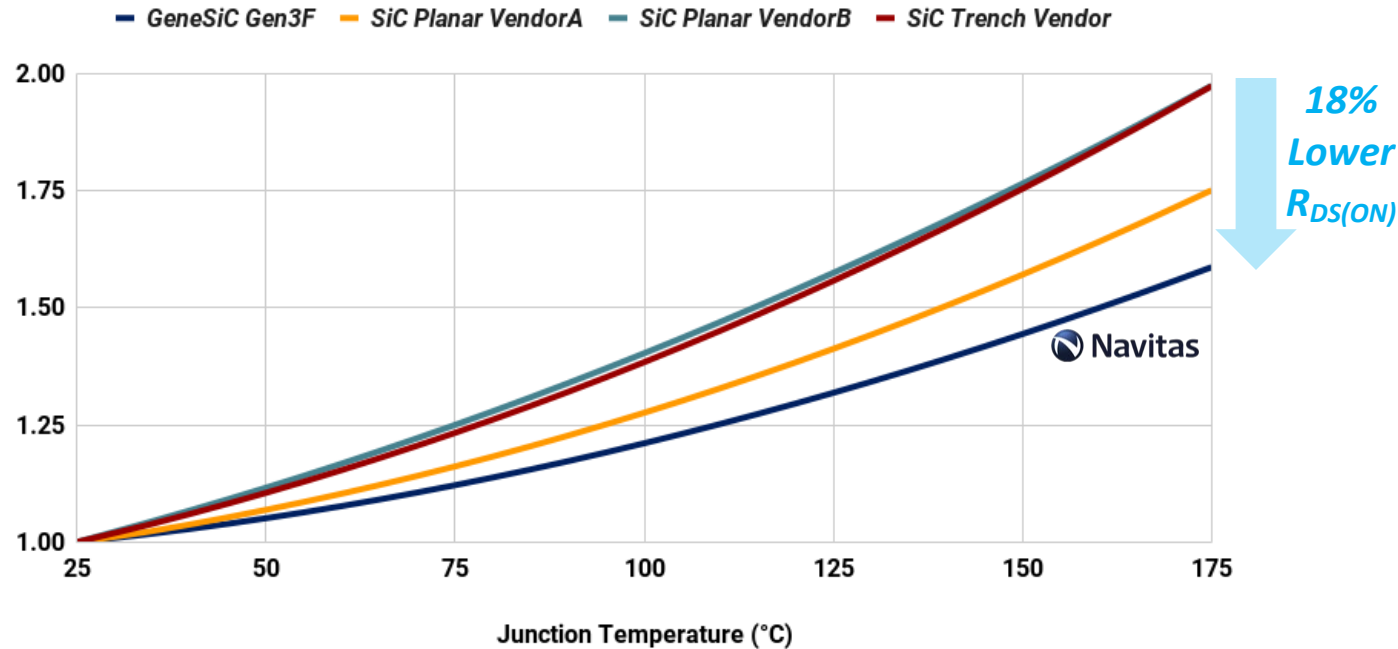
	<p>SiC Planar</p>	<p>SiC Trench</p>	<p>GeneSiC SiC MOSFET</p>
Manufacturability	<ul style="list-style-type: none"> ➤ High-yield & low-cost manufacturing 	<ul style="list-style-type: none"> ➤ Complex manufacturing ➤ Low-yield & high-cost 	<ul style="list-style-type: none"> ➤ High-yield & low-cost manufacturing
Performance	<ul style="list-style-type: none"> ➤ Higher $R_{DS(ON)}$ per chip area ➤ Slower switching FoM 	<ul style="list-style-type: none"> ➤ Lower $R_{DS(ON)}$ per chip area ➤ Faster switching FoM ➤ Worst $R_{DS(ON)}$ vs. temperature 	<ul style="list-style-type: none"> ➤ Lowest $R_{DS(ON)}$ per chip area ➤ Faster switching FoM ➤ Stable $R_{DS(ON)}$ vs. temperature
Reliability	<ul style="list-style-type: none"> ➤ Simpler device structure enables excellent reliability 	<ul style="list-style-type: none"> ➤ Reliability concerns due to complex device structure 	<ul style="list-style-type: none"> ➤ Simpler device structure enables excellent reliability

Trench-gate advantage is NOT true in SiC

Gen3 Fast SiC MOSFETs for Industry-Leading Performance Navitas

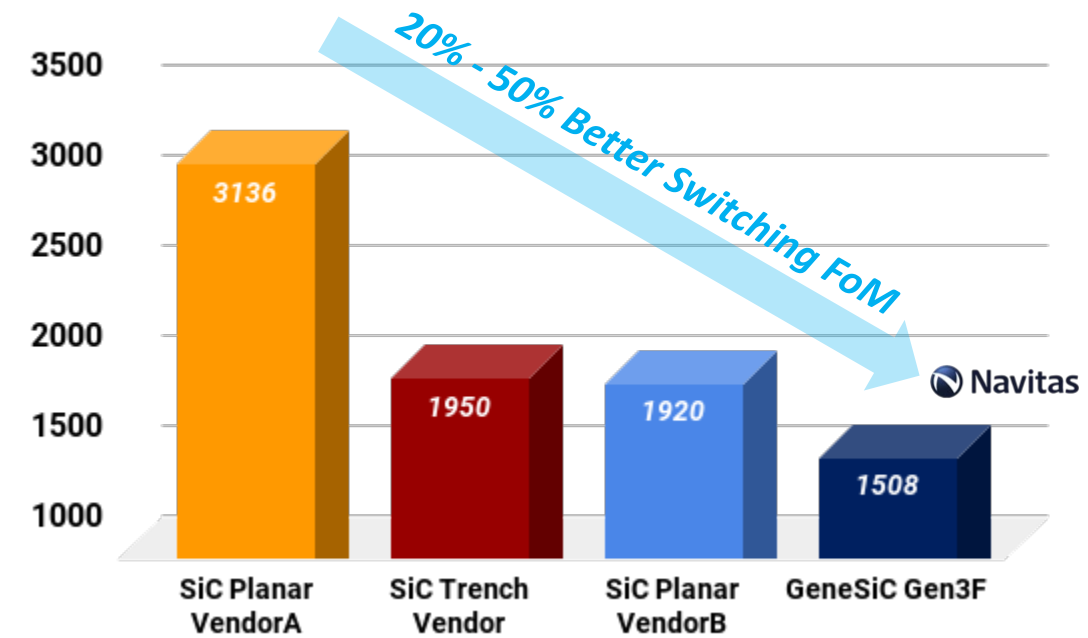
Static Performance (1200V)

$R_{DS(ON)}$ vs. T_j (normalized)



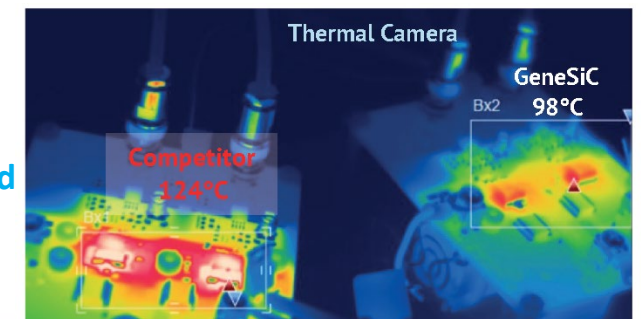
Dynamic Performance (1200V)

$R_{DS(ON)} \times E_{OSS}$ at 125°C (mΩ-μJ)

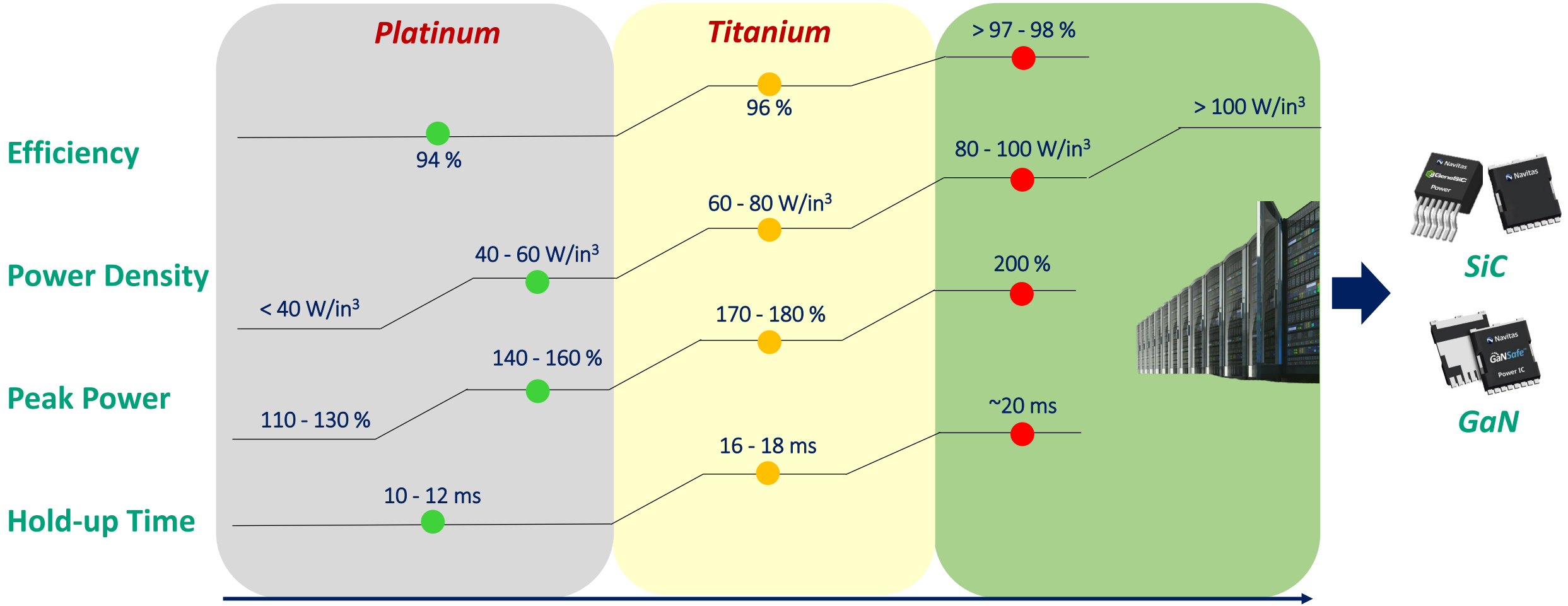


- ❑ Gen3 Fast offers 10% -18% lower $R_{DS(ON)}$ at hot temperature (175°C)
- ❑ 20% - 50% better $R_{ON} \times E_{OSS}$ switching figure-of-merit
- ❑ Enables lower losses and cooler operation
 - ✓ Better system efficiency and longer lifetime

In-Circuit High-Speed Test

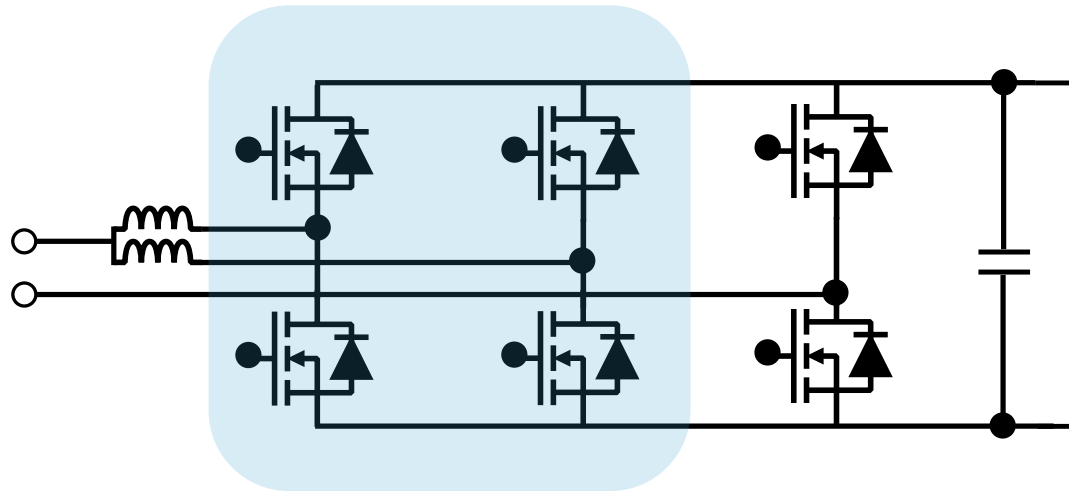


Data-Center PSU Trend Towards High Efficiency and High Power Density



SiC & GaN are key semiconductor technologies to meet server PSU development

Interleaved CCM Totem-Pole PFC (> 2.7kW CRPS)



650V SiC MOSFETs

Key MOSFET parameters for CCM TP PFC

- Low $R_{DS(ON)}$ at all temperatures
- Low E_{OSS} , Q_{RR} , Q_G
- Low body diode V_F and low $C_{OSS,tr}$
- High, stable $V_{GS(TH)}$ and high C_{ISS}/C_{RSS}



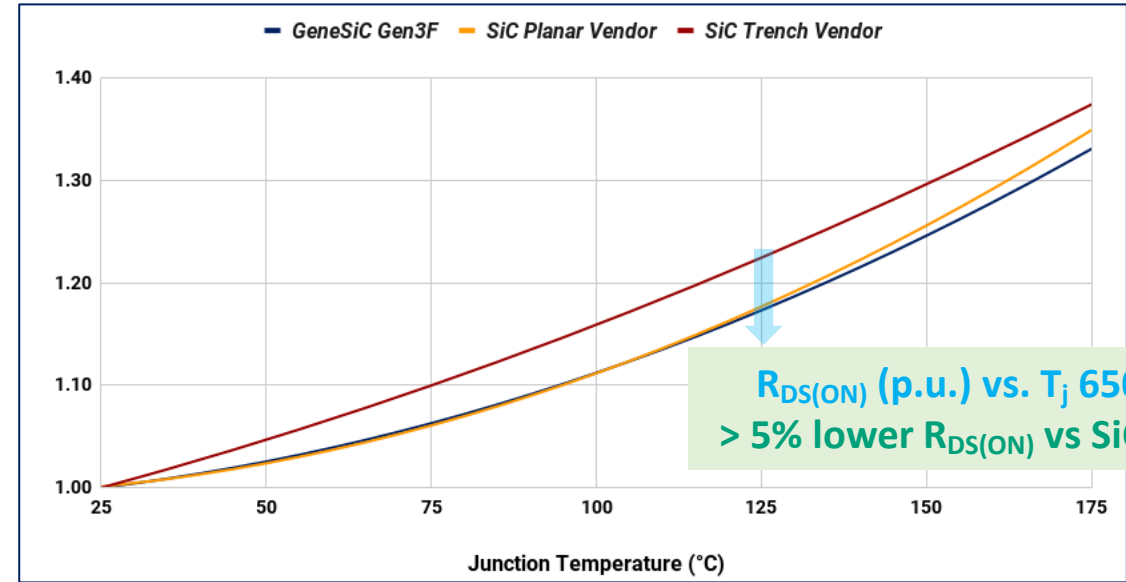
$R_{DS(ON)}$ @ $V_G = 18V, T_j = 25^\circ C$	TO-LL	TO-263-7
650V 25m Ω	G3F25MT06L	G3F25MT06J
650V 33m Ω	G3F33MT06L	G3F33MT06J
650V 45m Ω	G3F45MT06L	G3F45MT06J
650V 60m Ω	G3F60MT06L	G3F60MT06J

- TO-LL (Transistor Outline Lead-Less) package
- 30% savings in PCB area than TO-263-7 (D2PAK-7L)
- 2.30mm profile, 60% less volume than TO-263-7
- Low package inductance - 2nH
- Kelvin-source packages for lowest switching losses
- 100% avalanche (UIL) tested SiC MOSFETs

Figure of Merits (FoM) for CCM Totem-Pole PFC

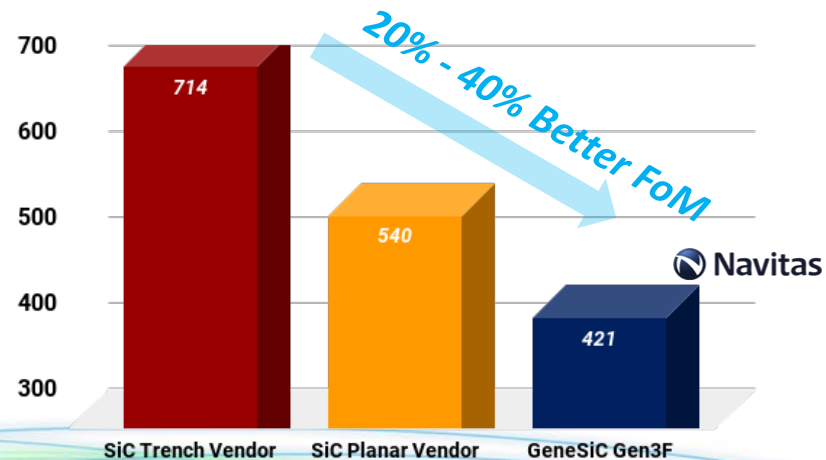
☐ Lowest $R_{DS(ON)}$ at all temperatures
✓ Lowest conduction losses

☐ Best-in-class E_{OSS} , Q_{RR} and Q_G
✓ Lowest switching losses

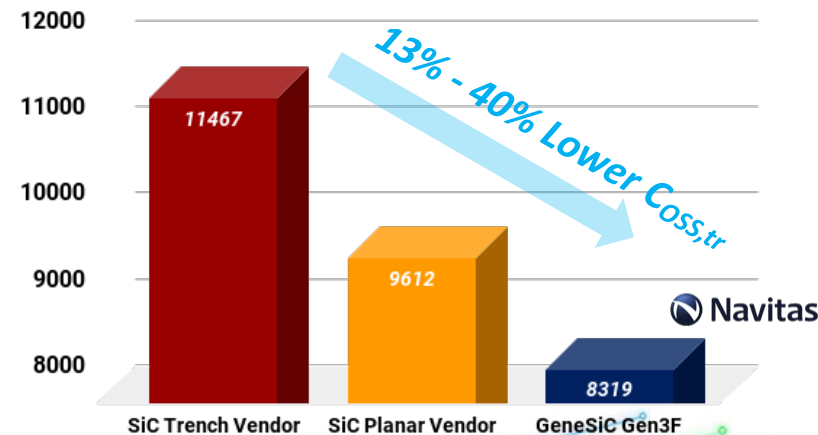


Hard-Switching FoM (650V)

$R_{DS(ON)} \times E_{OSS}$ at 125°C (mΩ-μJ)



$R_{DS(ON)} \times C_{OSS,tr}$ at 125°C (mΩ-pF)



Low body diode V_F and low $C_{OSS,tr}$ to enable low dead-time losses

Switching Robustness (650V)

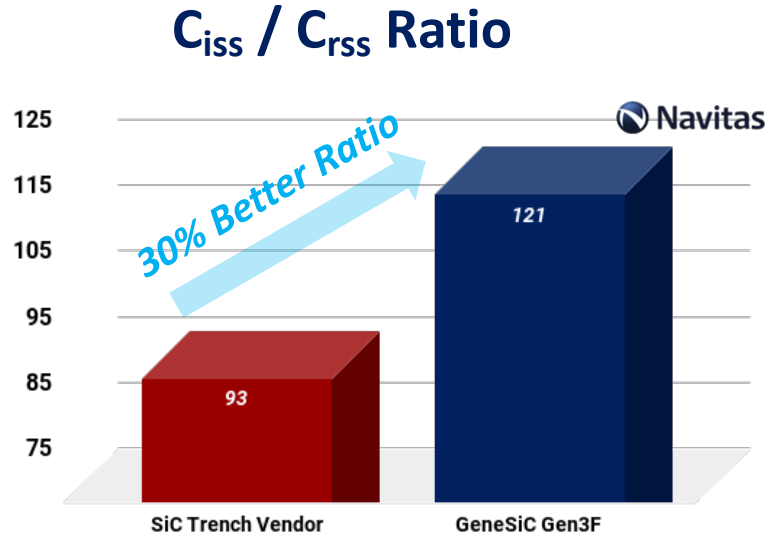
□ Potential V_{GS} overshoot can be estimated by “capacitance ratio”

$$\frac{C_{GS}}{C_{GD}} = \frac{C_{iss}}{C_{rss}} - 1 \quad \rightarrow \quad \Delta V_{GS} = \frac{C_{GD}}{C_{GS}} \Delta V_{DS}$$

□ Higher C_{iss} / C_{rss} ratio (larger C_{GS} in comparison to C_{GD}) is preferred

□ “Gen3 Fast” MOSFETs optimized for “capacitance ratio”

□ ~30% better “capacitance ratio” as compared to SiC trench

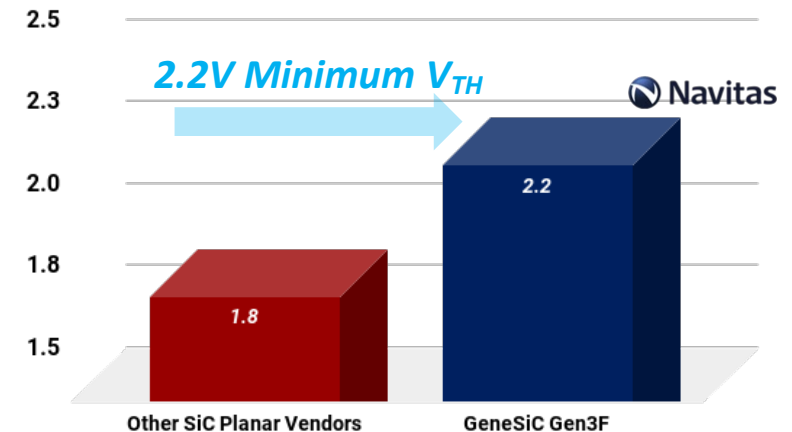


□ Although SiC trench MOSFETs offer higher V_{TH} (~3.5V) they are more susceptible to overshoots, and poor $R_{DS(ON)}$ vs. T_j and $R_{DS(ON)} * E_{OSS}$ FOMs make them “less efficient”

□ “Gen3 Fast” designed for robust fast-switching performance!

□ 2.2V minimum V_{TH} vs. 1.8V minimum V_{TH} specification from other planar SiC MOSFET vendors. Potential for “0V” turn-off with low-inductance package (TO-LL) and low-inductance PCB design

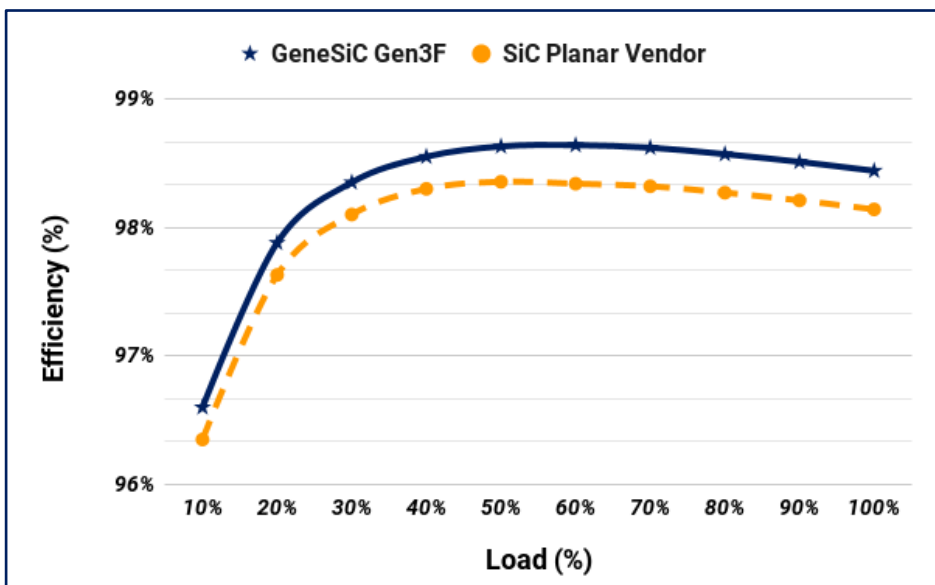
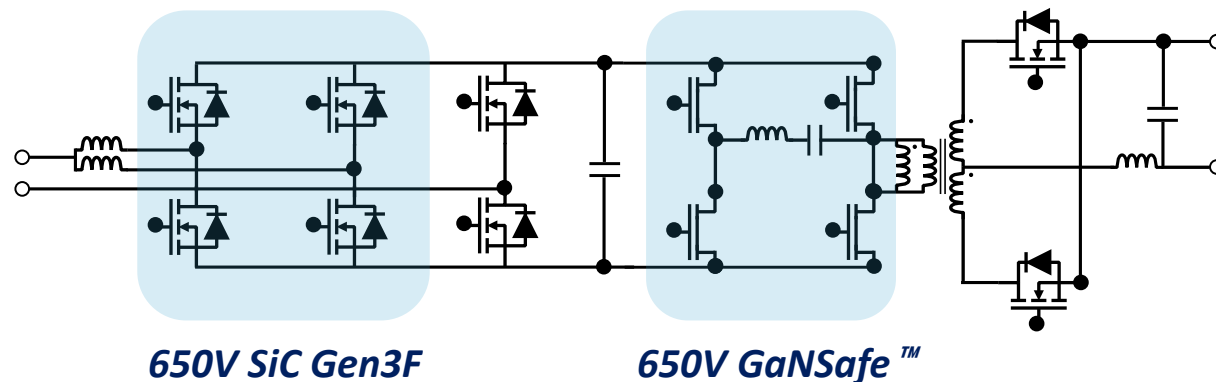
Best-in-Class V_{TH} (Planar SiC)





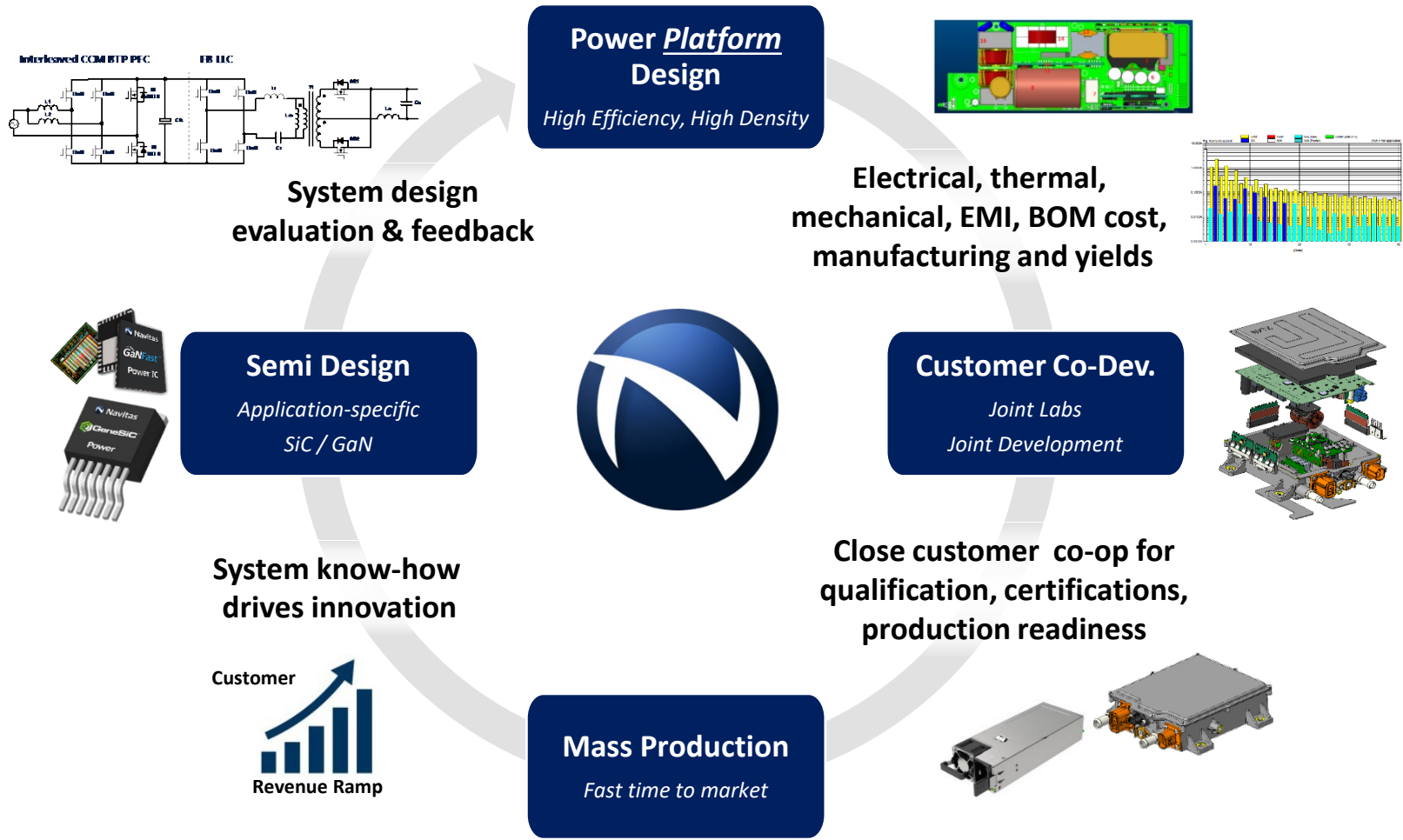
Platform Features

- ❑ Supports 2.7kW, 3kW and 3.2kW
- ❑ Up to 98 W/in³ power density
- ❑ Titanium+ efficiency
 - ❑ 96.3 % @ 50 % load
 - ❑ > 96 % @ 20 % - 60 % load



- ❑ 3.2kW interleaved CCM TP PFC
- ❑ Better than titanium efficiency (titanium requires 96%) measured using GeneSiC Gen3F 650V SiC MOSFETs (*45mΩ TO-LL*)
- ❑ Excellent performance at high input current, high temperature conditions, as Gen3F's conduction loss is the lowest

230V AC input; including EMI loss and auxiliary power loss



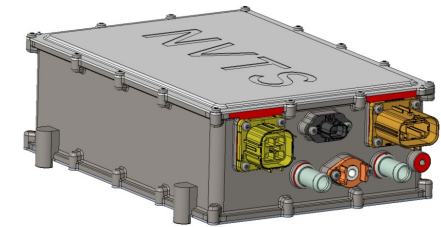
SERVER PSU DESIGN CENTER



3.2kW CRPS Platform
SiC in CCM TP PFC & GaN in FB LLC
98 W/in³ with Titanium+ Efficiency



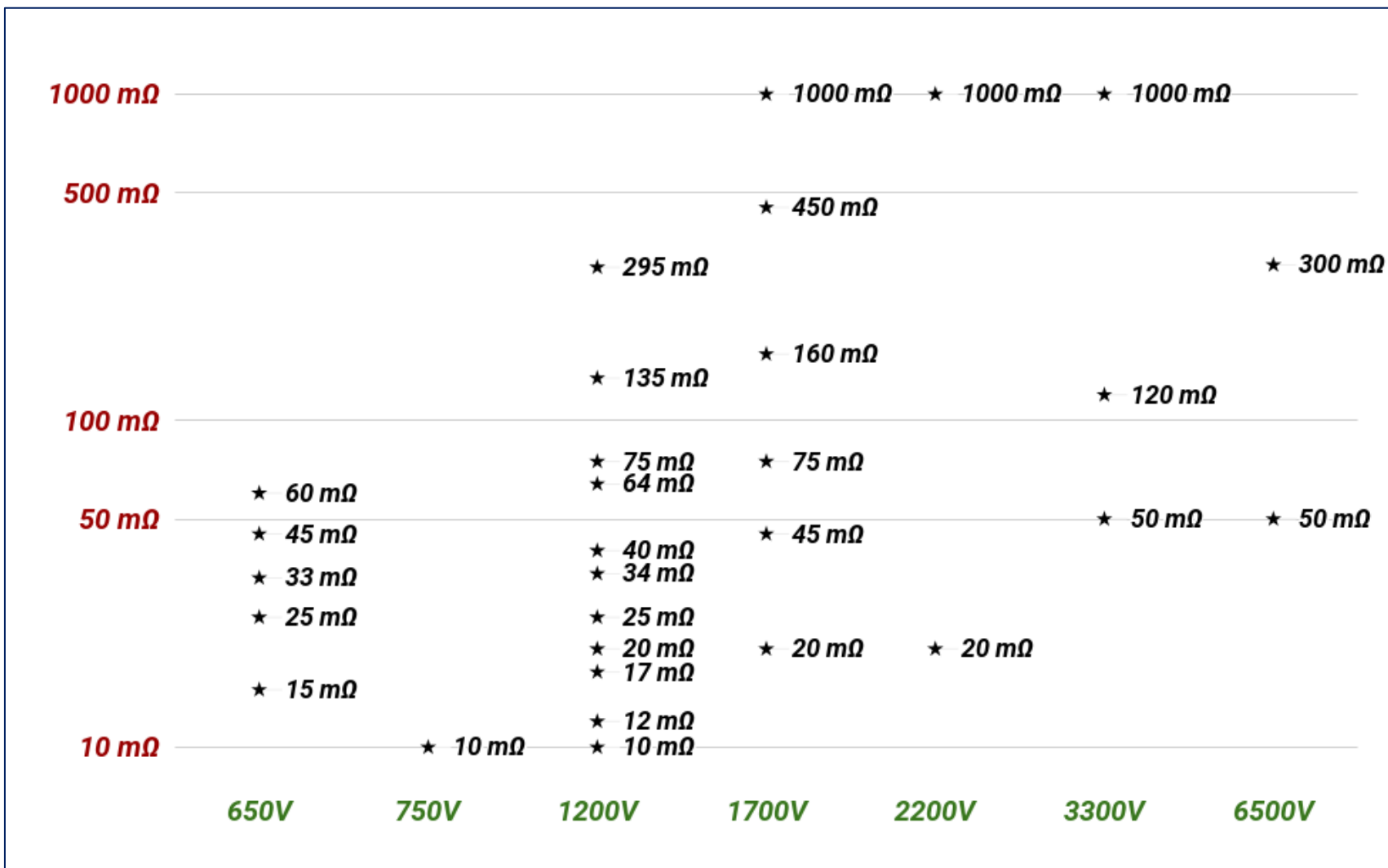
EV SYSTEM DESIGN CENTER



22kW OBC + 3kW DC-DC Combo
Bi-Directional; SiC-based 1- ϕ & 3- ϕ Compatibility
CCM AC/DC (60 kHz) + CLLC DC/DC (120 kHz~250 kHz)
HV-LV DC/DC (65 kHz)

3.5 kW/L with Peak Efficiency > 95.5%

Broadest⁽¹⁾ SiC MOSFET Portfolio

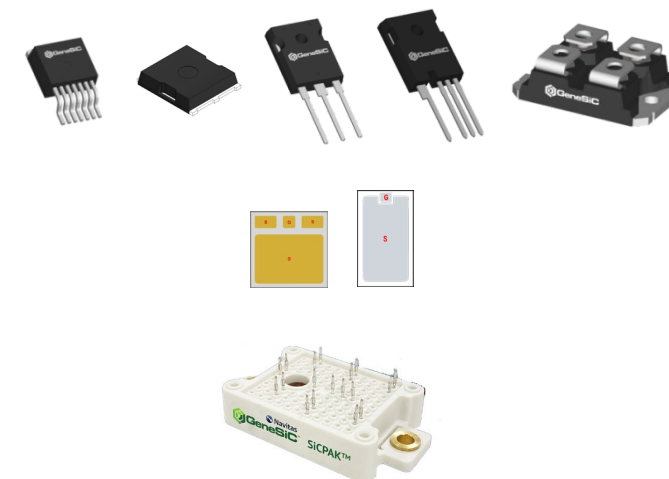


✓ 60+ SiC MOSFET Products

✓ Discrete

✓ Bare Chips

✓ Power Modules



Note (1): based on GeneSiC voltage range of production released SiC MOSFETs compared to all publicly identified voltage ranges of other SiC suppliers.