IS01.2 : Maximizing MVHV SiC Performance and Reliability with Advanced Power Device and Packaging Technologies for Mission-Critical Energy Infrastructure Applications

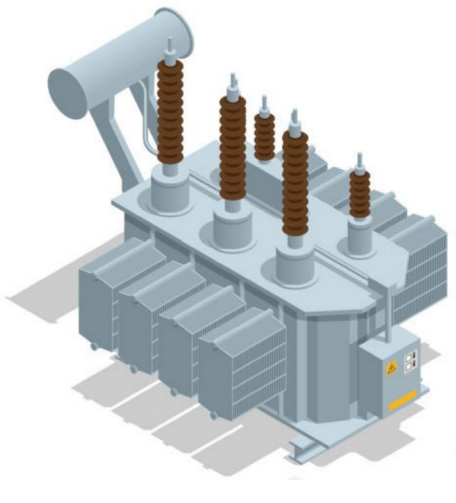
Sumit Jadav

Sr. Director of Technical Marketing, Navitas Semiconductor

Navitas®

Challenges with Existing Energy Infrastructure

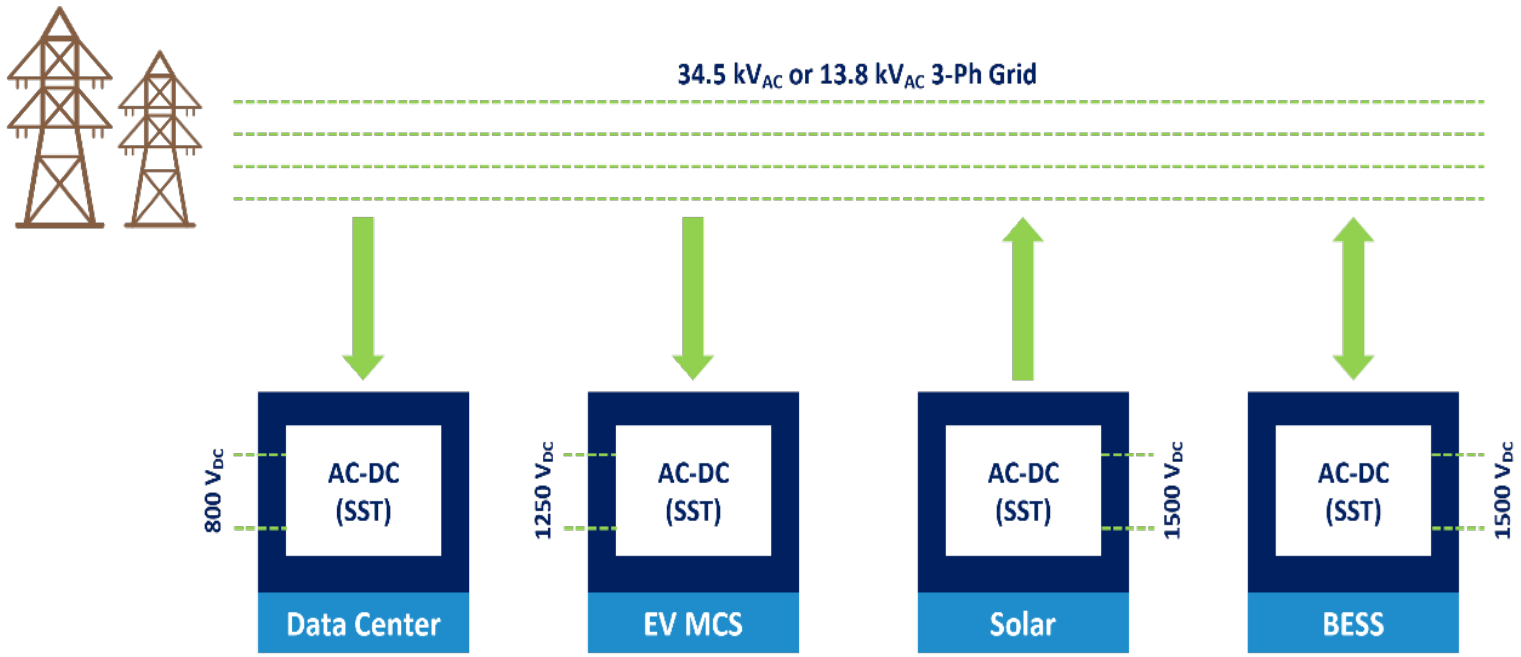
Power transformers are the backbone of power grids that provide step-up/step-down voltage conversion and are needed for galvanic isolation



Widely used line-frequency transformers have inherent limitations:

- **Low Power Density:** Operate at line-frequency (50/60 Hz), hence bulky in weight and volume causing problems for mobility and space allocation
- **Low Efficiency:** Face significant core losses and require second stage AC/DC conversion which reduces overall power transfer efficiency
- **Maintenance Nightmare:** High maintenance cost due to reliance on liquid and solid insulation systems that naturally degrade over time
- **Low Uptime:** Lack of modularity and power/voltage scalability compromises system uptime
- **Supply Shortages:** Increased lead times (over two years) and prices due to heavy reliance on copper and labor-intensive manufacturing

Solid State Transformers : Revolutionizing Power Delivery



	MVAC Grid	DC Load / Generation
Utility-Scale BESS	34.5kVAC 24.5kVAC 13.8kVAC	1500VDC to 2400VDC
Utility-Scale Solar		1500VDC to 2000VDC
Data Center Power Delivery		800VDC ; Future 1500VDC
EV Megawatt Charging		1000VDC to 1250VDC

Line Frequency Transformer (LFT)

Medium Frequency Transformer (MFT in SST)

Power Density	< 1 kW / l	> 15 kW / l
Frequency	50/60 Hz	> 100 kHz

Benefits of Solid State Transformer (SST):

- ❑ Single-stage AC/DC or DC/AC conversion
- ❑ Up to 1% - 2% efficiency improvement
- ❑ Over 10x reduction in size
- ❑ Modular and scalable for voltage/power
- ❑ Higher up-time (> 99%)
- ❑ Up to 50% faster construction time

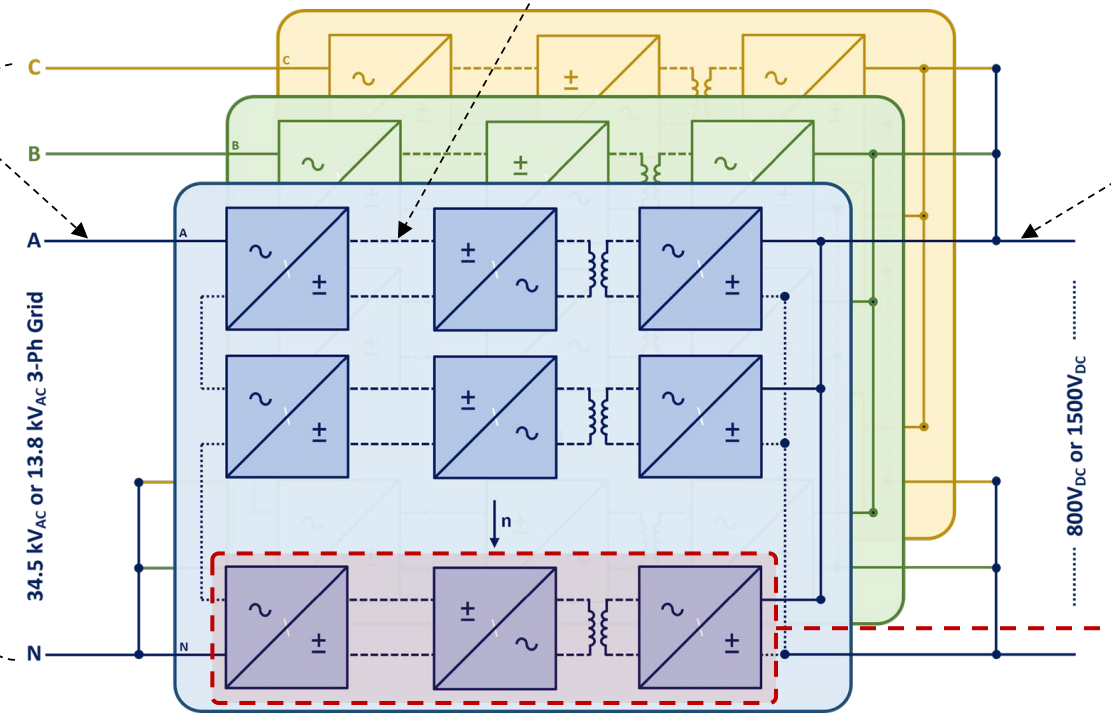
Solid State Transformer : System Overview

AC Voltage *(per Sub-System)*
- ❑ ~ 0.5 kV_{AC}
- ❑ ~ 1.1 kV_{AC}
- ❑ ~ 1.5 kV_{AC}

DC Voltage *(per Sub-System)*
- ❑ 800 V_{DC}
- ❑ 1500 V_{DC} to 1800 V_{DC}
- ❑ 2000 V_{DC} to 2400 V_{DC}

Output Voltage *(per Sub-System)*
- ❑ 800 V_{DC} (AI Data Center)
- ❑ 1000 V_{DC} to 1250 V_{DC} (EV Charging)
- ❑ 1500 V_{DC} to 2000 V_{DC} (Utility-Scale Solar)
- ❑ 1500 V_{DC} to 2400 V_{DC} (Utility-Scale BESS)

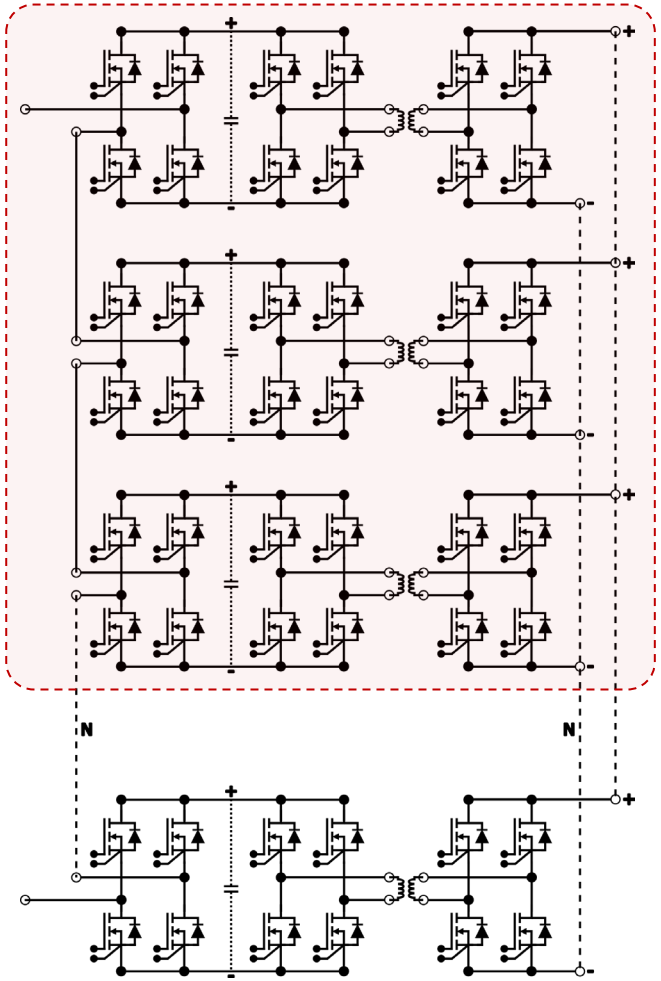
MVAC Grid
- ❑ 13.8 kV_{AC} *(3-Ø L-L)*
- ❑ 24.5 kV_{AC} *(3-Ø L-L)*
- ❑ 34.5 kV_{AC} *(3-Ø L-L)*



Converter Cell *(Sub-System)*
- ❑ 40 kW to 400 kW per Cell
- ❑ ISOP Inter-Connection
- ❑ 1 MW to 8 MW per SST
- ❑ 1x AC-DC *(ex: AFE)*
- ❑ Hard-Switched *(< 10 kHz)*
- ❑ 1x Isolated DC-DC *(ex: DAB)*
- ❑ Soft-Switched *(< 150 kHz)*

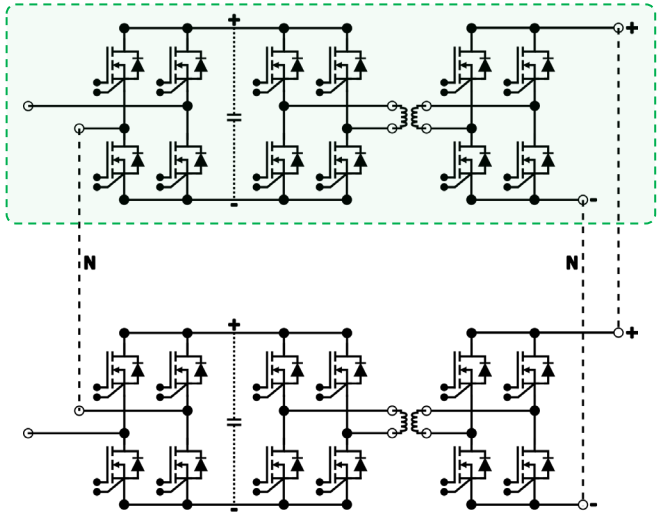
High-Voltage SiC : Key Enabling Technology for SST

1200V SiC-Based Cell Architecture



Over 50% reduction in number (N) of series-connected power converter cells enabled by high-voltage SiC (> 2kV) …

3300V SiC-Based Cell Architecture



Number (N) of Cells in Series per Phase			
	13.8kV$_{AC}$	**24.5kV$_{AC}$**	**34.5kV$_{AC}$**
1.2kV SiC	16	28	40
2.3kV SiC	8	14	20
3.3kV SiC	6	10	14
6.5kV SiC	3	5	7
⋮	⋮	⋮	⋮

Benefits of High-Voltage SiC (> 2kV) :

- ❑ > 50% reduction in series-connected cells
- ❑ Lower BOM count
- ❑ Less complex system design
- ❑ Higher system power density

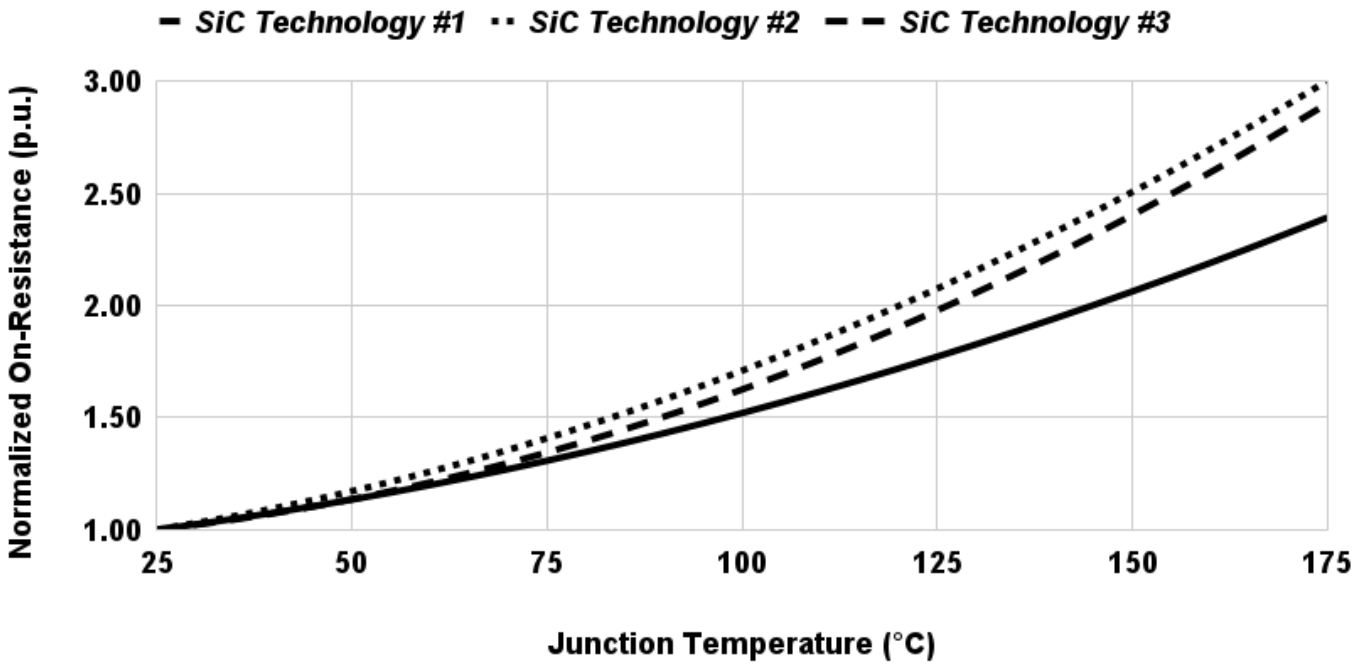
Optimizing High-Voltage SiC for Efficiency

Active Front End (AFE)

- ❑ Hard-switched
- ❑ < 5 kHz switching frequency typically
- ❑ Dominated by conduction loss

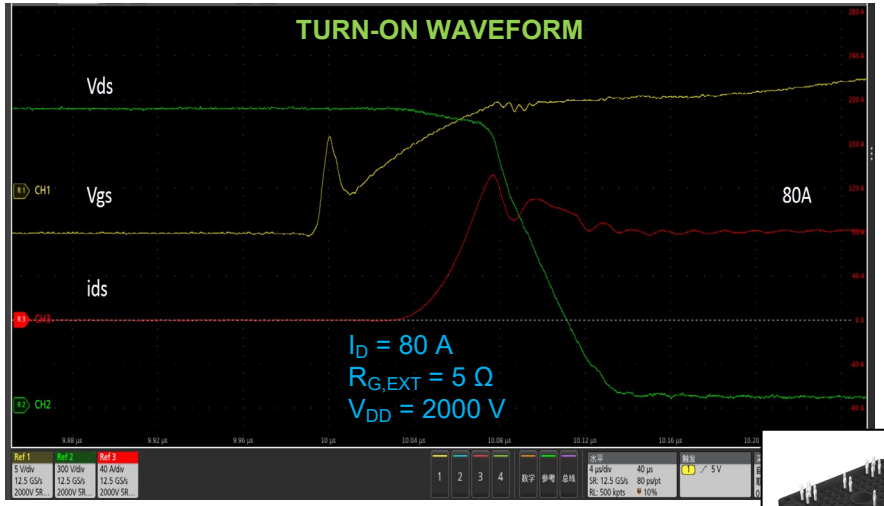
Dual Active Bridge (DAB)

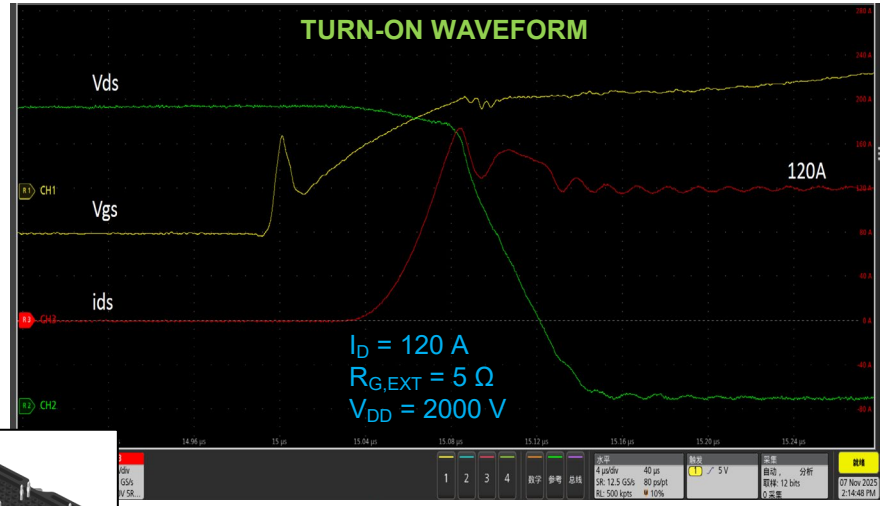
- ❑ Soft-switched
- ❑ < 150 kHz switching frequency typically
- ❑ Dominated by conduction loss

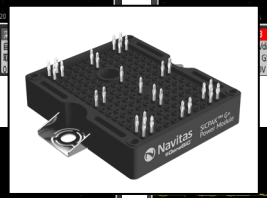


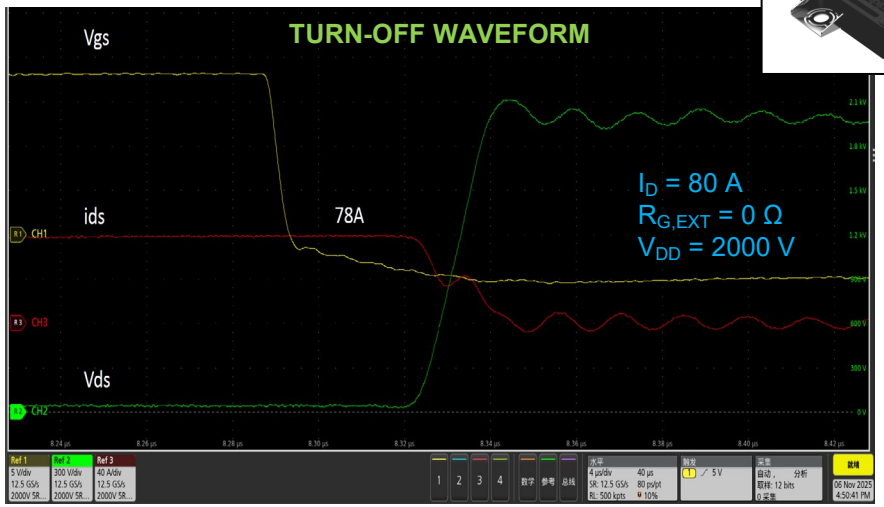
- ❑ Different high-voltage SiC MOSFET technologies exist in the market – large differences in temperature coefficient of on-state resistance ($R_{DS,ON}$ vs. T_J)
- ❑ Selecting the right high-voltage SiC MOSFET technology with low on-state resistance across a wide temperature range helps optimize efficiency

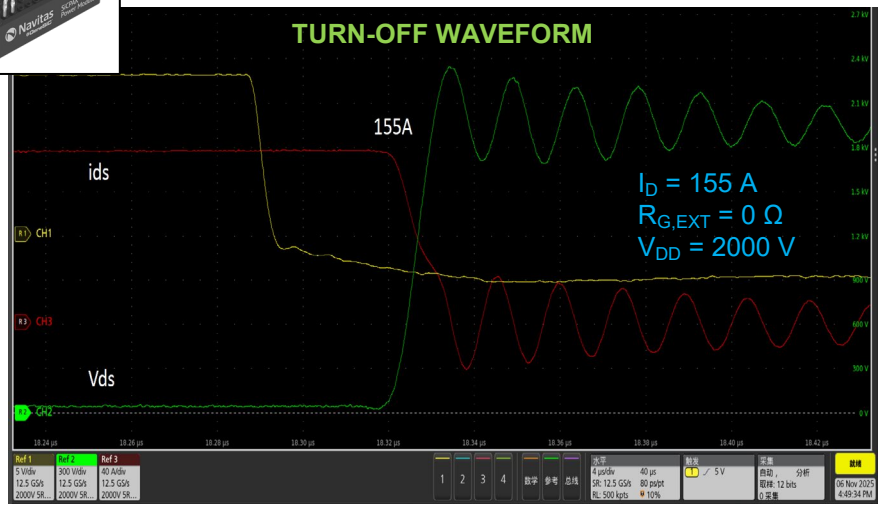
3300 V 100 A SiC Power Module Switching Performance











3300V 100A SiC Power Module Switching Waveforms (DPT)

2000V / 80A Switching

- ❑ Turn-on dI/dt = Up to 11.5 A/ns
- ❑ Turn-off dV/dt = Up to 130 V/ns

2000V / 120A Switching

- ❑ Turn-on dI/dt = Up to 14 A/ns
- ❑ Turn-off dV/dt = Up to 160 V/ns

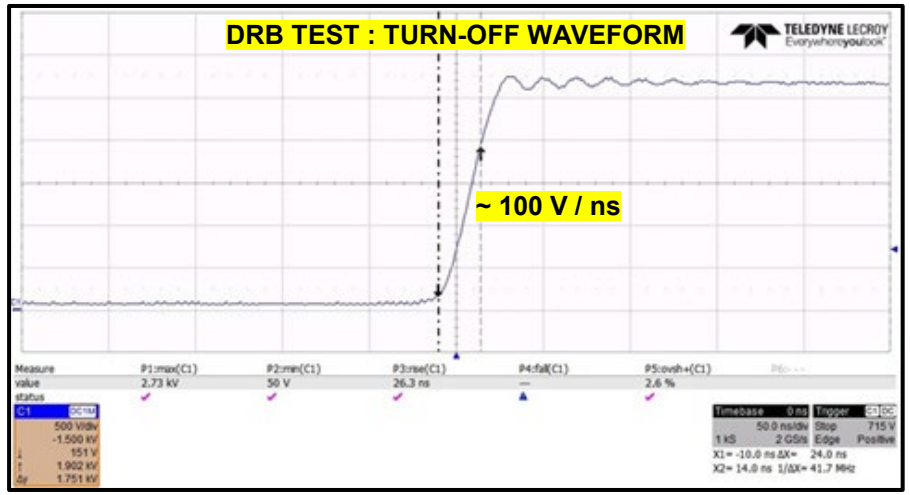
3300 V SiC Dynamic Reverse Bias (DRB) Reliability Test

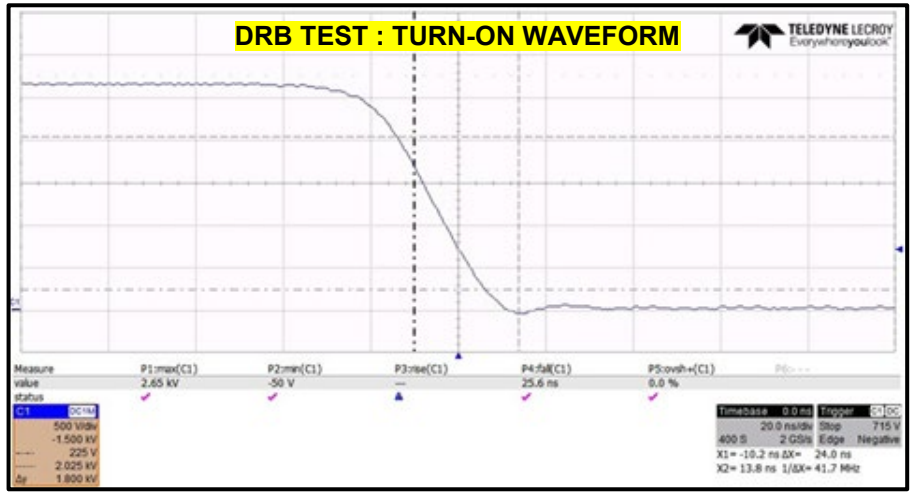
Reliability Validation for Repetitive High dV/dt

- Switching loss optimization at high operating frequencies (ex: 100 kHz) requires driving high-voltage SiC MOSFETs at turn-off dV/dt typically in 50 V / ns to 100 V / ns range
- dV/dt robustness validated through DRB testing

DRB Test Conditions

- $V_{DS,static}$ = 2640 V (80 % of $V_{DS,max}$)
- $V_{GS,static}$ = +20 V / -5 V
- $f_{switching}$ = 20 kHz
- dV/dt $_{turn\text{-}off}$ = 100 V / ns
- Monitored parameters = I_{DSS} , I_{GSS} , $V_{BV,DSS}$, $V_{GS,TH}$, $R_{DS,ON}$
- Test duration = 1000+ hours
- Pass criteria = shifts permissible as per AQG-324
- Accelerated testing (challenging test setup and BOM !)
  - $f_{switching}$ > 20 kHz
  - dV/dt $_{turn\text{-}off}$ = 100 V / ns to 200 V / ns





Energy-Infrastructure Demands 20+ Years Reliability

JEDEC		
Test	**Condition**	**Duration**
HTRB	80% V_{DS}	1000 hours
HTGB	Max. V_{GS-ON}	1000 hours
HTGB-R	Max. V_{GS-OFF}	1000 hours
TC	-55°C to 150°C	1000 cycles
IOL (PC_{MIN})	$\Delta T_J \geq 100°C$	10,000 cycles

+ relaxed parametric-shift criteria

AEC		
Test	**Condition**	**Duration**
HTRB	100% V_{DS}	1000 hours
HTGB	Max. V_{GS-ON}	1000 hours
HTGB-R	Max. V_{GS-OFF}	1000 hours
TC	-55°C to 150°C	1000 cycles
IOL (PC_{MIN})	$\Delta T_J \geq 100°C$	10,000 cycles
H3TRB	100V V_{DS}	1000 hours

+ stringent parametric-shift criteria

AEC-PLUS		
Test	**Condition**	**Duration**
HTRB	100% V_{DS}	2000 hours
HTGB	Max. V_{GS-ON}	2000 hours
HTGB-R	Max. V_{GS-OFF}	2000 hours
TC	-55°C to 150°C	3000 cycles
IOL (PC_{MIN})	$\Delta T_J \geq 100°C$	30,000 cycles
HV-H3TRB	80% V_{DS}	1000 hours
DRB	80%/100% V_{DS}	1000 hours
DGS	Max. V_{GS}	1000 hours

+ stringent parametric-shift criteria

Stringent Reliability Testing of High-Voltage SiC

Comprehensive reliability testing at SiC die level and SiC power module level …

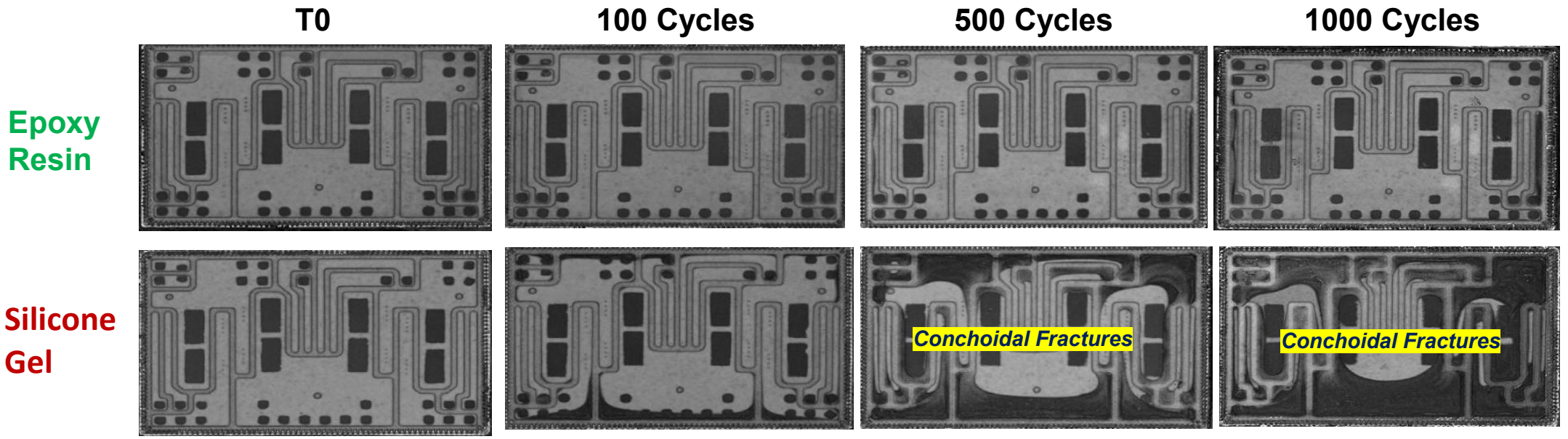
Switching Reliability Tests	**Test Conditions**	**'AEC-Plus' Grade**
Dynamic Reverse Bias (DRB)	$V_{DS,st}$ = 80% , $V_{DS,tr}$ = 90% - 100% , >20kHz , >100V/ns	1000 hr
Dynamic Gate Stress (DGS)	$V_{GS,st}$ = +22.5/-10V , >500kHz , >1V/ns	1000 hr
Dynamic H3TRB (D-H3TRB)	$V_{DS,st}$ = 80% , $V_{DS,tr}$ = 90% - 100% , >25kHz , >100V/ns	1000 hr

Static Reliability Tests	**Test Conditions**	**'AEC-Plus' Grade**
HTGB and HTGB-R	$V_{GS,st}$ = +22.5V & -10V , 175°C , V_{DS} = 0 V	2000 hr
LTGB and LTGB-R	$V_{GS,st}$ = +22.5V & -10V , -55°C , V_{DS} = 0 V	1000 hr
HTRB	$V_{DS,st}$ = 100% , 175°C , V_{GS} = 0 V	2000 hr
LTRB	$V_{DS,st}$ = 100% , -55°C , V_{GS} = 0 V	1000 hr
HV-H3TRB	$V_{DS,st}$ = 80% , T_a = 85°C , RH 85%	1000 hr

Improving Package Technology for Longer Lifetime

Reliability Improvement Area	Epoxy-Resin Potting Technology	Silicone-Gel Fill Technology
Thermal Shock Test (-40°C to 125°C)	>3000 cycles	<250 cycles
Temperature Cycling (-55°C to 150°C)	>3000 cycles	<250 cycles
Power Cycling (PC_{sec})	+65% lifetime improvement	-
Temperature Humidity Bias (THB / HV-H3TRB)	Improved	-

Module Technology Lifetime Validation : Thermal Shock

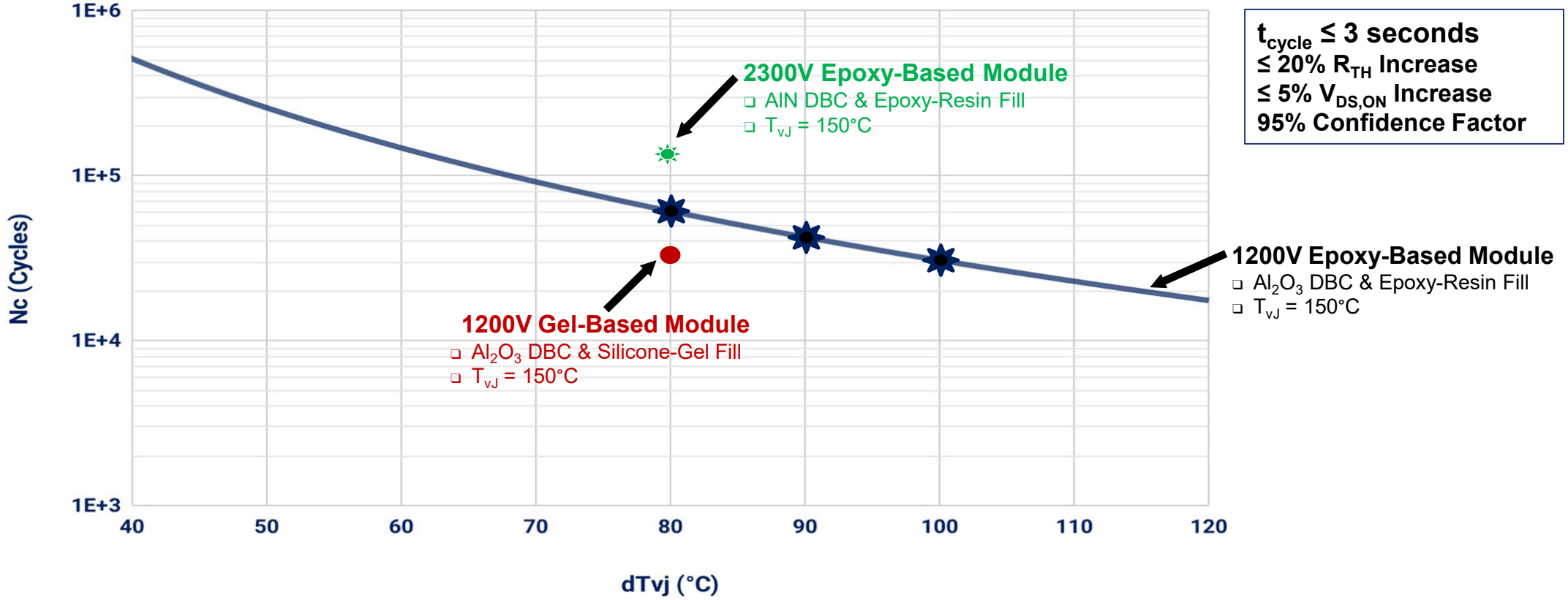


Results* after <u>1000 cycles of Thermal Shock Testing (-40°C to 125°C)</u>

✓ <15% thermal resistance increase for epoxy-resin vs. 33%-80% R_{th} increase for silicone-gel
✓ All epoxy-resin potted modules passed isolation tests ; all silicone-gel modules failed isolation test

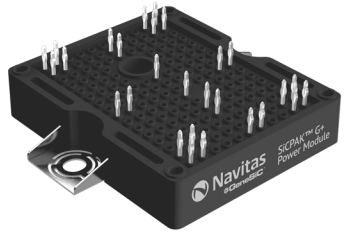
** actual test data comparison based on 1200V SiC power modules with Al_2O_3 DBC assembled with different potting technology methods*

Module Technology Lifetime Validation : Power Cycling



- ✓ **>500k Power cycles at dT_J = 40°C for Al_2O_3 DBC based epoxy-resin potted module**
  - **Epoxy-resin potting technology enabled over 65% longer lifetime compared to silicone-gel**
- ✓ **Additional 60% lifetime improvement by changing BOM from Al_2O_3 DBC to AlN AMB**

Navitas High-Voltage SiC Module Portfolio for SST



SiCPAK™ G+ (56.7mm x 65mm)

Voltage	Package	Configuration	$R_{DS,ON}$ per Switch	Part Number	Status
3300V	SiCPAK™ G+	Full-Bridge	22.5 mΩ	G4H22MT33GB4	Sampling Now
2300V		Half-Bridge	5.8 mΩ	G4H06MT23GB2	Sampling Now
		Full-Bridge	11.5 mΩ	G4H11MT23GB4	Sampling Now
		Full-Bridge	8 mΩ	G4H08MT23GB4	Sampling Now
1200V	SiCPAK™ G	Half-Bridge	4.6 mΩ	G3F05MT12GB2	In Production
1200V	SiCPAK™ G	Full-Bridge	9.3 mΩ	G3F09MT12GB4	In Production

+ more modules in development …

Authors' Names and Affiliations
(Optional: Contact Information)