



New-Generation of Trench-Assisted Planar SiC MOSFETs

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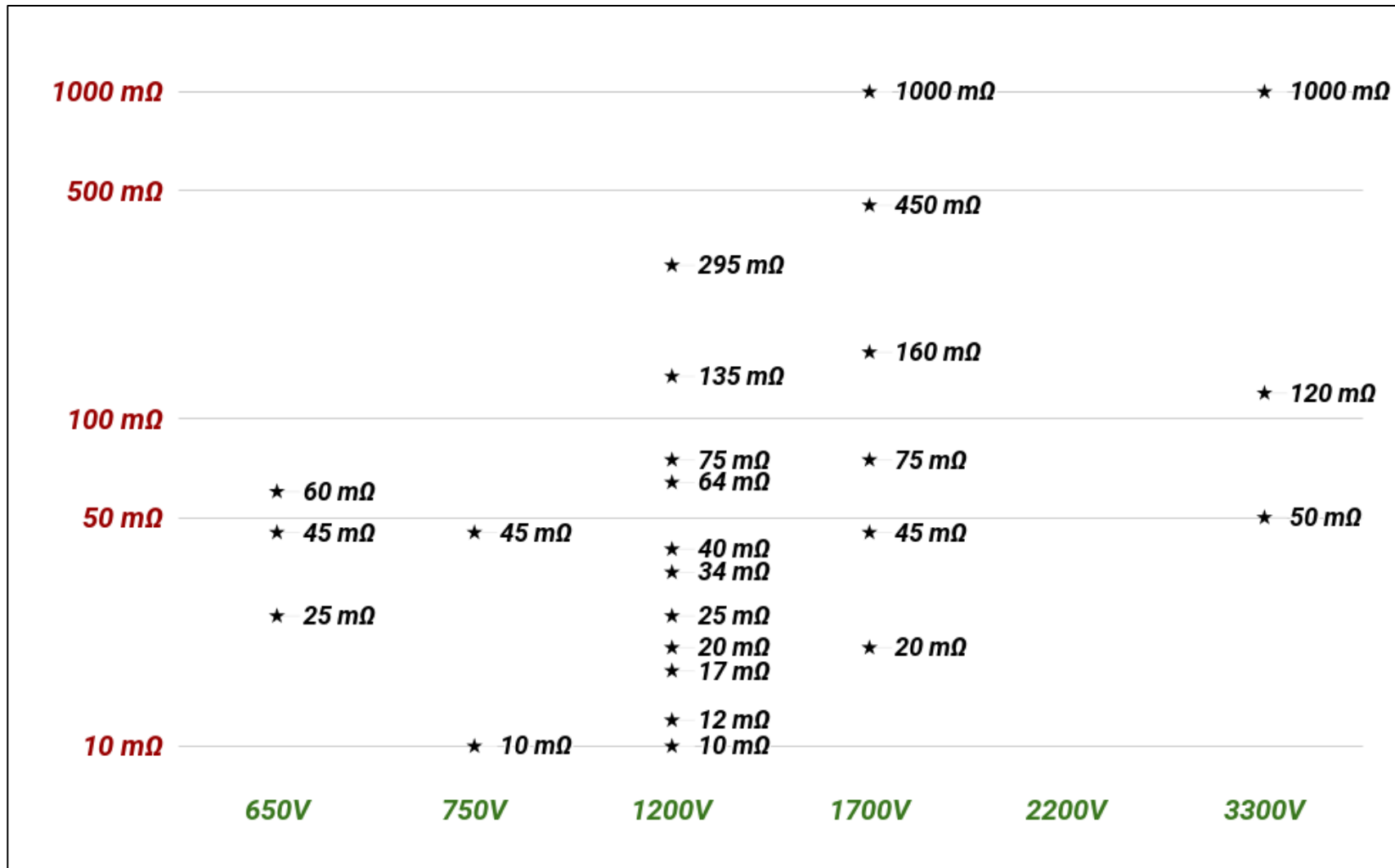
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Broadest SiC MOSFET Portfolio

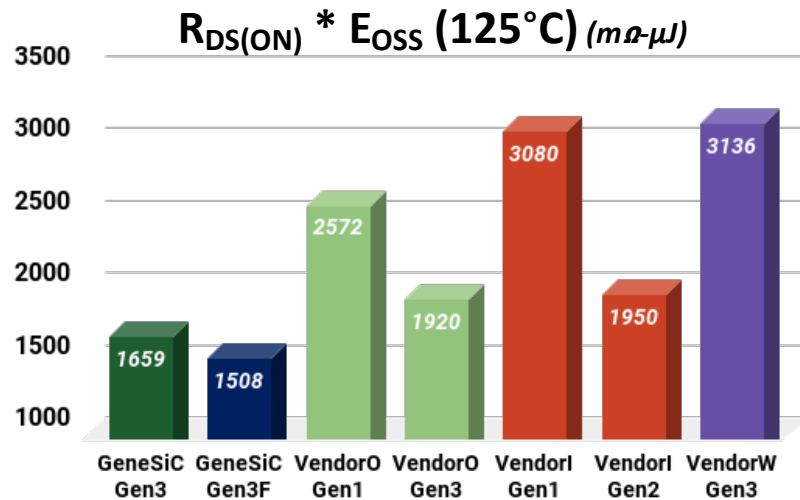


- ✓ 60+ SiC MOSFET products
- ✓ Discrete
- ✓ Bare Die
- ✓ Power Modules



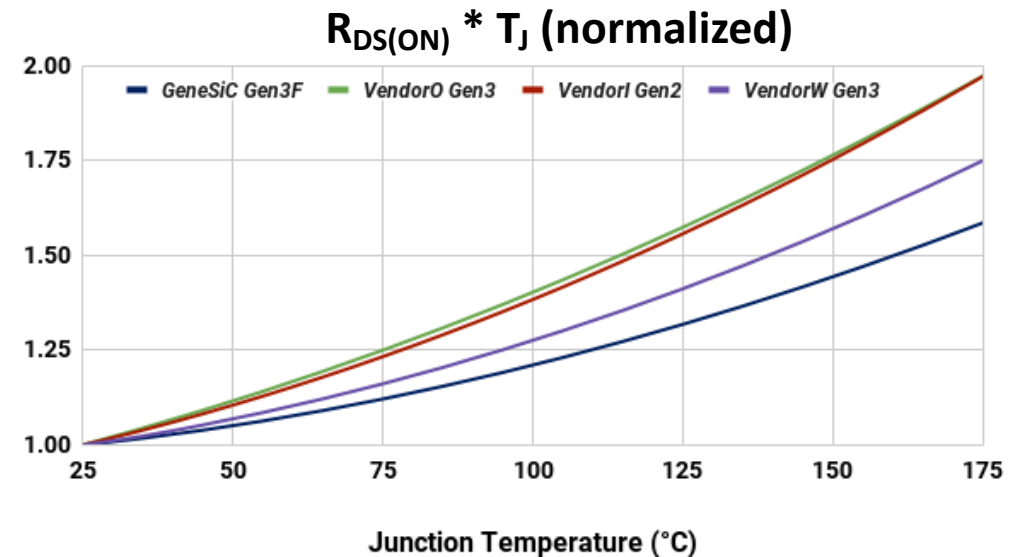
Note (1): based on GeneSiC voltage range of production released SiC MOSFETs compared to all publicly identified voltage ranges of other SiC suppliers.

- Traditional designs using planar or trench techniques, which must compromise between manufacturability, performance, and/or reliability.
- GeneSiC trench-assisted planar-gate technology enables leading-edge performance with high-yielding manufacturing.



Lowest switching FoM ($R_{ON} * E_{OSS}$) when compared to other planar & trench technologies

Gen3F at 125°C
 21% lower than vendor-O (Gen3)
 51% lower than vendor-W (Gen3)
 22% lower than vendor-I (Gen2)



22kW OBC + 3kW DC-DC Combo
 Bi-Directional; SiC-based 1-φ & 3-φ Compatibility

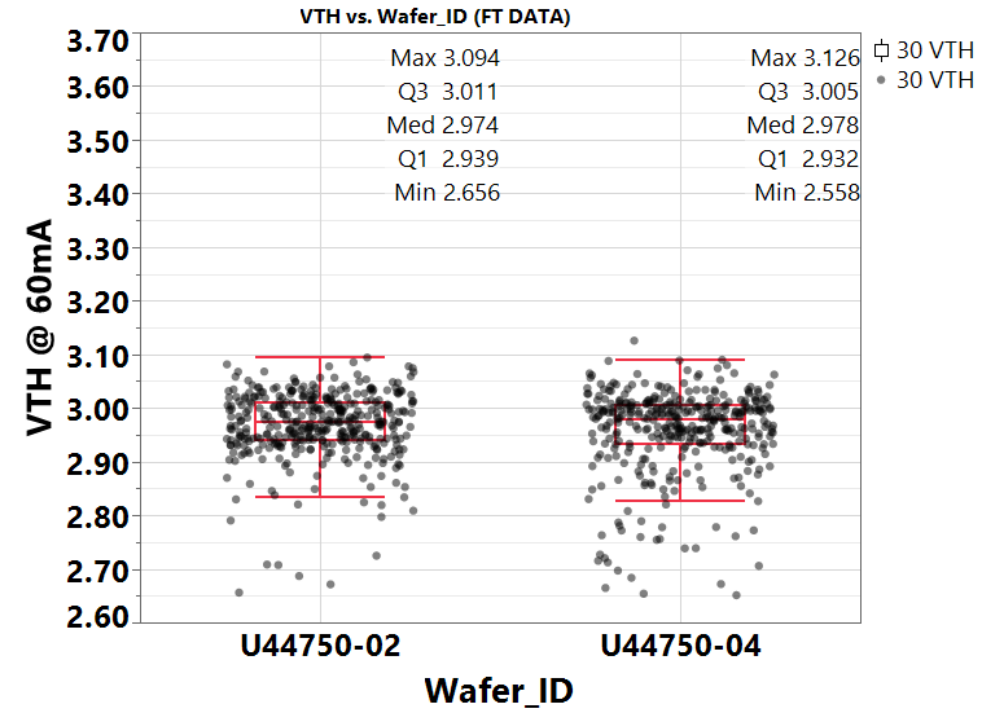
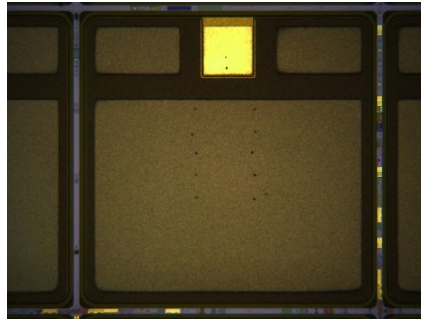
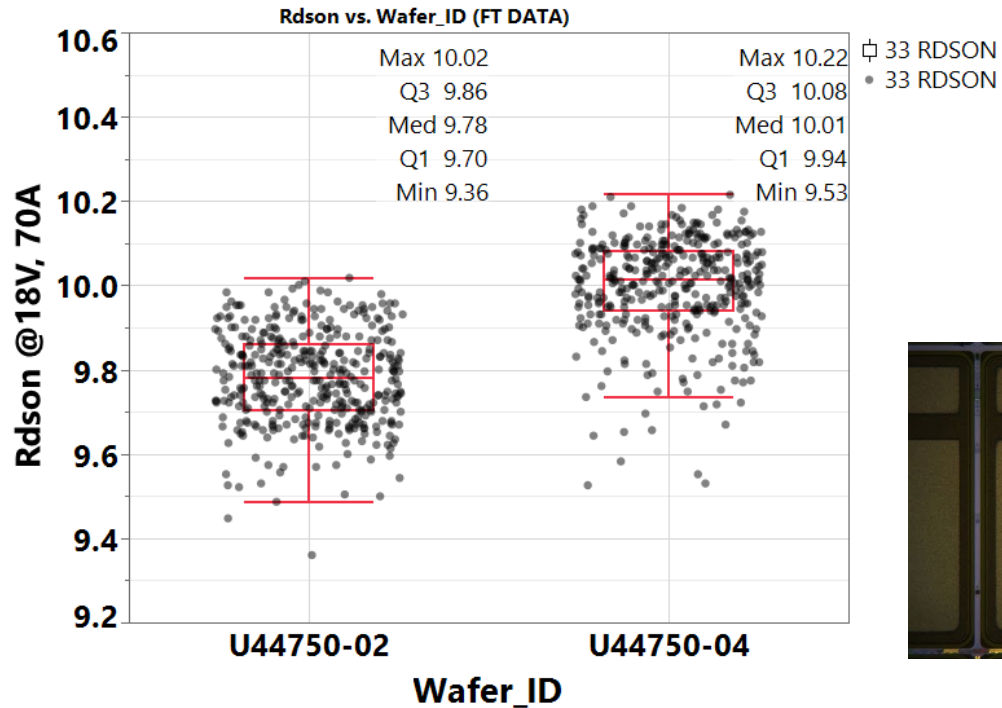


G3R40MT12K
 1200V 40mΩ TO-247-4

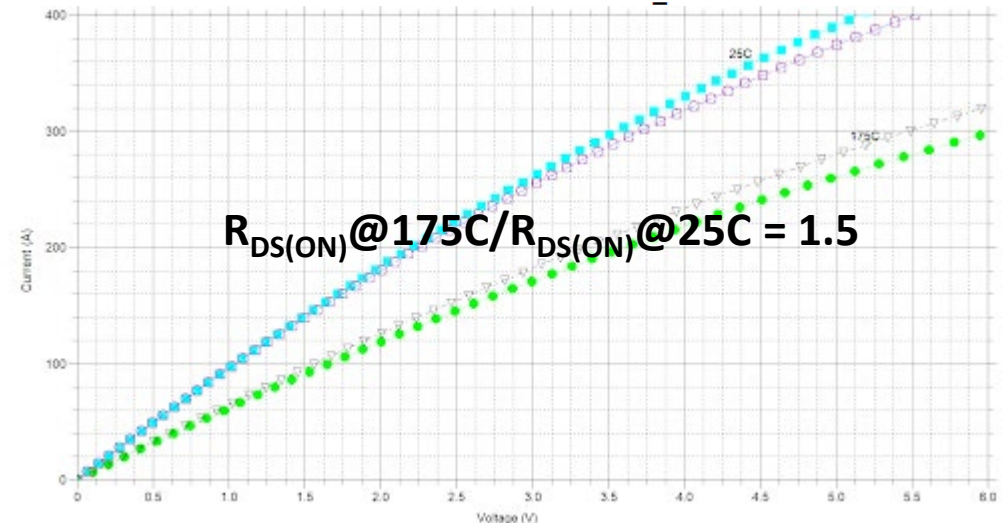
1200V G3 / G3F Fast SiC MOSFET
>95% Efficiency @ Full Load

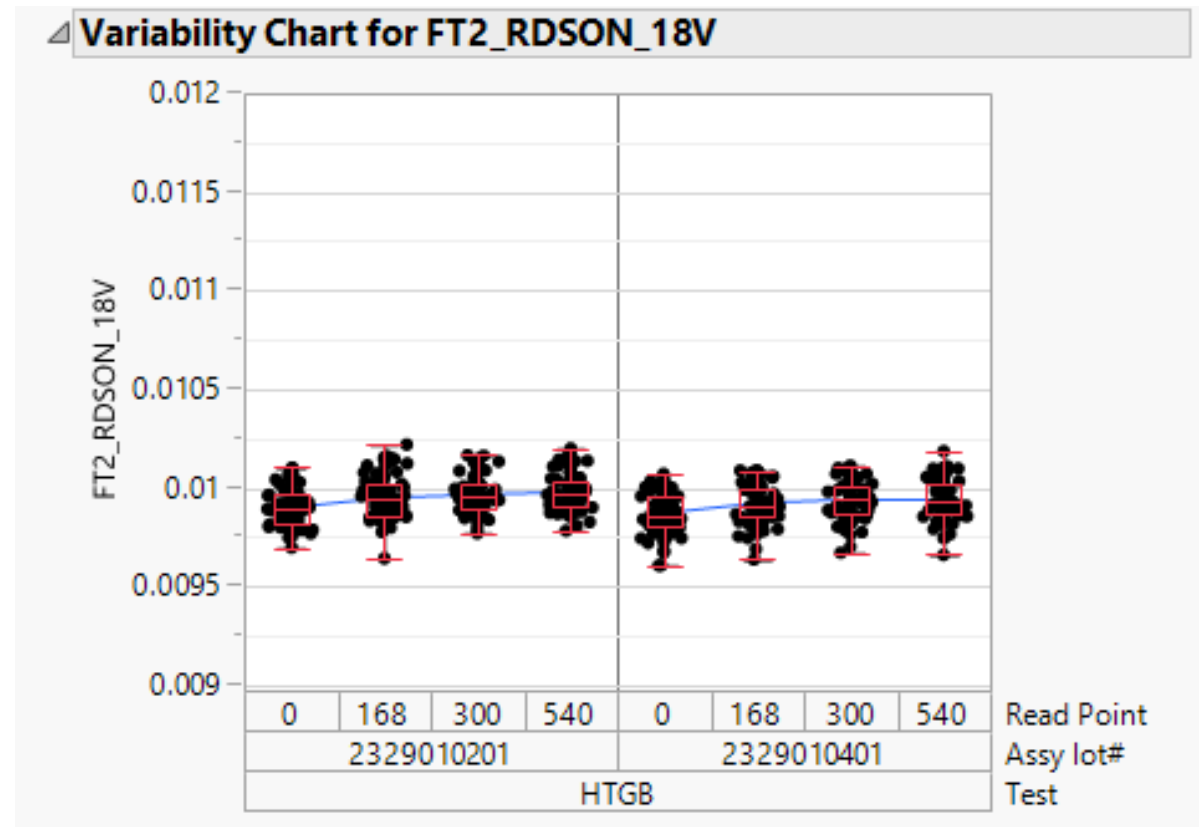
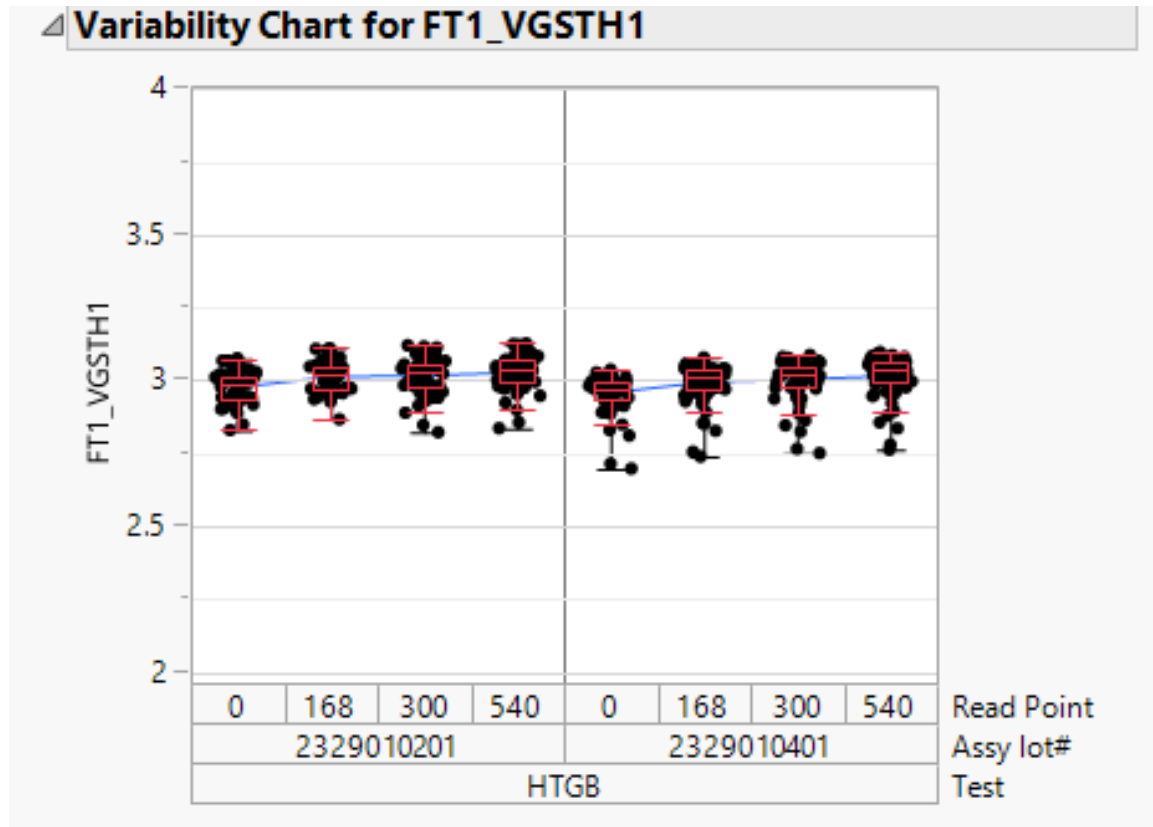
All data based on 1200V 40mΩ - 45mΩ production parts

New-Generation 750 V SiC MOSFETs



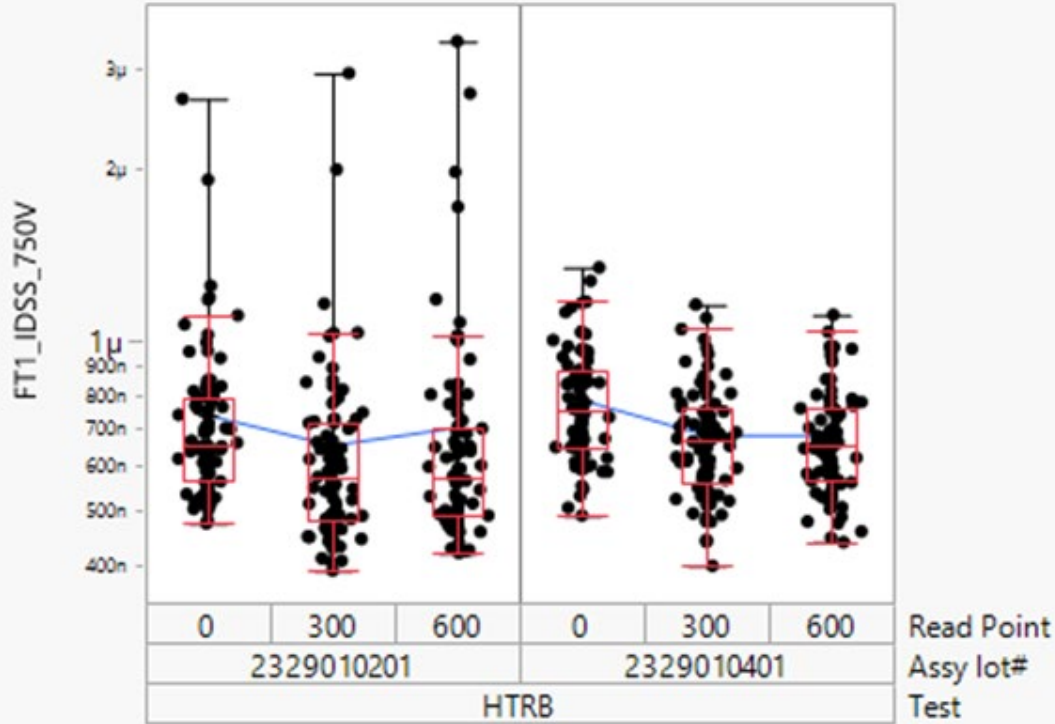
- T5 mm x 5 mm chips with (optional) solderable top metal
- Extremely tight $R_{DS(ON)}$ (10 mOhm) and V_{TH} (3.0 V) distributions across wafers



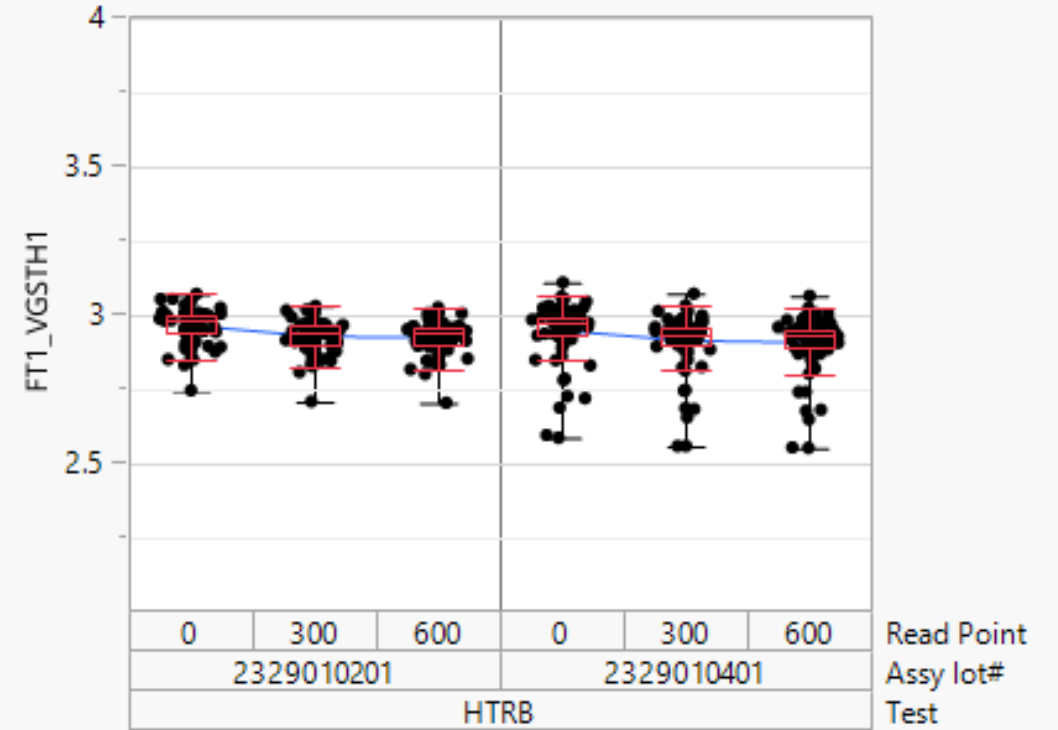


- Vgs +22 V stress applied at 175°C
- Less than 3% V_{TH} variation observed after 540 hours

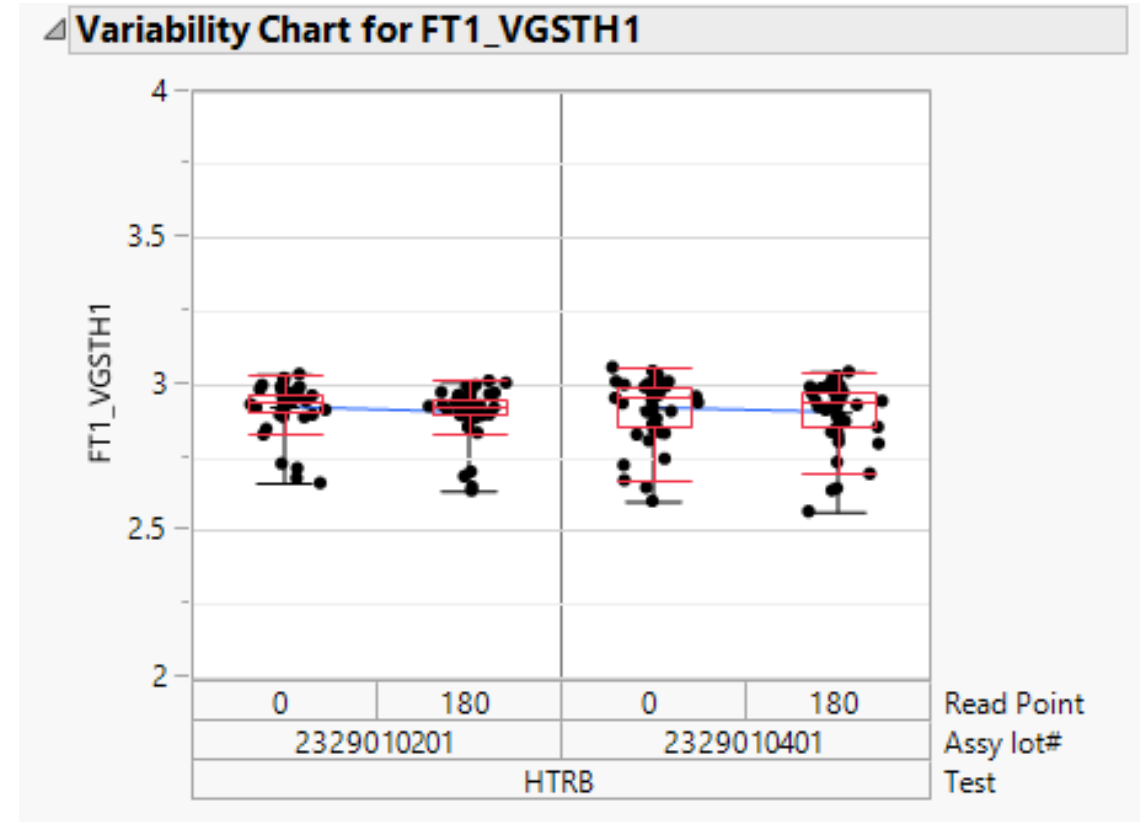
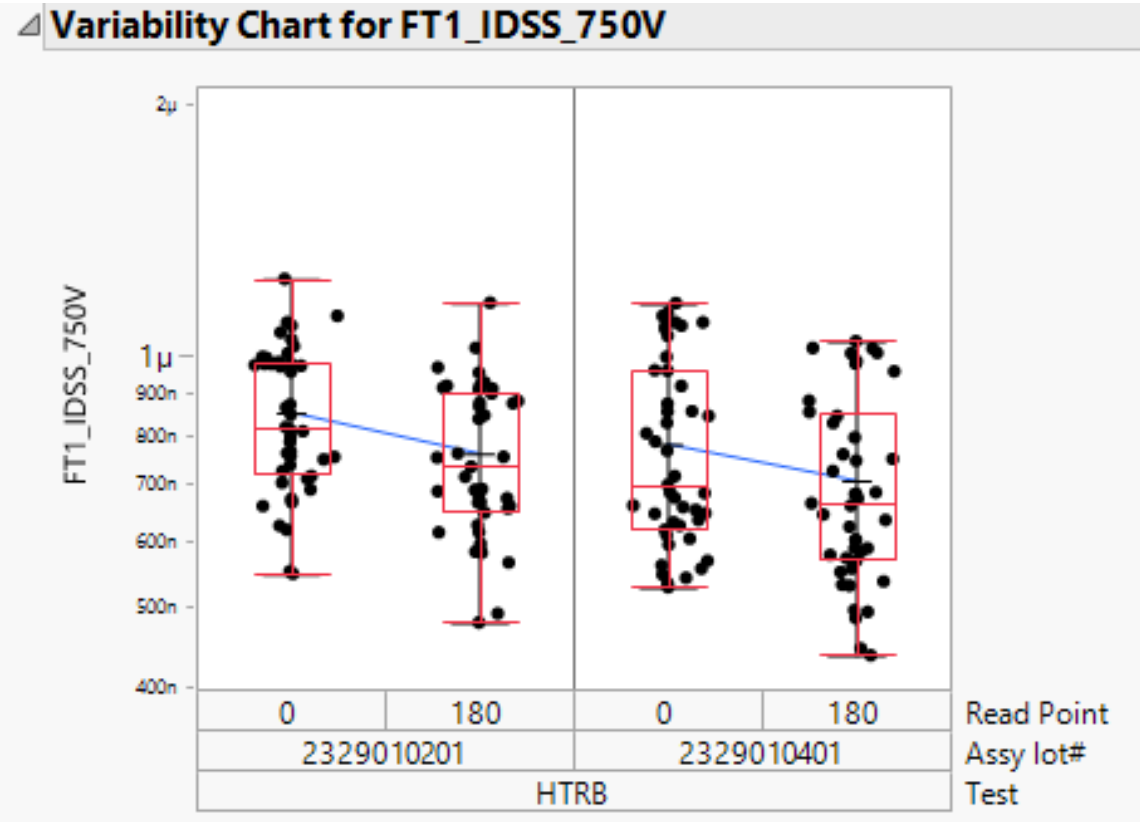
▲ Variability Chart for FT1_IDSS_750V



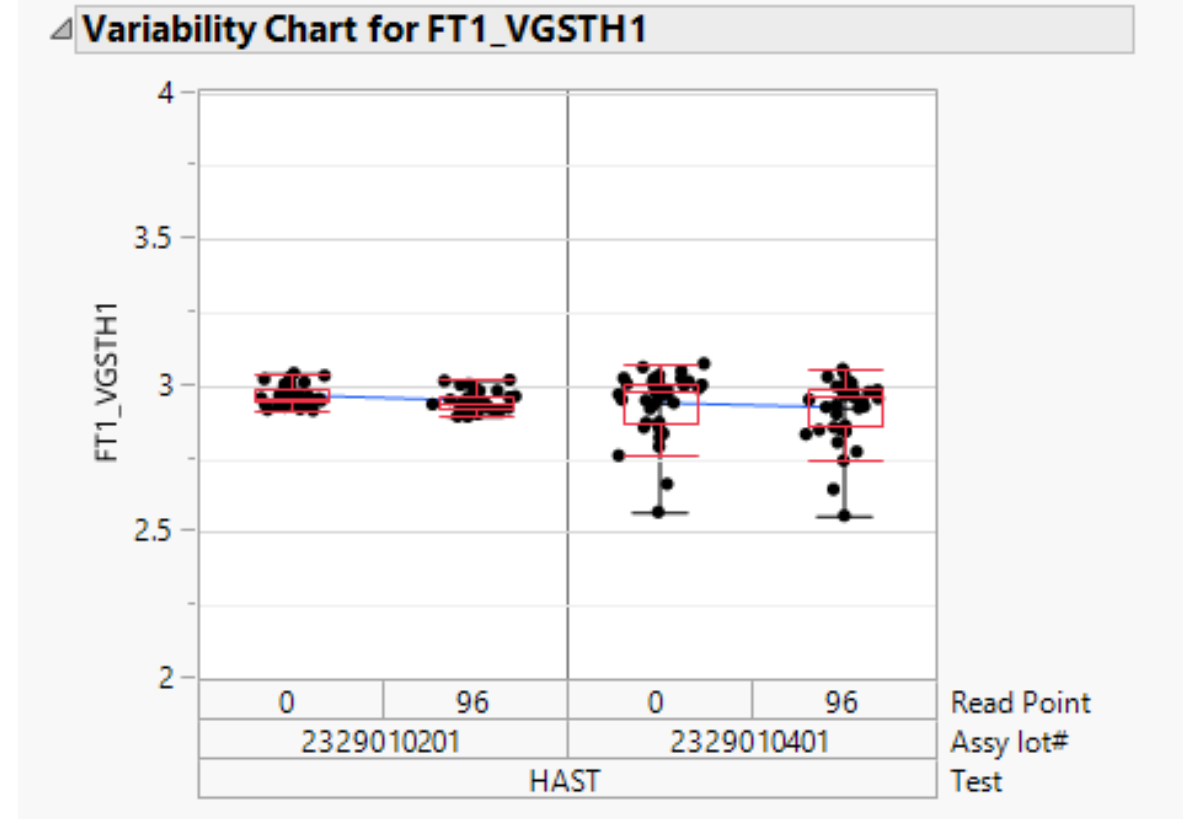
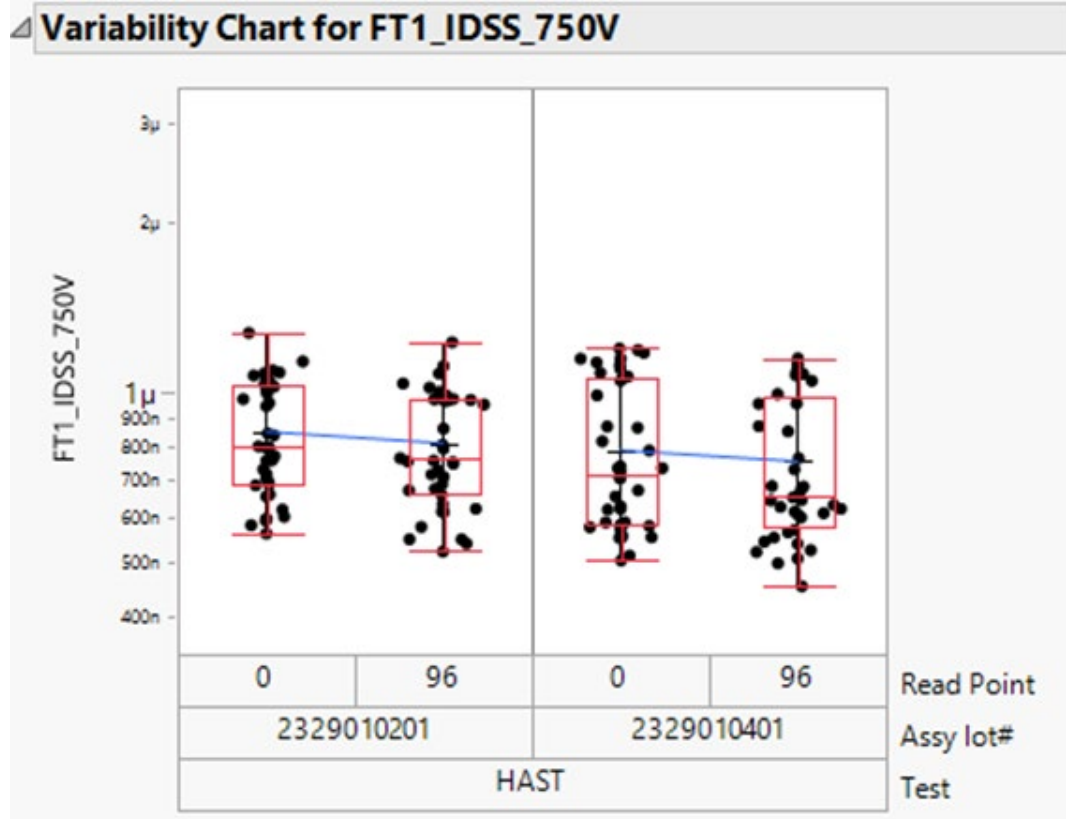
▲ Variability Chart for FT1_VGsth1



- Minimal Idss or V_{TH} shift observed during 750 V/175°C HTRB stress



- Excellent parameter stability observed even under accelerated HTRB stress



- Excellent robustness of key parameters under 96 hour accelerated humidity stress conditions

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