Next-generation GaN Isolators / Level-Shifters for High Frequency, High Efficiency Power Conversion

PSMA Industry Session, Isolation Barrier Technologies for Power Electronics

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Scope: The Half-Bridge Challenge

- **Half-Bridge Topologies:**
  - Active Clamp Flyback (25-65W)
  - LLC (90-400W+)

- **Switching Frequency** 100 kHz – 1 MHz+

- **Functional (not galvanic) isolation** (650 V)

- **Function** (uni-directional)
  - High-side Power
  - High-side Signal

- **Normalized to** 160 mΩ, 2.5 nC $Q_G$, eMode GaN FETs
  - Focus on driver, level-shifter influence
Level-Shift Performance → System Size, Cost

- **Efficiency**
  - Level-shift (driver) loss
  - Propagation delay loss

- **Speed**
  - Propagation delay
  - Switching frequency

- **Noise**
  - Common Mode Transient Immunity (CMTI) ($dV/dt$)

- **Features**
  - Protection (shoot-through, ESD, UVLO, etc.)
  - Programmability

- **Cost**
  - Integration, component count, magnetics size
A Note on Prop Delay

- Traditional ‘discrete’ level-shifter
  - Measured from the incoming PWM_H signal to a 10% change in the level-shifter’s own output
  - No account for FET speed, $R_G$, $Z_G$, etc.

- Integrated GaN Power IC
  - Measured from PWM_H signal to a 10% change in high-side FET $V_{DS}$
  - Complete accountability
# High-Frequency Level-Shift Candidates

<table>
<thead>
<tr>
<th>Silicon-On-Insulator (SOI)</th>
<th>Capacitive-Coupled</th>
</tr>
</thead>
<tbody>
<tr>
<td>e.g. IR2113, UCC21521</td>
<td>e.g. Si8610</td>
</tr>
</tbody>
</table>

- **Silicon-On-Insulator (SOI)**
  - e.g. IR2113, UCC21521

- **Capacitive-Coupled**
  - e.g. Si8610

<table>
<thead>
<tr>
<th>Inductive-Coupled</th>
<th>GaN Power IC</th>
</tr>
</thead>
<tbody>
<tr>
<td>e.g. ADuM1234, ADuM3223, BM60210FV-C, 2ED020I06</td>
<td>e.g. NV62xx</td>
</tr>
</tbody>
</table>

### Representative images, not to scale

- Silicon-On-Insulator (SOI)
- Capacitive-Coupled
- Inductive-Coupled
- GaN Power IC
Discrete Half-Bridge Drive: 5 Losses

1. Level-shift loss = \( f(Q_{LS}, F_{SW}, V_{BUS}) \)
2. FET gate-charge loss = \( f(Q_{G}, F_{SW}, V_{CC}) \)
3. Quiescent loss = \( f(V_{CC} \times I_{QCC}, V_{BS} \times I_{QBS}) \)
4. Gate-loop loss = \( f(L_{CS}, I_{OUT}, F_{SW}) \)
5. Bootstrap diode loss = \( f(C_{B-S \ Diode}, Q_{rr}, F_{SW}) \)
Start with the single GaN Power IC

- Proprietary AllGaN™ technology
- Monolithic integration
- 650 V, eMode, GaN FET, GaN driver, GaN logic
- Very fast (prop delay and turn-on/off of 10-20 ns)
- High dV/dt immunity (200 V/ns) with control
- Digital in, power out...

Gate-Loop Loss $= fn(L_{CS}, I_{OUT}, F_{SW})$

- Common source inductance loss
- Damping resistor needed to reduce oscillation, voltage spike at the FET gate

\[
R_{damp} \geq \sqrt{\frac{4(L_g + L_s)}{C_{gs}}}
\]

<table>
<thead>
<tr>
<th>$L_g + L_s$ [nH]</th>
<th>$R_{damp}$ [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>2.83</td>
</tr>
<tr>
<td><strong>2</strong></td>
<td><strong>4</strong></td>
</tr>
<tr>
<td>3</td>
<td>4.9</td>
</tr>
<tr>
<td>4</td>
<td>5.66</td>
</tr>
</tbody>
</table>

$C_{gs} = 500\text{pF}$
Integration is Key

1. External driver: Oscillation

2. External driver + $R_G$: In control, Slow, Lossy

3. Integrated driver: In control, 10x faster, Zero loss
External drivers

- Significant turn-off losses
- Just 1-2 nH of gate loop inductance can cause voltage spikes that create unintended turn-on of the GaN FET
- Adding a gate resistor reduces spikes but slows down the circuit creating additional losses

Integrated GaN drivers (iDrive™)

- Eliminate the problem
- Negligible turn-off losses
Half-Bridge iDrive GaN Power IC

- Proprietary AllGaN™ technology
- Monolithic integration of 650V eMode GaN FET, driver, logic
- Internal level-shift, bootstrap
- Ground-referenced, digital input
- High dV/dt immunity (200 V/ns)
- Zero inductance turn-off loops
- Very fast (prop delay and turn-on/off of 20-40 ns)
- ESD, UVLO, shoot-through protection
- Flexible topologies: Active Clamp Flyback, Half-Bridge, LLC, etc.
Half-Bridge GaN Power IC at 2 MHz
Bootstrap Diode Loss = fn\left( C_{B-S\ Diode}, Q_{rr}, F_{SW}\right)

- External diode ES1J (600 V, 1 A, $V_F = 1.7$V at 1 A, SMA)
3x Lower Level-Shift Total Loss at 1 MHz

FET-specific loss (e.g. I^2R) common across all options, not included
5x Smaller, Easier

Si8610 + 2x FETs + Bootstrap + Rs, Cs

NV62xx

Size (PCB Area, mm²)

<table>
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<tr>
<th>Component</th>
<th>PCB Area [mm²]</th>
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<tbody>
<tr>
<td>SOIC, IR2113</td>
<td>350</td>
</tr>
<tr>
<td>Capacitive-coupled, UCC21521</td>
<td>300</td>
</tr>
<tr>
<td>Capacitive-coupled, Si8610BB-B-1S</td>
<td>250</td>
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<tr>
<td>Inductive-Coupled, ADuM1234</td>
<td>200</td>
</tr>
<tr>
<td>Inductive-Coupled, ADuM3223</td>
<td>150</td>
</tr>
<tr>
<td>Inductive-Coupled, BM60210FV-C</td>
<td>100</td>
</tr>
<tr>
<td>Inductive-Coupled, 2E002006</td>
<td>50</td>
</tr>
<tr>
<td>GaN, NV62xx</td>
<td>5</td>
</tr>
</tbody>
</table>
High-Frequency Half-Bridge Integration

Disparate technologies:
Hybrid isolator / driver with discrete powertrain

Homogeneous platform:
Lateral GaN-on-Si, NV6250 Half-Bridge GaN Power IC

**3 Losses**
(FET-size, $I^2R$ independent)

1) Driver loss, $R_G$ loss
2) Bootstrap supply
3) Level shifter

**Zero Losses**
(FET-size, $I^2R$ independent)

1) No gate driver loop parasitics, matched driver-FET capability, negligible loss vs frequency
2) Low equivalent $V_F$, zero $Q_{rr}$
3) Extremely fast, low-power level shifter, multi-MHz operation, short propagation delay
45W Adapter – 25 W/in³

Half-Bridge GaN IC: 63.5°C

Diode bridge: 68.1°C

59.1 x 33.5 x 15.7 mm

EN55022 Quasi-peak limit

QP measure

45W, 90VAC, no airflow, room ambient
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Additional APEC references:
Paper ID#1104, State-of-the-Art Mobile Charging: Topologies, Technologies and Performance, Tom Ribarich and Stephen Oliver (Navitas)
Paper ID#2158, Active Clamp Flyback Using GaN Power IC for Power Adapter Applications, Lingxiao Xue and Jason Zhang (Navitas)
Paper ID#1159, GaN Power ICs at 1 MHz+: Topologies, Technologies and Performance, Dan Kinzer (Navitas)
Paper ID#1117, Next-Generation GaN Isolators for High Frequency, High Efficiency Power Conversion, Stephen Oliver, Marco Giandalia (Navitas)