Parallelized Bidirectional Switches Drive Efficiency to Further Heights

By Weijing Du, Director of Applications Engineering, Navitas Semiconductor

The push for efficiency in power conversion is unrelenting. Nowhere is this more apparent than in systems that need to sustain power levels measured in hundreds of watts. Though novel power-switching topologies have greatly improved conversion efficiencies, solar inverters, heavy-duty motor drives, and other high-power systems can lose significant amounts of energy through the resistances that build up in their circuits.

The evolution of designs like grid-connected microinverters for solar generation and variable-frequency motor drives provides important examples of the architectural changes successive designers have implemented to reduce losses and maximize the use of energy.

Topology Considerations

If we first look at a conventional topology used in a microinverter. This demands several power-conversion stages to convert a high-current DC input into grid-compatible AC. That architecture suits the nature of silicon-based semiconductor technologies, which have a preferred direction for current. This leads to the use of bridge circuits, in which different half-bridge elements engage at different points of the power cycle to either rectify an AC input or invert DC to AC. Inverters based on these topologies need DC-link elements to handle the bidirectional current of an AC output, which introduces additional resistance with resultant energy losses.

A topology like the matrix converter provides a potentially more efficient alternative. This topology uses bidirectional switching to eliminate DC-link elements, each of which incurs resistance losses. Though the matrix architecture was proposed some time ago, it did not find favor because conventional silicon-based power semiconductors only support bidirectional switching to a limited extent. Parasitic paths allow some reverse conduction. For example, every silicon MOSFET contains a body diode, which allows reverse current flow. Many conventional IGBT circuits have included anti-parallel diodes to allow low levels of reverse conduction. These additional devices help the circuit deal reliably with inductive loads that would otherwise result in device damage.

Featured in Power Systems Design – March 2026

In principle, it is possible to use antiparallel diodes in combination with back-to-back silicon MOSFETs or IGBTs. But these structures introduce higher on-resistance levels than is desirable. Ideally, a monolithic device would allow bidirectional operation without increasing losses. Such a device has become possible following the development of technologies that implement high-mobility carriers such as gallium nitride (GaN). The high-electron mobility of the underlying material coupled with the use of device structures to encourage the formation of a two-dimensional electron gas naturally supports current flow in either direction through the channel when it is conducting.

GaN-Based Bidirectional Switches

Bidirectional switch (BDS) structures leverage the above properties. At the schematic level, a GaN BDS appears as two back-to-back switches. Inside the device, the two switches are arranged as separate regions joined by a common drain region. Take the Navitas NV6428 as an example. When the gates controlling both sources are at 0V, the BDS blocks current flow in both directions. The device acts as the equivalent of two diodes facing each other in series.

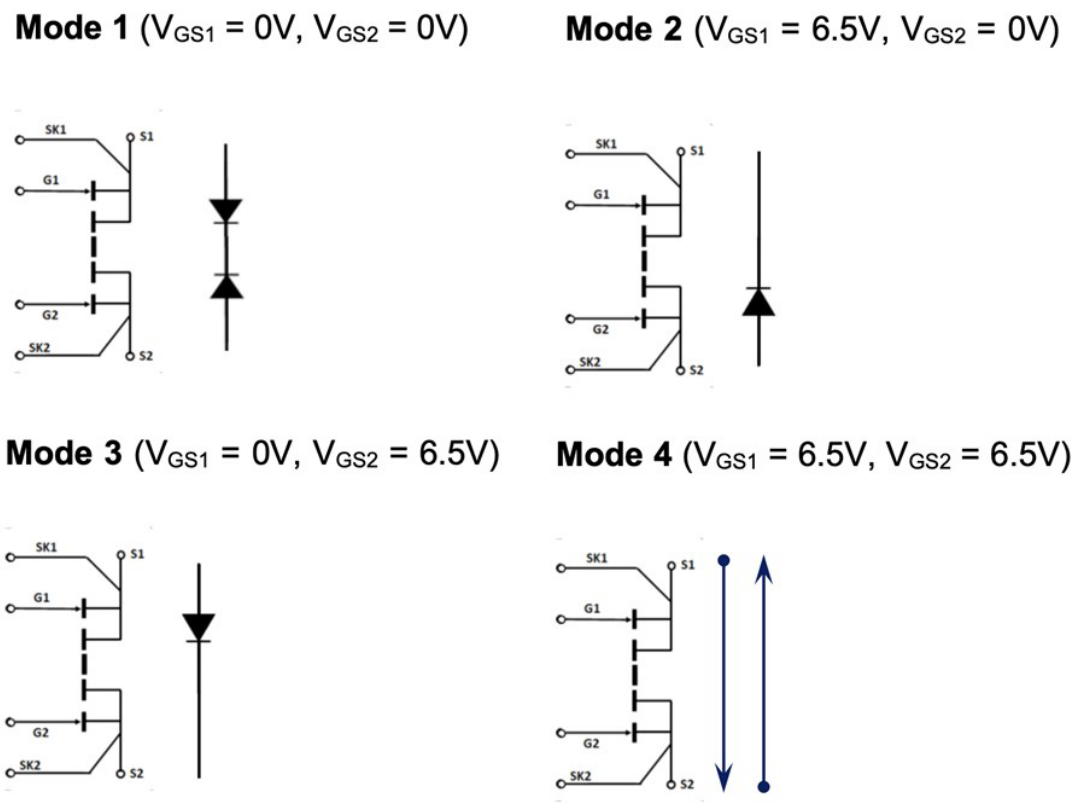

Figure 1: BDS modes

Featured in Power Systems Design – March 2026

When the voltage on one gate increases past the turn-on threshold, the BDS acts as a diode. Current can flow in one direction but not in reverse. Swapping the gate voltages allows current to flow in the opposite direction. If both gates are above the threshold voltage, current can flow equally freely in either direction.

Considerations for Device Design

There are some device-design issues that need to be considered when implementing high-performance BDS-based circuits. The substrate potential between the shared drain can change dynamically based on the different states of each source. Ideally, the substrate should be held at the lowest source voltage to prevent unwanted increases in Rds(on), which result from back-biasing or back-gating. The best solution is to employ substrate clamping between the two source regions and the common substrate. This ties the substrate voltage to the lowest source voltage, ensuring high conductivity in all modes.

A major advantage of this flexibility coupled with the low overall Rds(on) of GaN is improved performance at higher switching frequencies. Achieving similar results with silicon devices demands the use of parallel structures that are difficult to control and balance. Though BDS GaN offers lower resistance than silicon in serial circuits, paralleling brings the ability to reduce losses even further in high-current circuits.

With parallel circuits based on unidirectional devices, paralleling demands care to ensure equal loading across the individual circuit paths. Parasitic effects play a key role in determining how much current will pass through each of the parallel devices when turned on. Effects such as inductance can be problematic: they can restrict switching frequency.

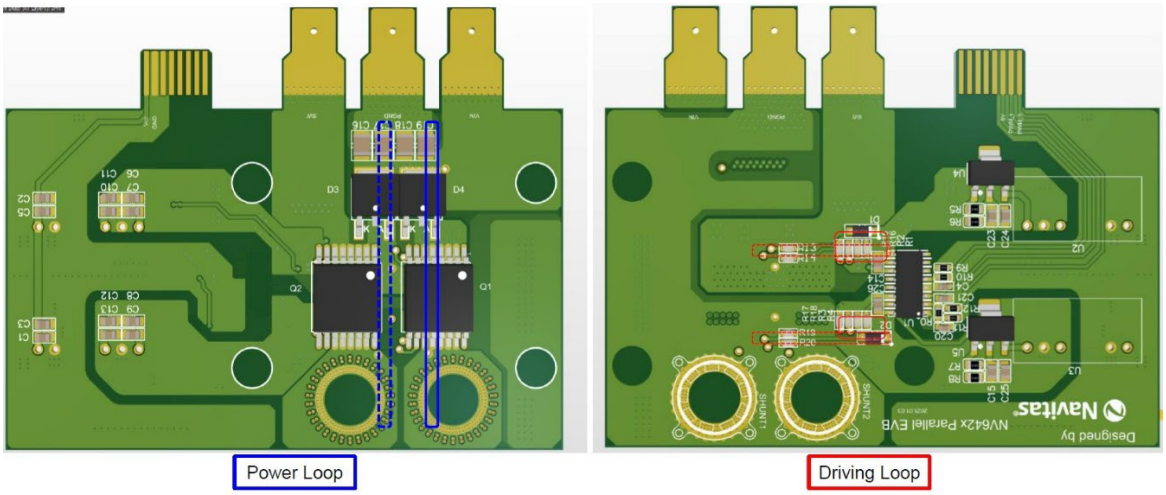

Figure 2: Example PCB layout for parallel operation highlighting the power and driving loops

Featured in Power Systems Design – March 2026

Differences in inductance caused by unequal trace lengths can lead to variations in the inevitable current oscillations caused by reverse recovery and similar effects when each device turns off. The time difference in current peaks across different devices can account for as much as 25% of the switching time. A balanced layout can reduce this effect significantly.

PCB layout is also important to BDS GaN in both serial and parallel configurations. However, tests by Navitas have shown these devices are well-behaved in parallel circuits that operate at high switching frequencies. The bidirectional nature of the switches coupled with their high conductivity up to switch-off helps reduce the oscillation effects encountered with unidirectional switches in antiparallel configurations.

To control switching behavior precisely, the use of BDS devices requires some attention to the gate-driver configuration and layout. The core recommendation is to use two floating gate driver channels to deliver PWM-generated gate drive inputs to the pair of gates on each BDS. One of the two gates may not be referenced to ground or a DC rail. Handling this situation requires a drive channel that can float to high voltage, and which can match the range of the source it is driving.

In some applications, both sources are switching nodes. Both the gate-drive outputs and the power supplies for them must be able to float to remain referenced to the source being driven. With some circuits, a ground-referenced power supply is sufficient. In other cases, an isolated floating power supply for one or both gate drives may be required.

A further recommendation is to employ isolated drivers that can turn on both gates simultaneously when bidirectional operation is needed. That should also be followed for parallel devices to prevent excessive loading on one of the paths. Similarly, optimizing the PCB to reduce the length of the power and gate-drive loops helps minimize the impact of parasitic inductance. A further consideration is the use of resistors on the gate-drive inputs and on the source-driver connections. These suppress gate ringing during switching.

Featured in Power Systems Design – March 2026

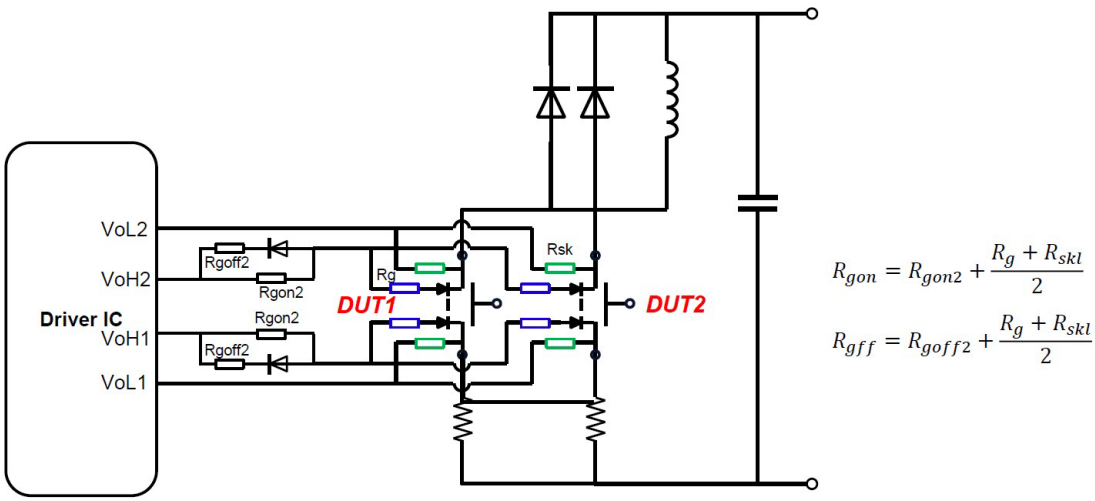

Figure 3: Resistor placement and calculations for the gate drivers

Performance of GaN BDS Under Test

Tests have shown that with these relatively simple design improvements, reliable operation at high switching frequencies is readily achievable. Described in JEDEC and IEC standards such as JEP182 and IEC60747, the double-pulse test is an important method for showing the desired behavior. This test provides the ability to evaluate rapid switching performance and losses through parasitic effects under the kinds of high-current and high-voltage conditions expected to be encountered with the loads used in real-world applications.

Using brief pulses in this type of testing limits the impact of self-heating in the device under test, helping to maintain a stable junction temperature. This minimizes possible errors in evaluation caused by changes in conductivity with temperature.

To perform the tests, an arbitrary waveform generator initiates two pulses in succession. The width of the first pulse is tuned to deliver a desired amount of test current through the load. The test equipment measures the turn-off delay, fall time, and changes in voltage and current at the end of the pulse. This initial pulse is quickly followed by a second that is designed to evaluate turn-on performance. This second pulse often reveals effects such as current overshoot. But the pulse is kept short enough to ensure stable measurements without excessive heating.

As well as showing device performance, the double-pulse test is also highly effective at showing how well-balanced devices are in a parallel configuration. With devices that are difficult to balance effectively, the current flow during each pulse will show one device dominating the other. In a practical application, this is undesirable as it implies one device will suffer increased stress, which leads to reliability issues. It also prevents the circuit from taking full advantage of the improvements that are theoretically achievable with a parallel configuration.

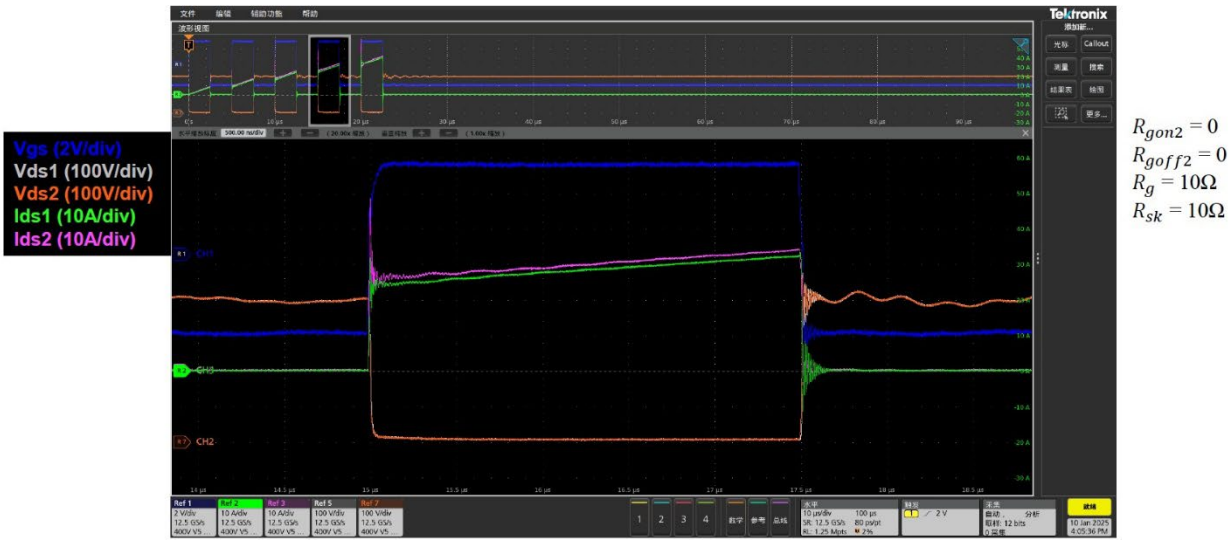

Figure 4: Pulse test shows close match in current increase during turn-on phase

Though there will inevitably be differences in current handling between devices in a parallel circuit, small deviations are not problematic. Tests performed on the NV6428 BDS GaN devices showed a difference of less than 2A when passing currents of more than 30A at peak.

Minor differences in gate threshold voltages will affect turn-on times. That has possible implications for the low-level ringing effects seen in any switched-mode power supply, even with suppression passives in place. Ideally, these ringing artifacts will be synchronized. The double-pulse tests performed by Navitas showed this to be the case: the current oscillations of two parallel devices during turn-off remained entirely in phase until the current dropped to zero. Tests of turn-on behavior similarly showed a synchronized overshoot and in-phase ringing until current flow settled approximately 200ns afterwards.

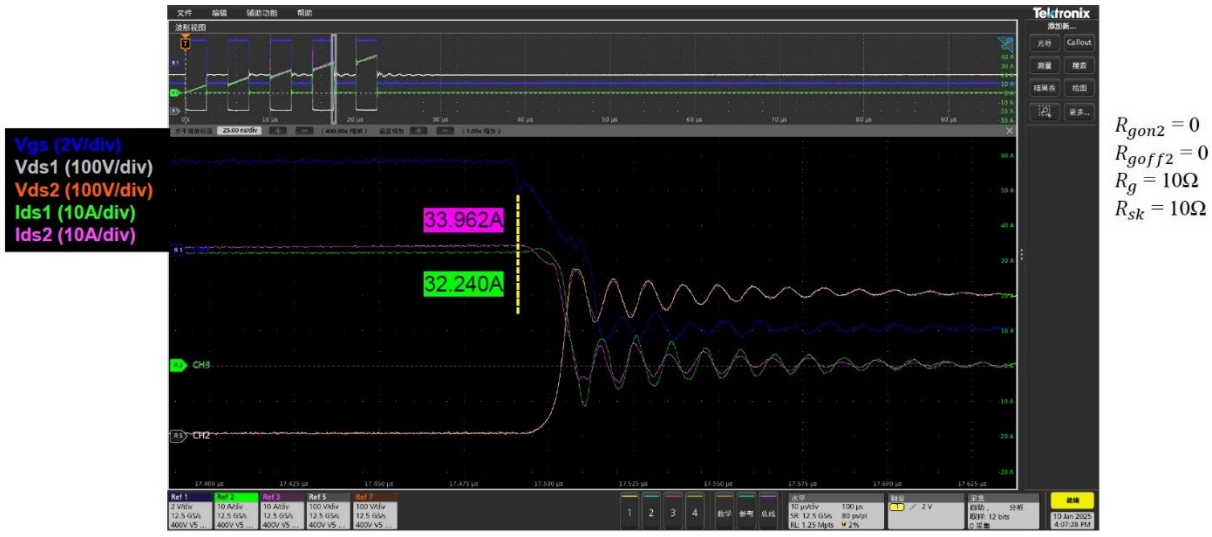

Figure 5: Synchronized oscillation for parallel devices in both voltage and current

Navitas engineers performed the tests at ambient room temperature and under elevated-temperature conditions at 120°C. Results remained consistent apart from expected changes in turn-on and turn-off losses. To help maintain good thermal performance, Navitas supplies the NV6428 and similar devices in top-cooled surface-mount packages with gull-wing leads. This design supports superior board-level temperature cycling.

Summary

By harnessing the high electron-mobility capabilities of GaN to the fullest extent, the BDS is helping to revolutionize the design of high-energy AC conversion circuits. This allows designers of such systems to push losses to even lower levels by taking advantage of parallel circuits and the new generation of BDS-based architectures.

Featured in Power Systems Design – March 2026