System integration benefits of GaN Power ICs

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Abstract

System partitioning is a key choice when it comes to deploying innovative solutions and overcoming technical and cost challenges in new system architectures. For years, GaN technology has been waiting to be widely adopted because of its specific technical requirements to drive the gate of the power FET in an optimal way and the cost associated to build a reliable scheme of drives and protections around the power stage that by itself is, in many cases, offering far superior performance if compared with a similar Silicon solution.

Integration of the power stage, drive, protection, logic and supply solutions in a monolithic GaN die overcomes those roadblocks and enables the implementation of high frequency (MHZ) off-line power supplies with a superior class of performance, low cost and improved reliability.

This paper will illustrate GaN power IC state of the art, integration capability and the benefits it brings in system efficiency and power density with a special focus on off-line voltage rated power ICs for AC/DC power converter applications.

1 GaN power IC technology

Gallium Nitride properties like maximum electric field (V/cm), energy gap (eV), electron velocity (cm/s) make this material suited for power and RF transistor construction. More specifically, AlGaN/GaN heterojunction structures enable high 2-Dimensional Electron Gas concentration and lateral electron mobility in the drift region and under the gate when the channel is formed with a positive voltage applied between the gate and source terminal of the structure as shown in figure 1.

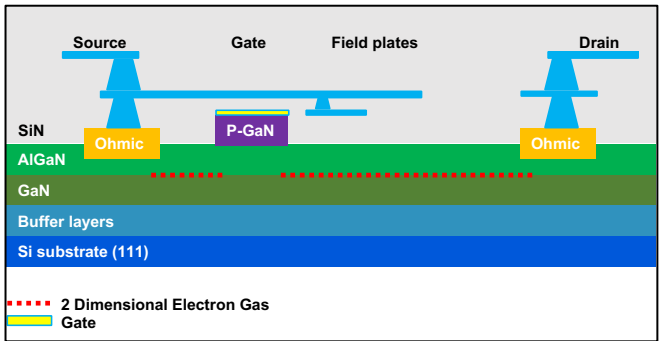

Fig. 1: GaN on Si High Voltage Enhancement Mode HEMT.

The result is a high breakdown voltage, enhancement mode (eMode), lateral FET which fits an IC requirement in terms of S-G-D terminal accessibility and performance.

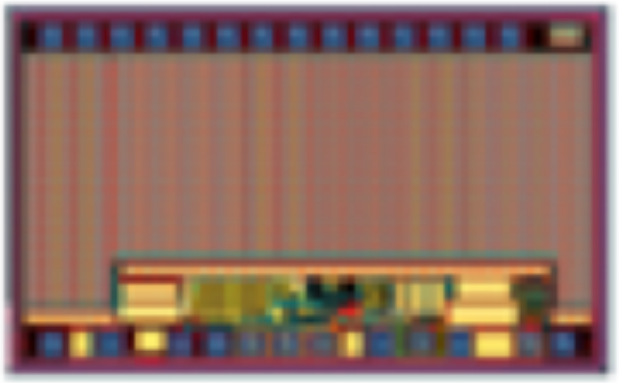

Fig. 2: Advanced HV GaN power IC with power FET, gate driver, under-voltage lock-out and dV/dt control.

At an advanced level of integration, many active and passive devices can be constructed and interconnected on the same die as in a planar IC process as long as proper isolation rules are applied between devices. Figure 2 shows a GaN power IC where most of the die is occupied by a

650V power FET and about 25% of the die is utilized for specific circuitry related to power FET drive and protection.
These power ICs find immediate application in the AC/DC and DC/DC switch mode power supply converters for consumer, industrial, or automotive segments.
Same die integration of specific features opens the doors to another level of efficiency and power density performance reached through innovative high frequency (>MHz) resonant topologies. The increased switching operating frequency of the converter allow a proportional reduction in size of the magnetic and capacitive elements of the converter stages increasing accordingly the converter power density (W/in^3). At the same time a significant improvement in the converter efficiency (%) is possible by the adoption of resonant topologies like ACF or LLC, instead of hard-switching topologies, for an optimized balance of switching and conduction losses.

2 GaN power IC integrated features

With converter power density and efficiency improvement targets in mind, the key feature of the IC consists of an optimal driver stage in terms of gate drive levels and controlled turn-on and turn off transient.

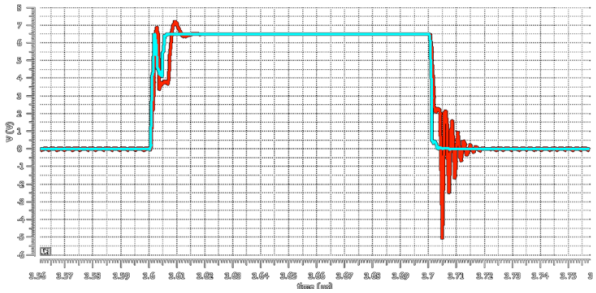

Fig. 3: Gate power FET ON and OFF transient simulations; the red waveform shows the ringing effect due to gate loop inductance - in blue the same gate driven by a monolithically integrated drive.

In a discrete FET approach the driver is part of a different IC and is electrically connected to the gate of the GaN power FET through PCB interconnection or bond wires in case of a co-package Multi-Chip-Module solution. In any of these cases a parasitic CSI (Common Source Inductance) will be part of the gate loop, so a large dI/dt related to turn-on and turn-off operation will cause positive and negative spikes of the gate voltage that will compromise the power FET reliability over time. While a gate resistor R_g is typically used as damping element for the gate loop inductance and power FET input capacitance resonant network, this resistor is also responsible for the slow down of the rise and fall time of the power FET gate and, in so doing, prolongs the voltage and current crossover time causing a significant increase in switching losses.
In addition, the R_g reduces the effective gate driver turn off strength making the power FET more susceptible to the Miller capacitance self turn-on effect in the case of half bridge complementary switching topologies. This effect can negatively impact efficiency performance and power FET reliability.
In order to avoid the use of an R_g, a monolithically integrated driver is so far the best solution.

2.1 Monolithic Integrated Driver

In a monolithic approach the gate driver is integrated in the same die of the power FET reducing the CSI to virtually zero by proximity of the gate pull-up and pull-down transistor to the gate of the power FET.

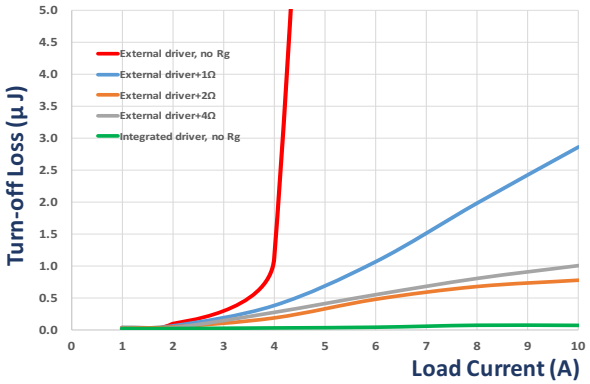

Fig. 4: Power-Fet turn-off losses in

The power FET driver is optimized for minimum propagation delay, ON gate voltage level, and immunity to Miller capacitance during OFF state. The virtual zero gate inductance loop of the integrated driver provides optimal gate ON↔OFF transition voltage profiles, avoiding gate

overshoot, typical of external drivers with large gate loop inductances. The virtual zero inductance in the turn-off loop delivers the fastest gate turn-off time (500ps) dropping the turn-off losses by 90% (Fig.4).

2.2 Integrated switching node slew rate control

While the turn-off sequence is optimized to minimize losses, the turn-on sequence needs to be also optimized for EMI system requirement, every time a hard switching event happens. For this reason, a driver should provide a selectable slew-rate value which can be chosen through the value of an external resistor. The external resistor (R_{DD} in Fig.5a) will be used to modulate the strength of power FET gate pull up transistor and, in turn, its rise time

The slew rate should be selectable in the range of 10 to 90V/ns (Fig.5b) so that the EMI figure is kept under control while impact on the turn-on losses is still negligible.

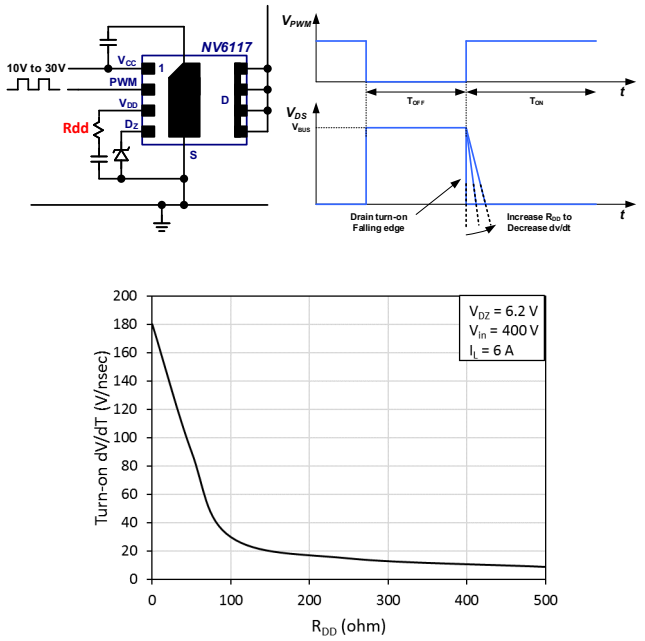

Fig. 5a: R_{DD} configuration and turn-on switching node dV/dt control.

Fig. 5b: Turn-on switching node dV/dt selection range.

By optimizing the driving sequence for radiated and conducted EMI the system may avoid or substantially reduce bulky EMI suppressors and improve the fundamental power density performance indicator.

2.3 Integrated voltage regulator

Like Si FETs, eMode GaN FETs need to be driven at an optimal gate voltage in order to achieve the best possible efficiency.

An integrated voltage regulator makes sure the rail to rail driver is biased with correct voltage (6.2V) to provide the ideal turn-on level to the gate of the power FET even with a wide range of VCC supply (10V~30V). An external Zener diode can be used to provide a reference voltage to the voltage regulator. This reduces external component count and optimizes conduction losses while still operating in a safe and reliable gate-source voltage range for the power FET.

An integrated voltage regulator could also allow the IC to go in standby mode when PWM input signal is not present, which reduces the VCC power consumption.

2.4 Integrated bootstrap FET

In a half-bridge configuration, using eMode GaN FETs for the high side brings considerable cost saving and efficiency improvement, however a voltage higher than the power rail supply (V+) is needed in order to bias the gate of the high side switch.

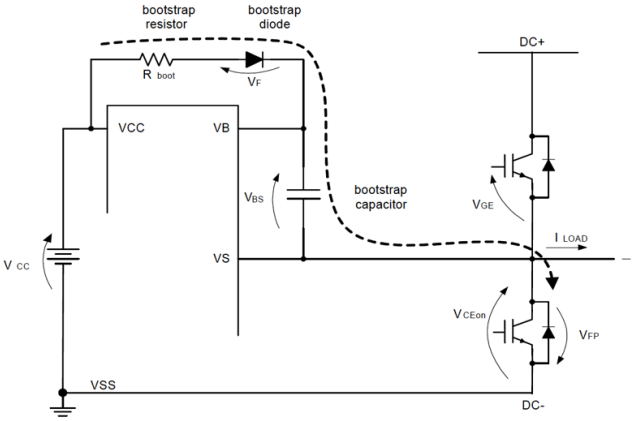

Fig. 6: Bootstrap power supply circuit implementation with discrete devices.

One of the most widely used methods to supply power to the high side gate drive circuitry of the

high voltage gate-drive IC is the bootstrap power supply. This bootstrap power supply technique has the advantage of being simple and low cost.

A possible implementation of bootstrap power supply circuit for a high voltage gate driver using discrete devices is shown in Fig.6 and it operates as follows: when the switching node goes below the IC supply voltage, Vcc, or is pulled down to ground (the low side switch is turned on and the high side switch is turned off), the bootstrap capacitor, C_{BOOT}, charges through the bootstrap resistor, R_{BOOT}, and bootstrap diode D_{BOOT}, from the Vcc power supply, as shown in Fig.5.

When the low-side switch is turned off and high-side switch is turned on, the high side quiescent current is provided by C_{BOOT}, and in this case the switching node is pulled to a higher voltage by the high-side switch so that VBS supply floats and the bootstrap diode is reverse biased and blocks the rail voltage from the IC supply voltage.

2.5 How to overcome bootstrap circuitry limitations

Besides being simple and low cost, a bootstrap circuit has two critical limitations:

1) The on-time of the duty-cycle is limited by the requirement to refresh the charge in the bootstrap capacitor;
2) The reverse recovery charge and diode parasitic capacitance of the bootstrap diode contribute converter losses;
3) The switching node can go negative during deadtime if the load current flows in the low-side freewheeling diode, causing the C_{BOOT} to overcharge at a voltage higher than Vcc. This can be even worse if the bootstrap diode forward voltage does not match the freewheeling voltage of the low side switch. This can happen if a silicon diode is used as bootstrap element and GaN eMode FET is used as low side switch.

Duty cycle limitation is overcome by proper selection of the bootstrap capacitor (7) that must also comply to start-up operations (8).

A GaN integrated bootstrap completely overcomes the overcharge and losses contribution limitation.

If a GaN eMode FET is used as a bootstrap element, its very low output capacitance can be neglected for the bootstrap losses. In addition, GaN technology is free of minority carriers which enables zero recovery charge reducing further bootstrap related power losses. It also eliminates diode recovery losses and avoids risk of dV/dt induced diode failure.

Bootstrap overcharge limitation can be instead overcome by a system integration approach. Fig.7 shows a monolithically integrated GaN half bridge with high and low side driver and bootstrap circuitry and a voltage regulator. In this case, a high voltage FET and driver are used in replacement of the external diode. The presence of the voltage regulator for the driver supply voltage ensures that no C_{BOOT} overvoltage is applied to the gate of the GaN FET.

An integrated high voltage GaN bootstrap FET device significantly reduces the board size if compared with an external solution because of the spacing required to properly manage the high voltage across devices.

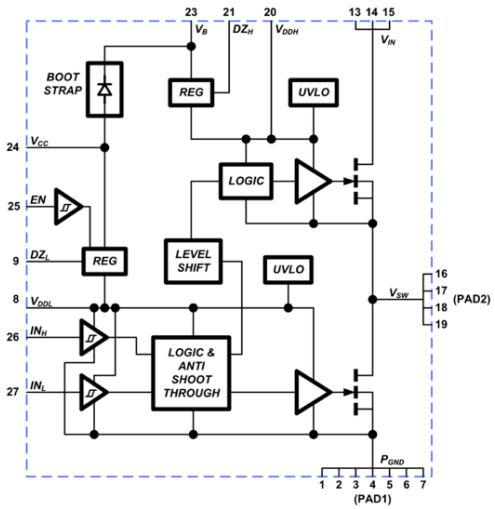

Fig. 7: Monolithically integrated GaN half bridge with high and low side driver, bootstrap and level shifter circuitry.

2.6 Integrated high voltage level shifter

In half bridge topologies, the driver and the ground referenced control signal are linked by a level shift circuit that must tolerate the high voltage difference and considerable capacitive switching currents between the floating high side and ground−referenced low side circuits. The high voltage gate driver ICs are differentiated by a unique level shift design. To maintain high

efficiency and manageable power dissipation, the level−shifters should not draw any current during the on−time of the main switch. A widely used technique for these applications is called pulsed latch level translators (8).

In order to maintain high efficiency and manageable power dissipation, the level shifters should not draw any current during the on-time of the main switch. Even a modest 1 mA current in the level shift transistors might result in close to 0.5 W worst-case power dissipation in the driver IC.

System efficiency will benefit from integrated level-shifter with the following characteristics:

1) Fast level shifting operation: to reduce reverse conduction operation of the high side during dead time (T_{prop}<50ns)

2) Low loss level shifting operation for high frequency operation: the use of pulses greatly reduces the power dissipation associated with the level translation. Pulse amplitude and duration have to be carefully designed to fit all operating conditions for resonant and hard switching converters topologies as in Fig.8.

3) dv/dt immunity up to 200V/ns: the pulse discriminator logic is able to distinguish the set/reset pulses from fast dv/dt noise transients caused by power device switching.

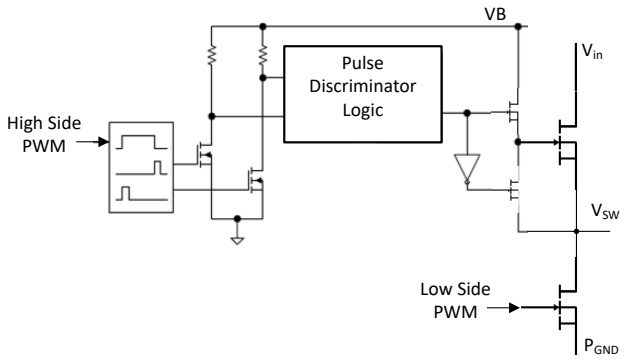

Fig. 8: Traditional scheme of a pulse-based level shifter for high voltage gate driver.

2.7 Robustness and reliability

The most integrated Silicon high voltage gate drive ICs have parasitic diodes, which, in forward or reverse breakdown, may cause parasitic SCR latch−up. The ultimate outcome of latch−up often defies prediction and can range from temporary erratic operation to total device failure (8).

GaN integrated power ICs do not have parasitic junctions and substrate diodes making the IC latch-up free.

GaN power ICs have demonstrated excellent reliability performance at static and dynamic test as well at temperature cycle. Devices have passed High Temperature Reverse Bias (1,000hrs @ 150C, 520V V_{DS}), High Temperature Operating Life (1,000hrs @ 150C, ZVS switching condition), ESD 1,000V HBM and 500V CDM.

Additional tests have also been conducted to be compliant with and exceed Jedec qualification standards.

3 Conclusions

In this work it has been shown how an integrated approach of power FET, gate driver, bootstrap and level shifter bring major system level efficiency and power density improvements and makes easy and convenient the use of eMode GaN power FET in off-line power converter.

The monolithic integration of the gate driver and power switch can effectively eliminate the parasitic inductance in the gate drive loop allowing more reliable performance even at MHz switching frequency while still improving efficiency.

The high switching frequency enables a major shrink in size of the power converter.

These power integrated circuits can be fabricated employing a GaN on Silicon 650V process.

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