Trench-Assisted Planar SiC MOSFET Technology

By Arash Salemi, Sumit Jadav, Jaehoon Park, and Siddarth Sundaresan

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1. Introduction

Navitas Semiconductor, under its GeneSiC™ SiC MOSFET product line, utilizes a proprietary **trench-assisted planar technology**. This advanced design aims to deliver a "no-compromise" solution, balancing performance, manufacturability, and reliability in a way that traditional planar or trench SiC designs often struggle to achieve. Although a trench MOSFET has a potential of lower specific on-resistance ($R_{ON,SP}$), it struggles with reliability/robustness and requires about 40% more process steps than planar thus increasing the cost and lowering the yield. Navitas' patented trench-assisted planar gate design is a no-compromise, next-generation solution; high-yield manufacturing, fast and cool operation, and extended, long-life reliability. It enables the lowest $R_{DS,ON}$ at high temperature and the lowest energy losses at high speeds. This enables unprecedented, industry-leading levels of performance, robustness and quality. Additionally, all GeneSiC SiC MOSFETs have the highest-published 100% production-tested avalanche capability.

2. Trench-Assisted Planar SiC MOSFET Technology

Navitas' GeneSiC™ trench-assisted planar silicon carbide (SiC) MOSFET technology uses a planar gate structure. In this design, the channel—where the current flows—is primarily created on the top surface of the SiC wafer. This planar configuration simplifies manufacturing compared to traditional trench technology. Planar-gate processes are generally less complex and result in higher manufacturing yields than processes involving deep-etched, high-aspect-ratio trenches.

The "trench-assisted" aspect introduces shallow trenches strategically placed within the device structure in source regions. These trenches are not for creating the main current path (as in a trench MOSFET). Instead, their primary functions in Navitas' SiC MOSFET design are to:

- **Optimize Electric Field Distribution for Enhanced Reliability and Robustness:** SiC, with its high breakdown strength, relies heavily on precise electric field management to prevent premature breakdown and ensure robust operation. The trenches help to smooth out and control the electric field peaks that can occur at corners or junctions, lowering stress on the gate oxide and long-term reliability as shown in Figure 1. The "multi-step profile" of the trench-assisted design helps to drive a smoother electric field distribution, resulting in lower voltage stress across the device and increasing avalanche capability, long-term reliability in high-voltage, high-temperature, high-dV/dt conditions.

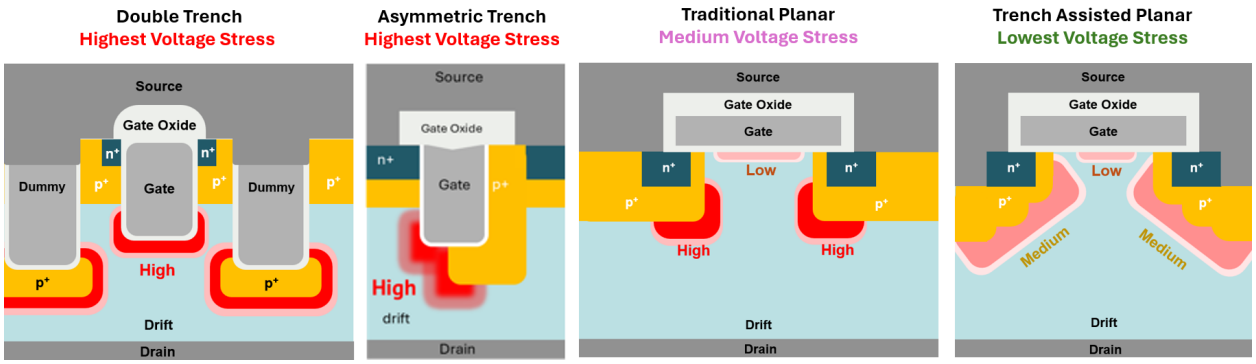

Figure 1. Cross-sectional views illustrating the cell pitch for different Power MOSFET technologies: double trench, asymmetric trench, traditional planar, and trench-assisted planar technologies.

- **Reduce On-Resistance ($R_{DS,ON}$) at High Temperatures:** Figure 2 illustrates the current spreading across all technologies listed in Figure 1. Trench-assisted planar technology demonstrates superior current spreading, a benefit attributed to the multi-step profile enabled by the trench-assist feature. Furthermore, Navitas's trench-assisted planar design has been optimized to achieve lower $R_{DS,ON}$, even at elevated operating temperatures. This presents a significant advantage, as $R_{DS,ON}$ typically increases with temperature in MOSFETs. By maintaining a lower $R_{DS,ON}$ across the operating temperature range, conduction losses are reduced, leading to cooler operation and higher efficiency. This improved performance is partly due to the enhanced current spreading facilitated by the trench-assist's multi-step profile.

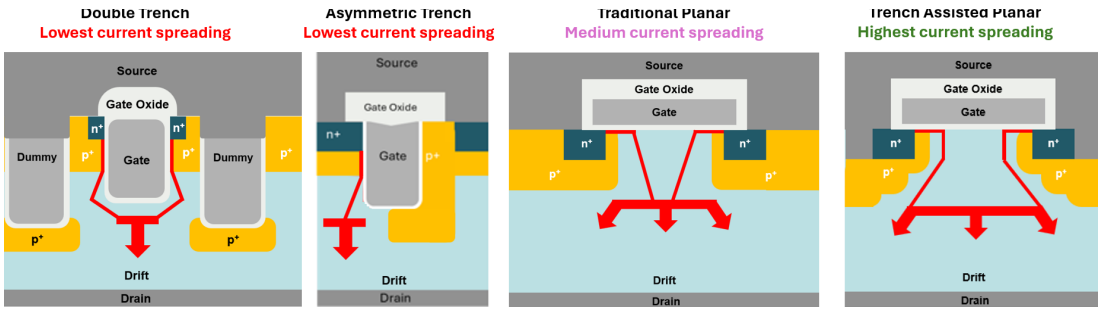

Figure 2. Schematic view of current spreading in traditional planar double trench, asymmetric trench, traditional planar, and trench-assisted planar technologies.

- **Improve Switching Performance:** The optimized device geometry and electric field control contribute to better switching characteristics, including potentially lower switching losses.
- **Enhance Gate Oxide Reliability:** A critical challenge in SiC MOSFETs, particularly trench-gate designs, has been the reliability of the gate oxide, which can be subjected to high electric fields at trench corners. The trench-assisted planar technology mitigates these stresses, leading to a more stable threshold voltage (V_{TH}) and improved gate oxide lifetime.

3. Advantages Compared to Planar and Trench SiC Technologies

3.1 Comparison with Traditional Planar SiC MOSFETs

- **Lower $R_{ON,SP}$:** The shallow trench in the source region of trench assisted-planar design provides enough surface to have an appropriate metallization in a smaller gap thus allowing for a lower cell-pitch as shown in Figure 3. It results in a lower $R_{ON,SP}$ compared to traditional planar design.

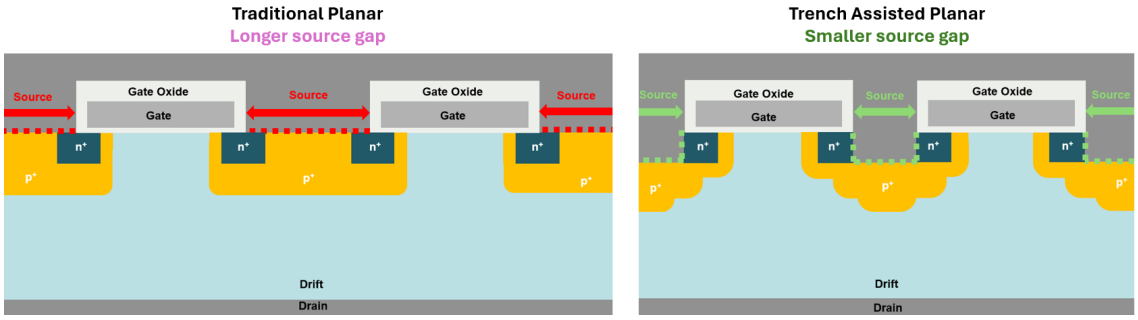

Figure 3. Cross-sectional view of source region in a traditional planar (left) and trench assisted planar (right)

- **Lower $R_{DS,ON}$ at Elevated Temperatures:** Navitas specifically highlights up to 20% lower $R_{DS,ON}$ at elevated temperatures compared to competitors, leading to lower conduction losses and cooler running. This is a direct benefit of the optimized current spreading as shown in Figure 3 and electric field management enabled by the trench assist as shown in Figure 1.
- **Lower Switching Losses:** The optimized electric field and potentially reduced parasitic capacitances contribute to faster and more efficient high-frequency switching, enabling higher power density.
- **Enhanced Reliability and Robustness:** The "multi-step profile" of the trench-assisted design helps to drive a smoother electric field distribution, resulting in lower voltage stress across the device and increasing long-term reliability in high-voltage, high-temperature, high-dV/dt conditions.

3.2 Comparison with Trench SiC MOSFETs

- **Simpler Manufacturing and Higher Yield:** Trench SiC MOSFETs, while offering very low $R_{DS,ON}$ due to their vertical channel, typically require more complex fabrication steps (e.g., etching deep, narrow trenches) which can lead to higher manufacturing costs and lower yields. Navitas's trench-assisted planar design retains the manufacturing simplicity of planar devices while gaining performance benefits.
- **Superior Gate Oxide Reliability:** A major concern with trench SiC MOSFETs is the high electric field concentration at the trench corners, which can stress the gate oxide and impact long-term reliability (see Figure 1). The trench-assisted planar design with its smoother electric field distribution minimizes these stresses, contributing to a more robust gate oxide. Navitas emphasizes rugged gate oxide (stable V_{TH}).
- **Enhanced Reliability and Robustness:** The "multi-step profile" of the trench-assisted design helps to drive a smoother electric field distribution, resulting in lower voltage stress across the device and increasing long-term reliability in high-voltage, high-temperature, high-dV/dt conditions.
- **Optimized for Overall Performance (not just $R_{DS,ON}$):** While trench designs can achieve the absolute lowest $R_{DS,ON}$ for a given chip area, they often face trade-offs in gate oxide reliability and potentially higher switching losses due to increased gate capacitance. Navitas's trench-assisted planar technology seeks a balance, delivering excellent $R_{DS,ON}$ with superior switching characteristics and robustness, providing a more balanced and practical solution for high-power applications.
- **Lower $R_{DS,ON}$ Shift with Temperature:** Navitas specifically states "low $R_{DS,ON}$ shift vs temp" for their trench-assisted planar technology, indicating more stable performance across the operating temperature range compared to both standard planar and trench designs.

4. Conclusion

Navitas's GeneSiC trench-assisted planar technology represents a significant advancement in Silicon Carbide (SiC) power MOSFET design, effectively overcoming the inherent trade-offs typically found in traditional planar and trench architectures. By strategically incorporating shallow trenches into a fundamentally planar gate structure, Navitas delivers a "no-compromise" solution. This innovative approach ensures high-yield manufacturing and excellent thermal dissipation, while simultaneously optimizing electric field distribution to achieve the lowest $R_{DS,ON}$ at high temperatures, reduced switching losses, and superior gate oxide reliability. Consequently, Navitas's GeneSiC MOSFETs offer industry-leading performance, robustness, and quality, enabling faster, cooler, and more reliable power conversion for demanding high-power applications like electric vehicles, data centers, and renewable energy systems.

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Contact: info@navitassemi.com