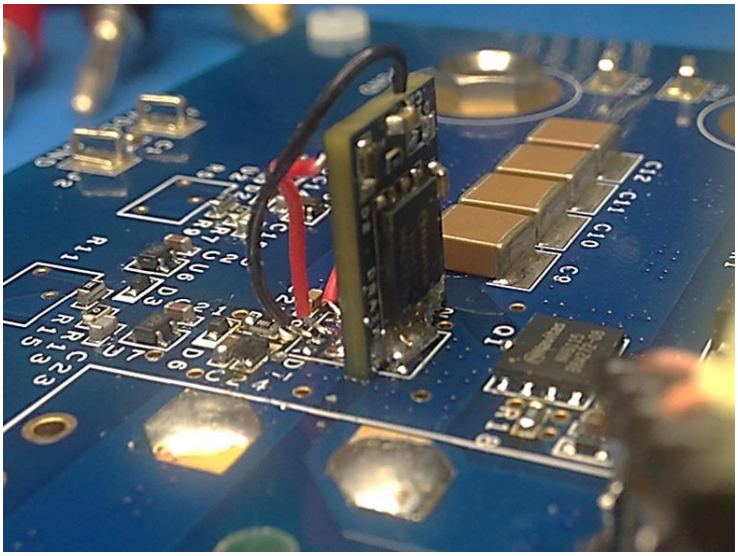
NV6115 Daughtercard

UG009b

This user's guide covers:

Demo Board#	Description	Parts Used	F_{SW}
NVE014B *(supersedes NVE014)*	**NV6115 Daughtercard**	**NV6115**	**N/A**



IMPORTANT NOTICE:

Hazardous voltages are present on this demo board. Personal contact with high voltages may result in injury or death. Correct handling and safety procedures must be observed. Boards are for lab bench evaluation only. Not for installation in end-user equipment.

CAUTION:

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

Description:

This demo board uses as single NV6115 GaN Power IC to provide easy evaluation of Navitas GaN in existing power supply circuits. While higher efficiency is expected with a simple 'drop-in' replacement using this daughtercard, the maximum benefits of GaN Power IC are achieved by re-designing the power supply with optimal layout and new magnetic components running at higher switching frequency. In other words, use this daughtercard to understand GaN's performance benefit at low frequency, then lay out a new board (with new, smaller magnetics) optimized for higher frequency.

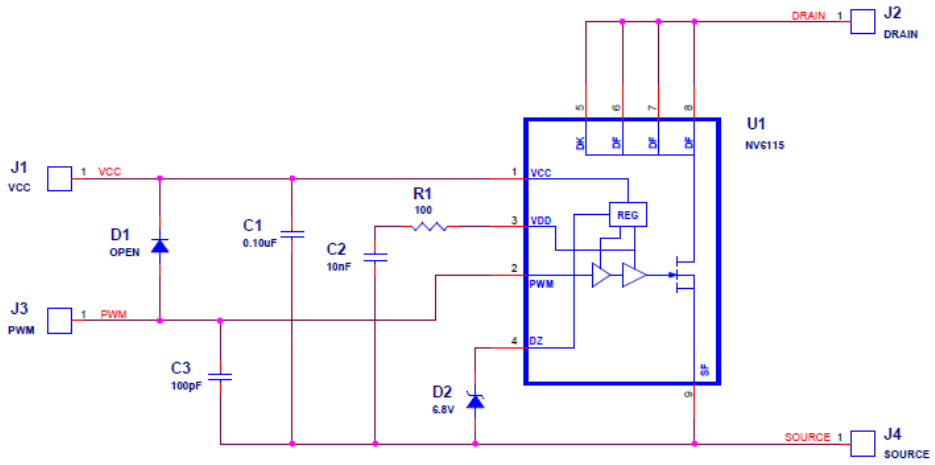
The NV6115 is designed for both hard switching topologies such as single switch PFC, and soft switching half-bridge topologies, e.g. Active Clamp Flyback (ACF) or LLC resonant DC-DC converters.

Operation Conditions, Performance:

For detailed description of the NV6115 GaN Power IC, including layout guidelines, please refer to the device datasheet (www.navitassemi.com (requires registration)). For individual files for schematic, PCB (gerber, .dxf), etc., please contact info@navitassemi.com.

The 4-terminal daughtercard contains all components required for simple evaluation of the NV6115, as shown in the schematic below (Fig.1). Connections are: V_{CC}, PWM_{IN}, Drain and Source.

Fig.1
Daughtercard
Schematic



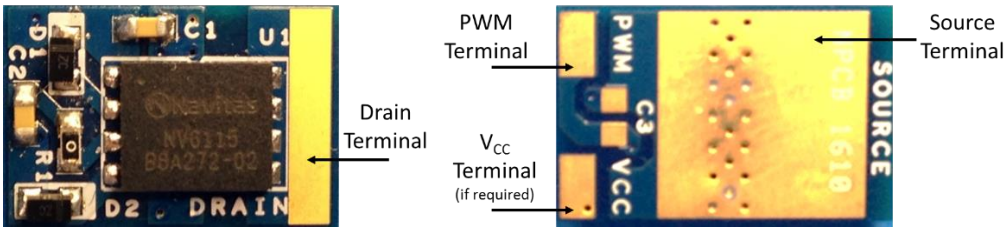
Features:

1) Turn-on dv/dt control (R1).
    a. Pre-installed with 100-ohm to limit dv/dt to 50V/ns. Can be increase to reduce dv/dt further to avoid potential noise problem.
2) Filter capacitor to reduce noise to PWM pin (C3)
    a. Pre-installed (100pF) to reduce noise coupling to PWM pin.
3) Standard bias voltage.
    a. V_{CC} range 10-20V.
4) 3-pin operation
    a. If PWM signal > 10V, user can install D1 to derive V_{CC}.
    b. Only 3 connections are needed: PWM, Drain and Source.

The daughtercard measures 9x13mm, and is shown in Fig.2. It is a “drop-in” for all low side switch sockets, and for half bridge high side socket when a standard half bridge driver with bootstrap diode is used. For power supplies that use a pulse transformer to drive the high side switch, a slight modification is needed. A bootstrap diode is needed to create a bias voltage (>10V), and a 3kΩ PWM resistor to handle the negative transformer output voltage.

Fig.2 Daughtercard (front, back)

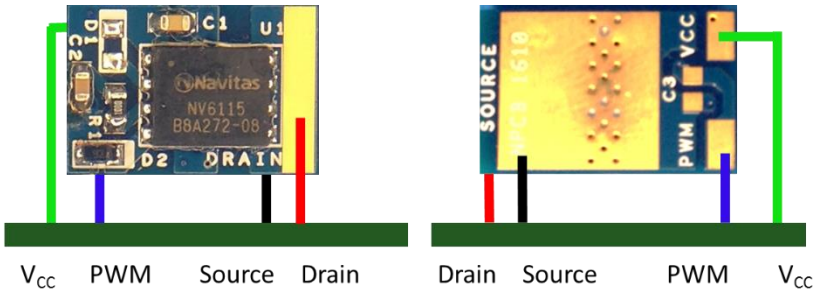
(with D1 populated)



Recommended use:

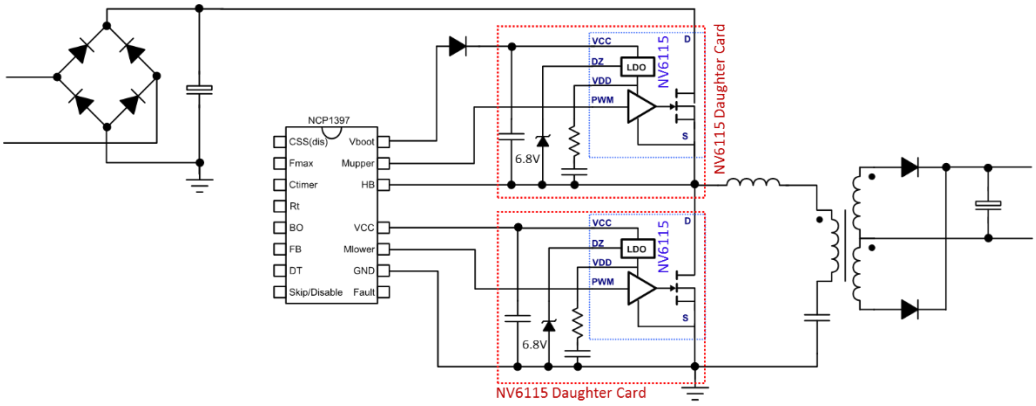
1) Orientation
    a. See Fig. 3
    b. It minimizes the length of connection wires
2) Source pad
    a. Daughtercard’s ground reference - the MOST important connection to motherboard. **Solder source pin as close as possible to the motherboard**. A long trace will introduce SOURCE inductance, which interferes with PWM logic. This is especially important when a current sense resistor is used on the source side. If source inductance noise is not avoidable, increase external PWM input resistor to filter out Ldi/dt induced noise. (See Fig 6)
    b. Attach heatsink to this terminal to simulate PCB cooling
    c. Extra source wire serves as a Kelvin reference for PWM signal
3) PWM input pad
    a. Connect to motherboard gate signal (direct to control IC output, or after gate-drive transformer as required), minimum length.
4) Drain terminal
    a. Use large gauge wire, minimum length.
5) VCC terminal
    a. 10V to 20V

Fig.3 Preferred mounting orientation



Example #1: LLC Half Bridge Circuit

Fig.4
LLC



Example #2: Active Clamp Flyback

Fig.5
ACF

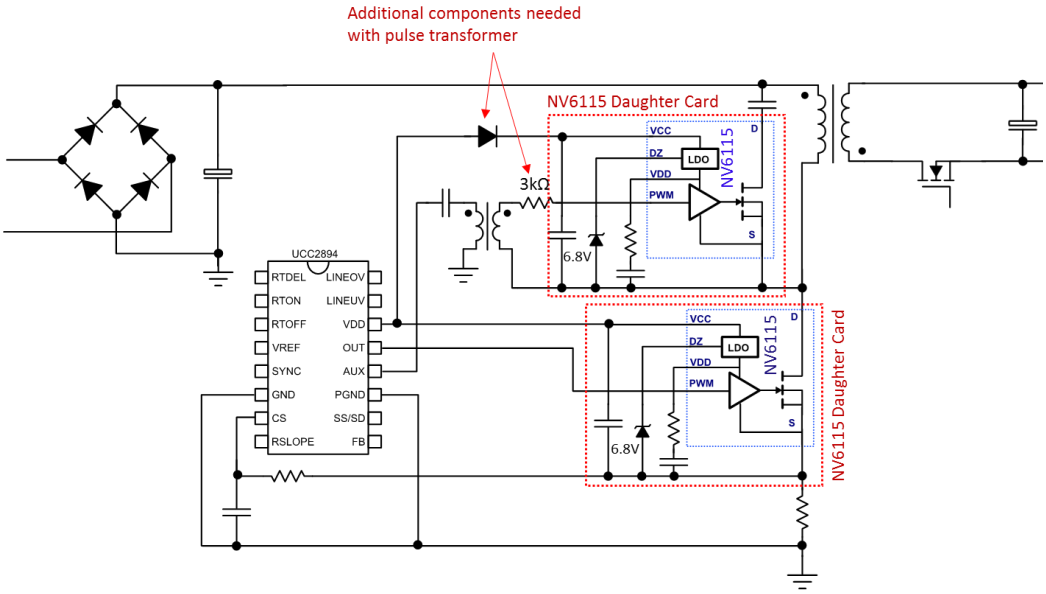
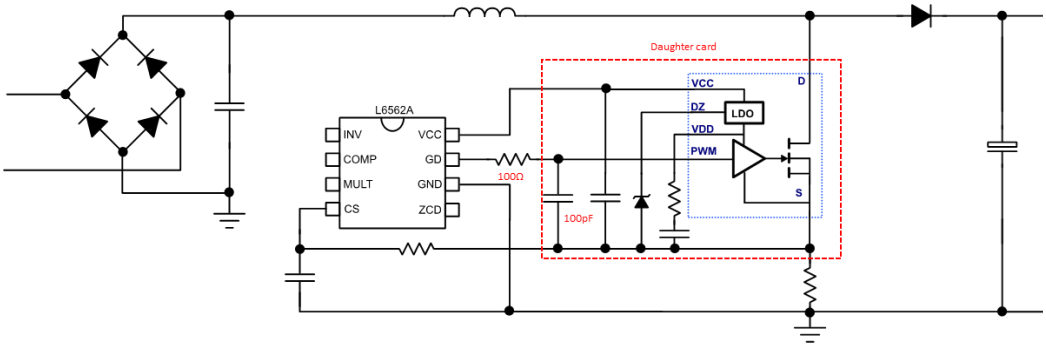


Fig. 6: PFC

Example #3: PFC Boost with Current Sense Resistor



Revision History:

Date	Status	Notes
5-2-16	RELEASED	First publication
6-9-16	RELEASED	Example #3 added. Input filter (C3) increased from 22pF to 100pF. External 100-ohm resistor is requested if current sense resistor is used.
9-1-16	RELEASED	Update to UG009b (NVE014B) C2 value changed to reduce startup time (100nF to 10nF) V_{CC} range extended (from 12-20V to 10-20V).

Additional Information:

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