### GeneSiC<sup>®</sup>

### G3F09MT12FB2

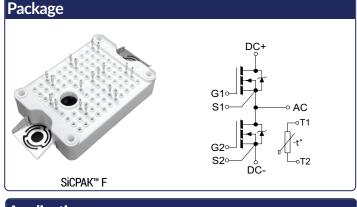
## 1200V 9.3m $\Omega$ Half-Bridge SiC Module

SiCPAK<sup>™</sup> F Series Trench-Assisted Planar Technology

#### **Built for Performance and Endurance**

- Epoxy-resin potting and trench-assisted planar SiC MOSFET technology for long-lasting reliability
- Engineered and qualified to withstand harsh stress, temperature variations, and power cycling
- Low on-resistance R<sub>DS(ON)</sub> across temperature
- Optimized switching speed and balanced  $Q_{GD}/Q_{GS}$  for faster, cleaner, and efficient switching performance
- Stable and consistent V<sub>GS,th</sub> for excellent current sharing and reliable switching
- Outstanding short-circuit & avalanche (UIS) performance
- THB (HV-H3TRB) qualification at module-level & dielevel
- Optional pre-applied Thermal Interface Material (TIM), "-T" orderable part number suffix

VDS	=	1200 V
Rds(on)	=	9.3 mΩ
D,DC (65°C)	) =	109 A



#### Applications

- EV Road Side Chargers
- Solar Inverters
- Energy Storage Systems (ESS)
- Uninterrupted Power Supplies (UPS)
- Motor Control and Drives
- Smard Grid and Distributed Generation
- Induction Heating and Welding

#### Absolute Maximum (per Switch Position) (At Tc = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	V <sub>DS,max</sub>	$V_{GS}$ = 0 V, I <sub>D</sub> = 100 $\mu$ A	1200	V	
Gate-Source Voltage (Dynamic)	V <sub>GS,max</sub>	Transient	-10/+22	V	
Gate-Source Voltage (Operation)	V <sub>GS,op</sub>	Static	-5/+18	V	Note 1
Virtual Junction Temperature	Tj	Operation	-40 to 175	°C	
Dower Dissinction	D	T <sub>H</sub> = 65°C, T <sub>j,op</sub> ≤ 175°C	238	\ <b>A</b> /	Fig. 17
Power Dissipation	PD	T <sub>H</sub> = 120°C, T <sub>j,op</sub> ≤ 175°C	119	W	Fig. 17
DC Continuous Drain Current		T <sub>H</sub> = 65°C, T <sub>j.op</sub> ≤ 175°C, V <sub>GS</sub> = 18 V	109	^	<b>Fig. 16</b>
DC Continuous Drain Current	ID,DC	$T_H$ = 120°C, $T_{j,op} \le 175$ °C, $V_{GS}$ = 18 V	77	A	Fig. 16

NOTE: This datasheet provides preliminary specifications. Parameters, conditions and values are subject to change.

Note 1: Recommended operating (static) on-state gate voltage is +15V to +18V and off-state gate voltage is -5V to -3V

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		) (At T <sub>C</sub> = 25°C Unless Otherwise Stated) Conditions –	Values				
Parameter	Symbol		Min.	Тур.	Max.	Unit	Note
Drain-Source Breakdown Voltage	V <sub>DSS</sub>	$V_{GS}$ = 0 V, $I_{D}$ = 100 $\mu A$	1200			V	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ = 1200 V, $V_{GS}$ = 0 V		1		μA	
Gate Source Leakage Current	I <sub>GSS</sub>	$V_{GS}$ = 22V, $V_{DS}$ = 0V $V_{GS}$ = -10V, $V_{DS}$ = 0V			100 -100	nA	
Gate Threshold Voltage	V <sub>GS,th</sub>	$V_{DS} = V_{GS}, I_D = 70 \text{ mA}$ $V_{DS} = V_{GS}, I_D = 70 \text{ mA}, T_i = 175^{\circ}\text{C}$	2.2	2.7 2.0	4.3	V	Note 2
Drain-Source On-State Resistance	Rds(on)	V <sub>GS</sub> = 18V, I <sub>D</sub> = 90 A V <sub>GS</sub> = 18V, I <sub>D</sub> = 90 A, T <sub>j</sub> = 175°C		9.25 16.65	12.5	mΩ	Note 3,4 Fig. 6-9
Input Capacitance	Ciss	N/ 0001/11/ 01/		9850			
Output Capacitance	Coss	V <sub>DS</sub> = 800V, V <sub>GS</sub> = 0V f = 100kHz, V <sub>AC</sub> = 25mV		364		pF	Fig. 12
Reverse Transfer Capacitance	Crss	- 1- 100km2, VAC - 25mV		23			
Internal Gate Resistance	<b>R</b> G,int	$V_{GS}$ = 18V, f = 500kHz, $V_{AC}$ = 25mV		0.65		Ω	
Gate-Source Charge	Q <sub>GS</sub>	$V_{DS}$ = 800V, $V_{GS}$ = +18/-5V		112			
Gate-Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 90 A		78		nC	Fig. 11
Total Gate Charge	$Q_{G}$	Per JEDEC JEP-192		392			
Turn-On Switching Energy (Body Diode)	E <sub>0n</sub>	Tj = 25°C, V <sub>GS</sub> = -5/+18V, R <sub>G(ext)</sub> = 4.7 Ω, L		2695		1	Fig. 24.27
Turn-Off Switching Energy (Body Diode)	Eoff	= 60 μH, I <sub>D</sub> = 120 A, V <sub>DD</sub> = 800 V		203		μJ	Fig. 24-27
Rise Time	tr	V <sub>DD</sub> = 800 V, V <sub>GS</sub> = -5/+18V		24			
Fall Time	t <sub>f</sub>	$R_{G(ext)}$ = 4.7 $\Omega$ , L = 60 $\mu$ H, I <sub>D</sub> = 120 A Timing relative to V <sub>DS</sub> , Inductive load		29		ns	Fig. 26

### **Body Diode Characteristics** (per Switch Position) (At T<sub>j</sub> = 25°C unless otherwise specified)

Deremeter	Sumbol	Conditions	Values			Unit	Nata
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit	Note
Diede Ferruerd Veltere		$V_{GS}$ = -5V, $I_{SD}$ = 45 A		4.5		У Г.	
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = -5V, I <sub>SD</sub> = 45 A, T <sub>j</sub> = 175°C		4.1		v	Fig. 18,19
DC Continuous Diado Current	1	$T_{H}$ = 65 °C, $T_{j,op} \le 175$ °C, $V_{GS}$ = -5 V		56		٨	
DC Continuous Diode Current	ISD	$T_{H}$ = 120 °C, $T_{j,op} \le 175$ °C, $V_{GS}$ = -5 V		37		A	

<u>NOTE</u>: This datasheet provides <u>preliminary specifications</u>. Parameters, conditions and values are subject to change.

Note 2: Tested after applying +25V for 80ms

Note 3: Device(Die) ON State resistance only: Package resistance reported separately in module characteristics Note 4: Total effective resistance per switch postition (HS or LS) = MOSFET R<sub>DS(ON)</sub> + package resistance by switch position

### **Module Characteristics**

Parameter	Symbol	Conditions	Values			Unit	Note
Parameter	Symbol	Conditions	Min.	. Тур. Мах.		Unit	Note
Thermal Resistance, Junction - Heatsink	R <sub>thJHS</sub>	per switch TIM = 80 $\mu m$ , $\lambda$ = 4.4 W/(m.K)		0.42		°C/W	Fig. 14
Case Temperature	Tc		-40		150	°C	
Stray Inductance	Lstray	Between DC+ and DC- f = 10 MHz		7.43		nH	
Package Resistance, HS	R <sub>HS</sub>	T <sub>C</sub> = 125 °C		1.58		- m0	Note 4
Package Resistance, LS	R <sub>LS</sub>	T <sub>C</sub> = 125 °C		1.48		mΩ	NOLE 4
Weight	W			28.1		g	
Case Isolation Voltage	Viso	AC 50 Hz, 60s		4000		V	
Comparative Tracking Index	CTI	Epoxy-resin EMC		200			
0 D' I		Terminal to Terminal		6.4		100.000	
Creepage Distance		Terminal to Heatsink		12.7		mm	

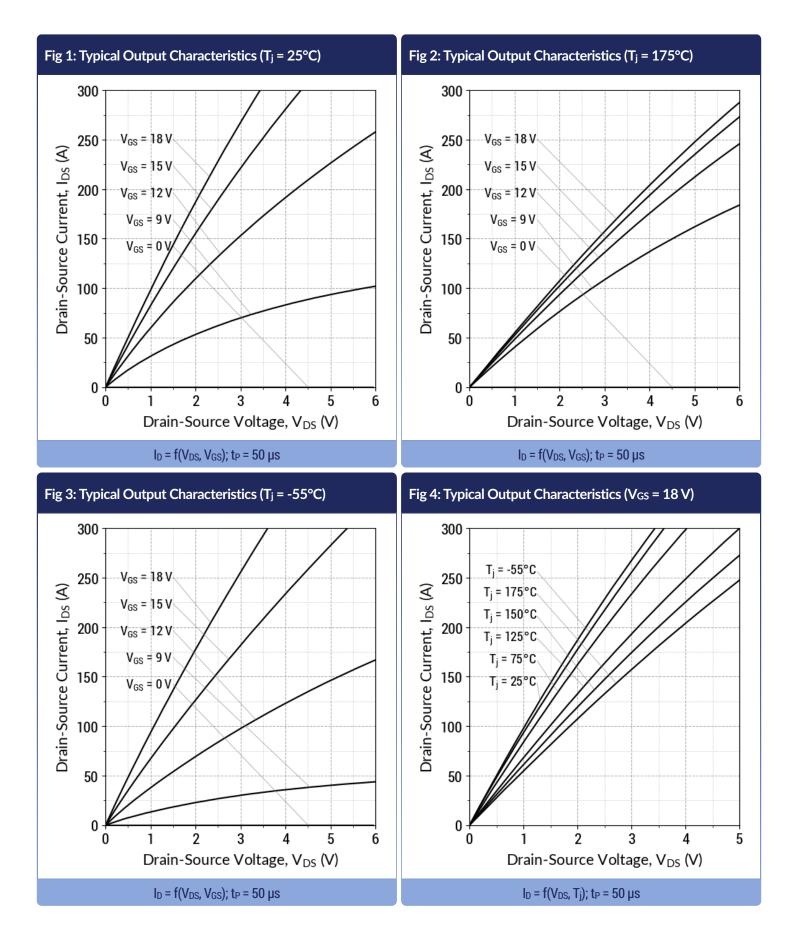
### NTC-Thermistor Characteristics

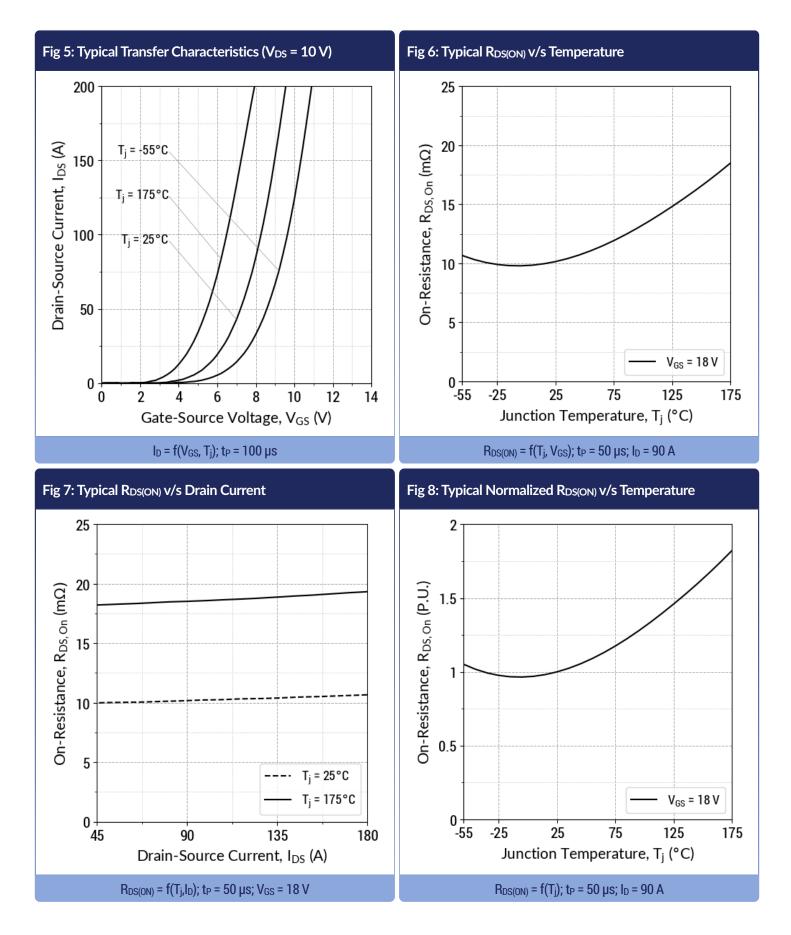
Parameter	Sumbol	Conditions		Values			Nata
Palameter	Symbol	Conditions	Min.	Тур.	Max.	Unit	Note
Rated Resistance	R <sub>NTC,25</sub>	T <sub>NTC</sub> = 25 °C		5		kΩ	
Resistance Tolerance	ΔR/R	T <sub>NTC</sub> = 25 °C	-5		+5	%	
Power Dissipation	P <sub>NTC,25</sub>	T <sub>NTC</sub> = 25 °C			20	mW	
	B <sub>25</sub> /B <sub>50</sub>	T <sub>2</sub> = 50 °C		3375			
Beta Value (B-value)	B <sub>25</sub> /B <sub>80</sub>	T <sub>2</sub> = 80 °C		3410		К	
	B <sub>25</sub> /B <sub>100</sub>	T <sub>2</sub> = 100 °C		3435			

skage F	Packing Method
PAK <sup>™</sup> F E	Box (Qty - 12)
PAK <sup>™</sup> F with TIM E	Box (Qty - 12)
F	PAK™ F I

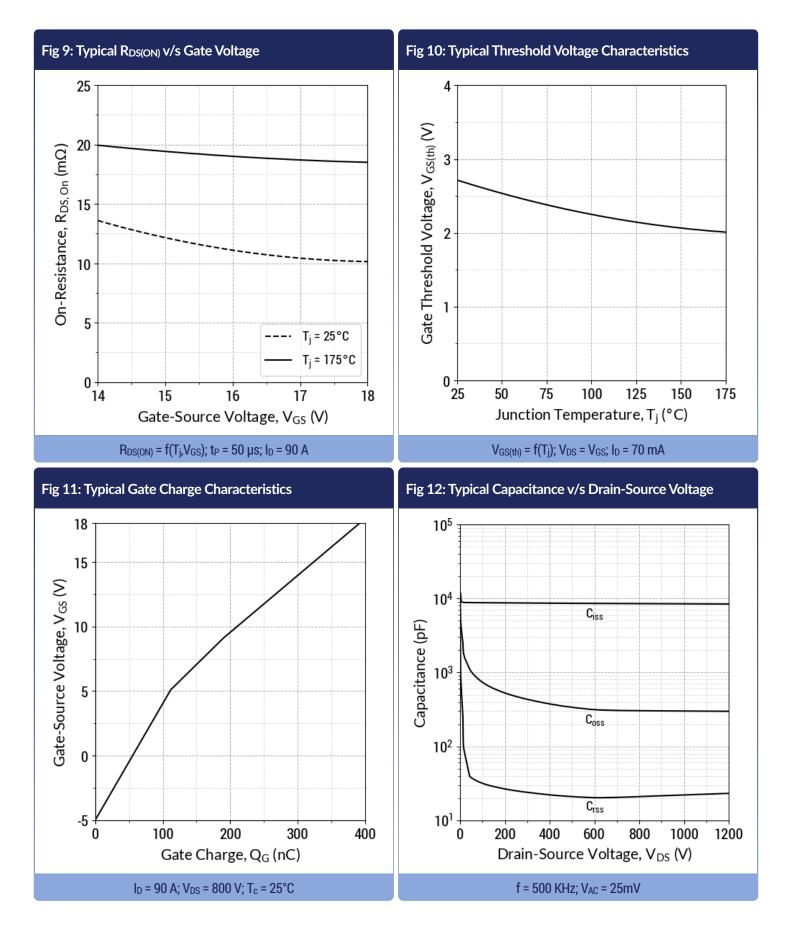
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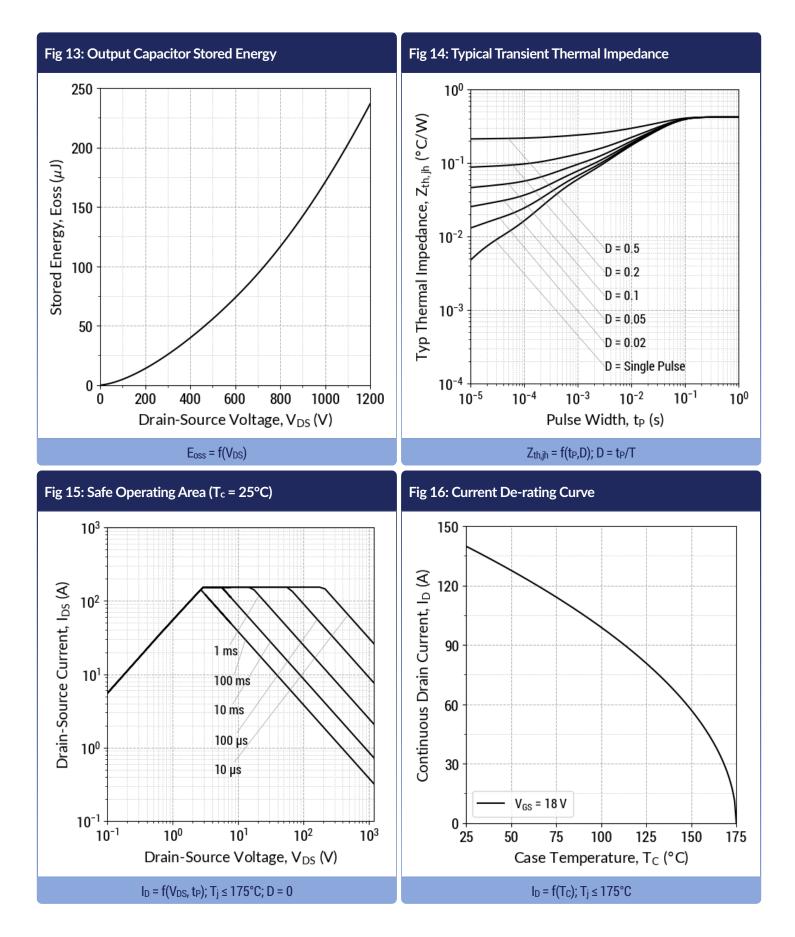
Note 4: Total effective resistance per switch postition (HS or LS) = MOSFET RDS(ON) + package resistance by switch position





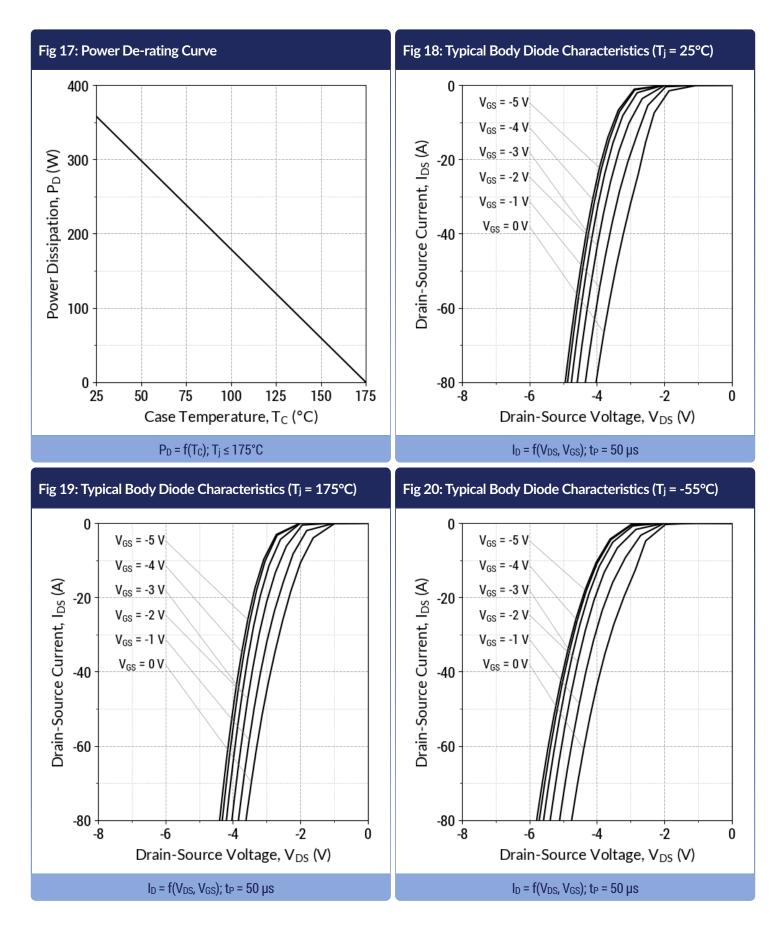
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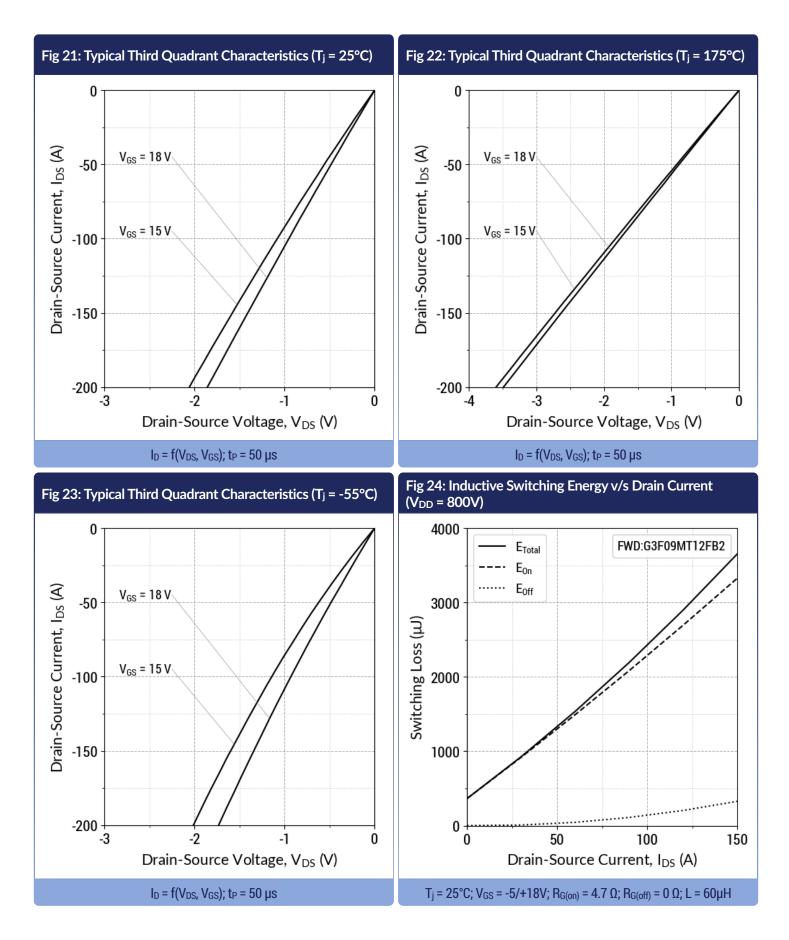
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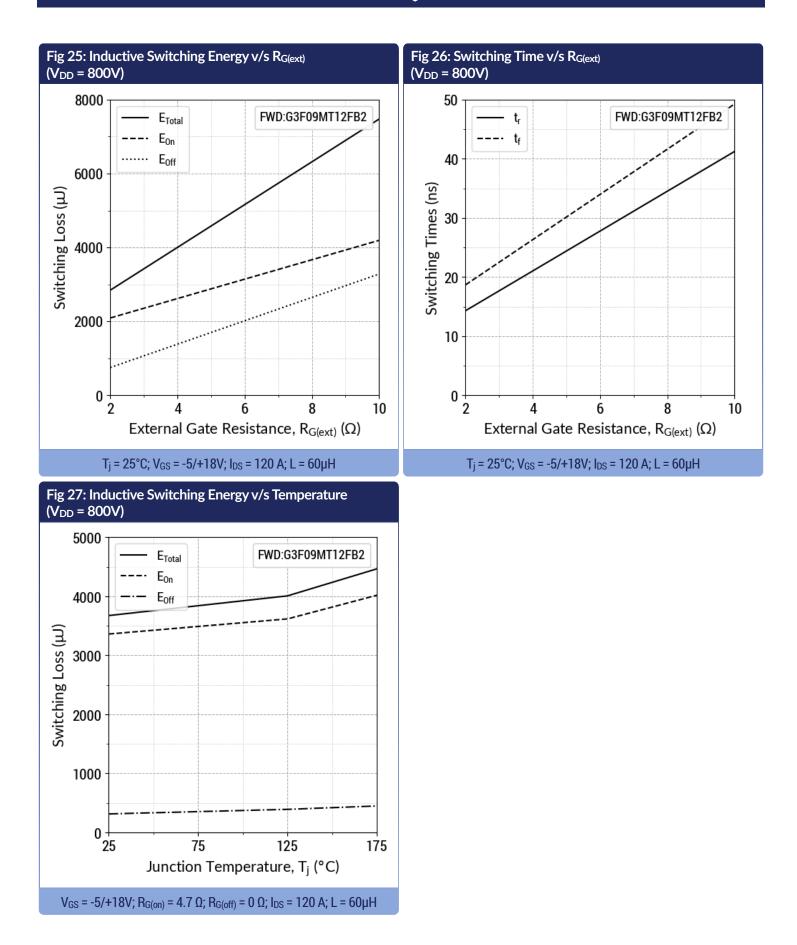
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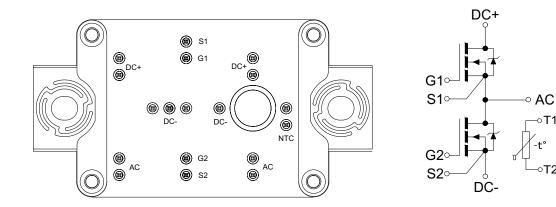
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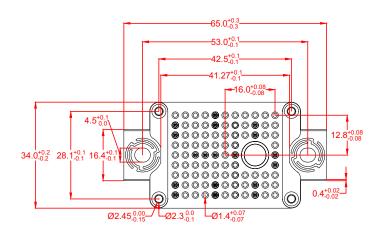


#### **ØGeneSiC**<sup>®</sup> G3F09MT12FB2

#### **Pinout and Package Dimensions**



TOP VIEW

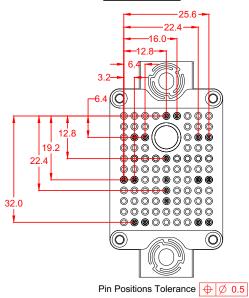


TOP VIEW

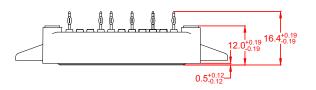
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-∘T2

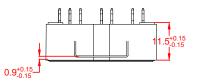
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SIDE VIEW







#### NOTES

1. Controlled dimension is millimeter (mm)

2. Dimensions do not include material protrusions

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