

650 V 28.5 mΩ SiC MOSFET

Silicon Carbide MOSFET

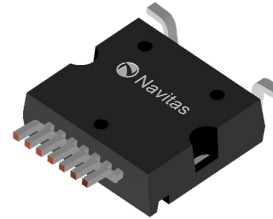
Trench-Assisted Planar Technology

V _{DS}	=	650 V
R _{DS(ON)(Typ.)}	=	28.5 mΩ
I _D (T _C = 100°C)	=	56 A

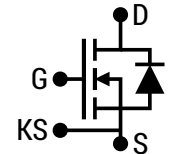
Features

- Gen3F (3rd Generation) Technology
- Most Stable R_{DS(ON)} over Temperature
- Low C_{OSS}, C_{RSS} and Balanced C_{ISS}/C_{RSS}
- Lower Q_{GD} and Balanced R_{G(INT)}
- Electromagnetically Optimized Design
- Robust Body Diode with Low V_F and Low Q_{RR}
- Superior Cost-Performance Index
- AEC-Q101 Qual in Progress and PPAP Capable

Package



HV-T2PAK



D = Drain (8-9, Tab)
 G = Gate (1)
 S = Source (3-7)
 KS = Kelvin Source (2)



Advantages

- Leading Performance and Robustness
- Lowest Conduction Losses at all Temperatures
- Lesser Switching Spikes and Lower Losses
- Faster and More Efficient Switching
- Reduced Ringing
- Ease of Paralleling without Thermal Runaway
- Excellent Power Density and System Efficiency
- Enhanced System Reliability

Applications

- xEV - OBC & DC-DC
- EV Fast Charging Infrastructure
- Solar / PV
- Energy Storage System
- Server & Telecom Power Supply
- Uninterruptible Power Supply
- Motor Control
- Class D Amplifiers

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	V _{DS(max)}	V _{GS} = 0 V, I _D = 100 μA	650	V	
Gate-Source Voltage (Dynamic)	V _{GS(max)}		-10 / +22	V	
Gate-Source Voltage (Static)	V _{GS(op)-ON}	Recommended Operation	15 to 18	V	Note 1
	V _{GS(op)-OFF}		-5 to -3		
Continuous Drain Current	I _D	T _C = 25°C, V _{GS} = -5 / +18 V	80	A	Fig. 16
		T _C = 100°C, V _{GS} = -5 / +18 V	56		
		T _C = 135°C, V _{GS} = -5 / +18 V	41		
Pulsed Drain Current	I _{D(pulse)}	t _p ≤ 3μs, D ≤ 1%, V _{GS} = 18 V	130	A	Note 2
Power Dissipation	P _D	T _C = 25°C	261	W	Fig. 17
Non-Repetitive Avalanche Energy	E _{AS}	L = 36 mH, I _{AV} = 4 A	288	mJ	
Operating Junction and Storage Temperature	T _j , T _{stg}		-55 to 175	°C	

Note 1: This product can support 0V turn-off gate drive voltage with optimized PCB layout and gate drive circuit configuration.

Note 2: Pulse Width t_p Limited by T_{j(max)}

NOTE: This datasheet provides preliminary specifications. Parameters, conditions and values are subject to change.

Electrical Characteristics (At $T_C = 25^\circ\text{C}$ Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	V_{DSS}	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	650			V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$		1	100	μA	
Gate Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 22\text{ V}$ $V_{DS} = 0\text{ V}, V_{GS} = -10\text{ V}$			100 -100	nA	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 12\text{ mA}$	2.2	2.7	4.3	V	Note 3
Transconductance	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 26\text{ A}$ $V_{DS} = 10\text{ V}, I_D = 26\text{ A}, T_j = 175^\circ\text{C}$		13.3 14.4		S	Fig. 5
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 18\text{ V}, I_D = 26\text{ A}, T_j = 175^\circ\text{C}$ $V_{GS} = 15\text{ V}, I_D = 26\text{ A}$ $V_{GS} = 15\text{ V}, I_D = 26\text{ A}, T_j = 175^\circ\text{C}$		28.5 40 38 46	38	m Ω	Fig. 5-9
Input Capacitance	C_{iss}			2394			
Output Capacitance	C_{oss}			163		pF	Fig. 12
Reverse Transfer Capacitance	C_{riss}			9.3			
C_{oss} Stored Energy	E_{oss}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$ $f = 500\text{ KHz}, V_{AC} = 25\text{ mV}$		15		μJ	Fig. 13
C_{oss} Stored Charge	Q_{oss}				104		nC
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			188			
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			260		pF	Note 4
Gate-Source Charge	Q_{gs}	$V_{DS} = 400\text{ V}, V_{GS} = -5 / +18\text{ V}$		20			
Gate-Drain Charge	Q_{gd}	$I_D = 26\text{ A}$		23		nC	Fig. 11
Total Gate Charge	Q_g	Per JEDEC JEP-192		81			
Internal Gate Resistance	$R_{G(int)}$	$V_{GS} = 18\text{ V}, f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$		1.3		Ω	
Turn-On Switching Energy (Body Diode)	E_{on}	$T_j = 25^\circ\text{C}, V_{GS} = -5/+18\text{V}, R_{G(ext)} = 4.7\ \Omega, L = 60.0\ \mu\text{H}, I_D = 26\text{ A}, V_{DD} = 400\text{ V}$		41		μJ	Fig. 24-27
Turn-Off Switching Energy (Body Diode)	E_{off}				21		
Turn-On Delay Time	$t_{d(on)}$			39			
Rise Time	t_r	$V_{DD} = 400\text{ V}, V_{GS} = -5/+18\text{V}$		12			
Turn-Off Delay Time	$t_{d(off)}$	$R_{G(ext)} = 4.7\ \Omega, L = 60.0\ \mu\text{H}, I_D = 26\text{ A}$		23		ns	Fig. 26
Fall Time	t_f	Timing relative to V_{DS} , Inductive load		11			

Note 3: Tested after applying 30ms pulse at $V_{GS} = +25\text{V}$

Note 4: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.
 $C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{oss} while V_{DS} is rising from 0 to 400V.

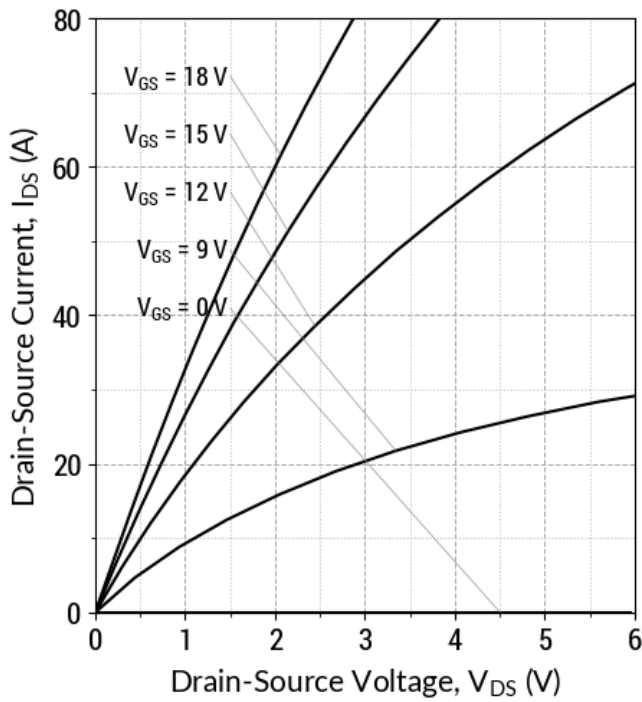
Reverse Diode Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	V_{SD}	$V_{GS} = -5\text{ V}, I_{SD} = 13\text{ A}$		4.3		V	Fig. 18-19
		$V_{GS} = -5\text{ V}, I_{SD} = 13\text{ A}, T_j = 175^\circ\text{C}$		3.8			
Continuous Diode Forward Current	I_S	$V_{GS} = -5\text{ V}, T_c = 25^\circ\text{C}$			42	A	
		$V_{GS} = -5\text{ V}, T_c = 100^\circ\text{C}$			25		
Diode Pulse Current	$I_{S(\text{pulse})}$	$V_{GS} = -5\text{ V}$		100		A	Note 2
Reverse Recovery Time	t_{rr}			12.5		ns	
Reverse Recovery Charge	Q_{rr}	$V_{GS} = -5\text{ V}, I_{SD} = 26\text{ A}, V_R = 400\text{ V}$ $dif/dt = 2400\text{ A}/\mu\text{s}, T_j = 25^\circ\text{C}$		130		nC	
Peak Reverse Recovery Current	I_{rm}			26		A	
Reverse Recovery Time	t_{rr}			15.5		ns	
Reverse Recovery Charge	Q_{rr}	$V_{GS} = -5\text{ V}, I_{SD} = 26\text{ A}, V_R = 400\text{ V}$ $dif/dt = 2400\text{ A}/\mu\text{s}, T_j = 175^\circ\text{C}$		250		nC	
Peak Reverse Recovery Current	I_{rm}			36		A	

Package Characteristics

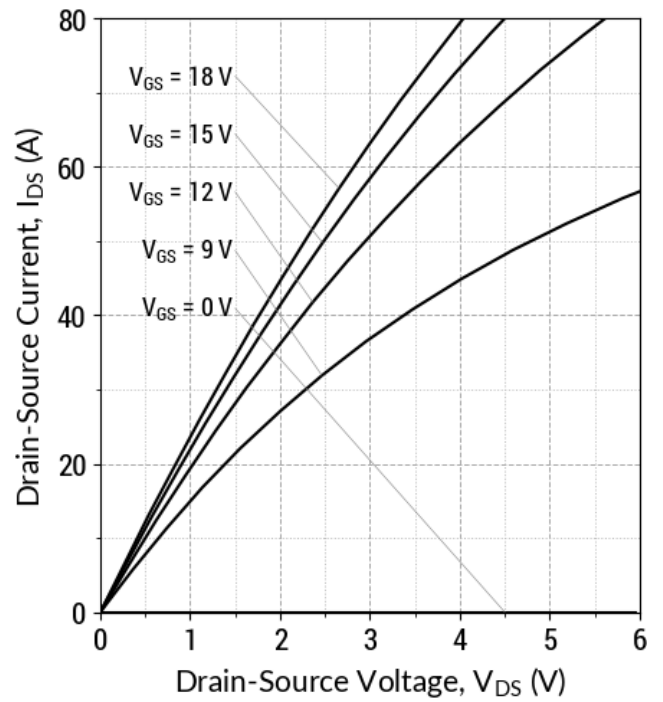
Parameter	Symbol	Conditions	Values	Unit	Note
Max Thermal Resistance, Junction - Case	$R_{thJC-Max}$	Maximum	0.57	$^\circ\text{C}/\text{W}$	Fig. 14
Weight	W_T		2.45	g	
Moisture Sensitivity Level	MSL		1		
EMC Material Group			II		

Fig 1: Typical Output Characteristics ($T_j = 25^\circ\text{C}$)



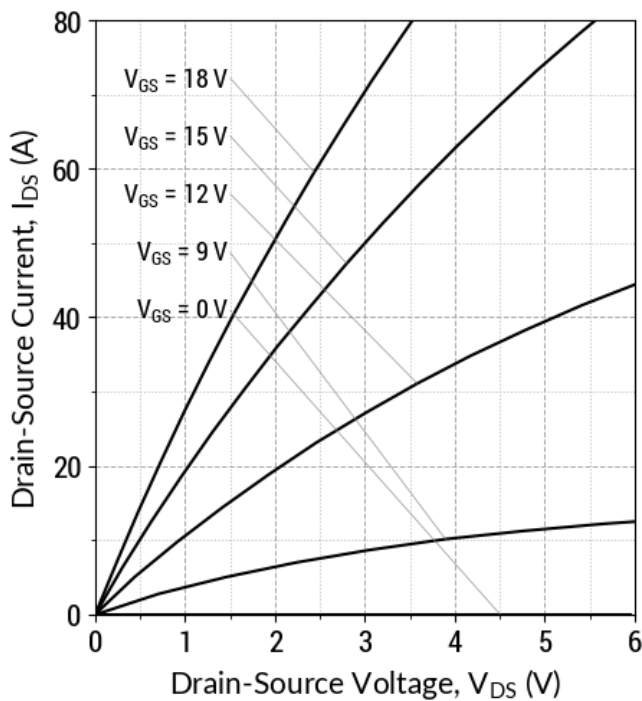
$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$

Fig 2: Typical Output Characteristics ($T_j = 175^\circ\text{C}$)



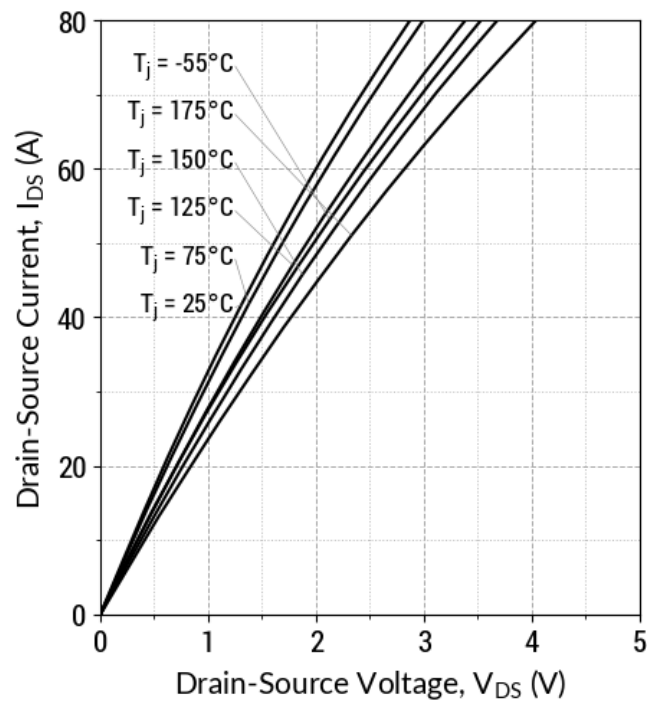
$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$

Fig 3: Typical Output Characteristics ($T_j = -55^\circ\text{C}$)



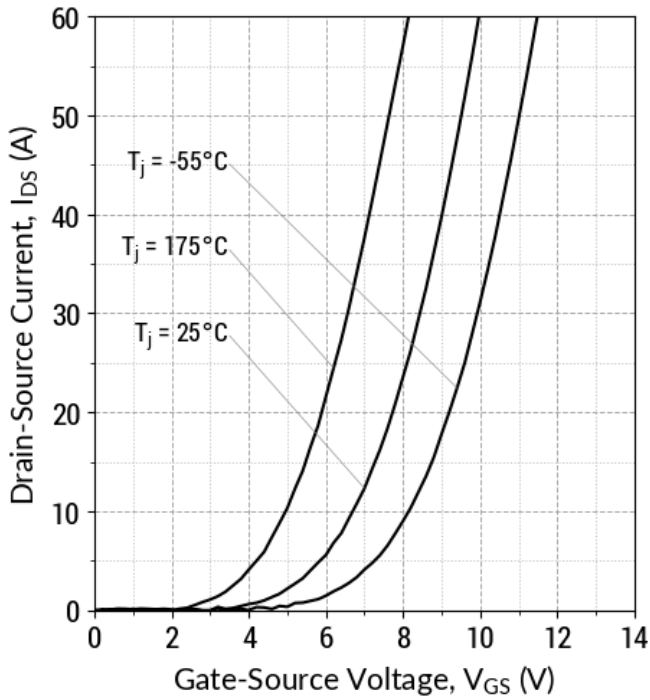
$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$

Fig 4: Typical Output Characteristics ($V_{GS} = 18\text{V}$)



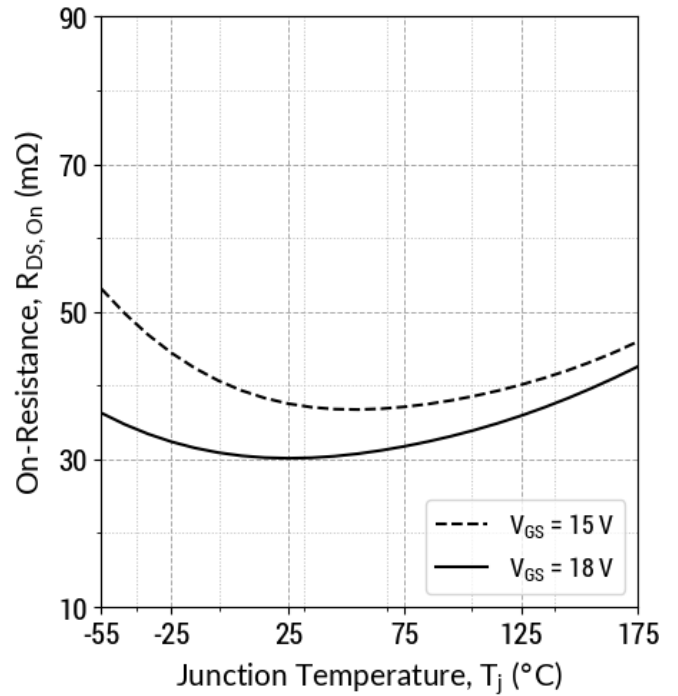
$I_D = f(V_{DS}, T_j); t_P = 50 \mu\text{s}$

Fig 5: Typical Transfer Characteristics ($V_{DS} = 10\text{ V}$)



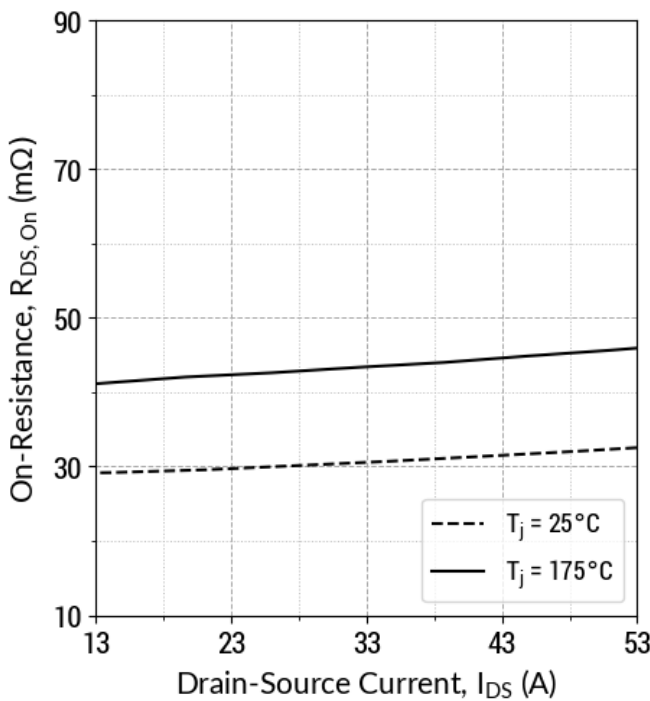
$I_D = f(V_{GS}, T_j); t_p = 100\ \mu\text{s}$

Fig 6: Typical $R_{DS(ON)}$ v/s Temperature



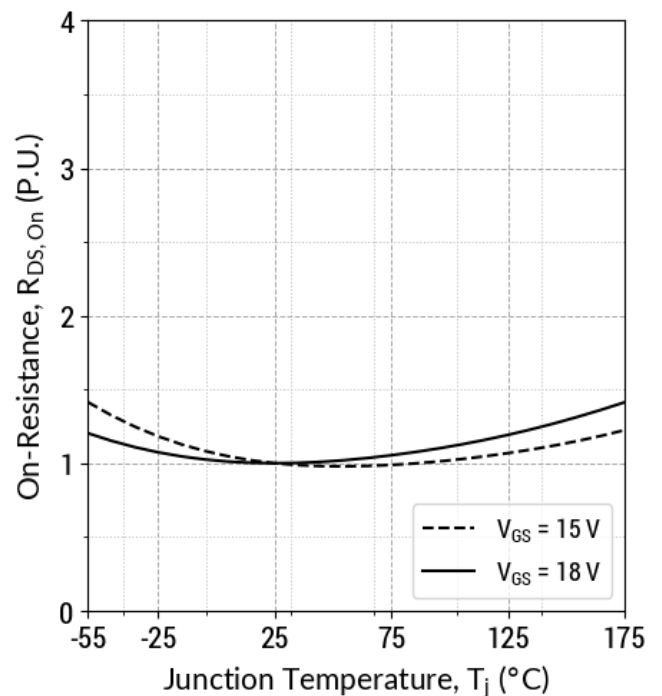
$R_{DS(ON)} = f(T_j, V_{GS}); t_p = 50\ \mu\text{s}; I_D = 26\text{ A}$

Fig 7: Typical $R_{DS(ON)}$ v/s Drain Current



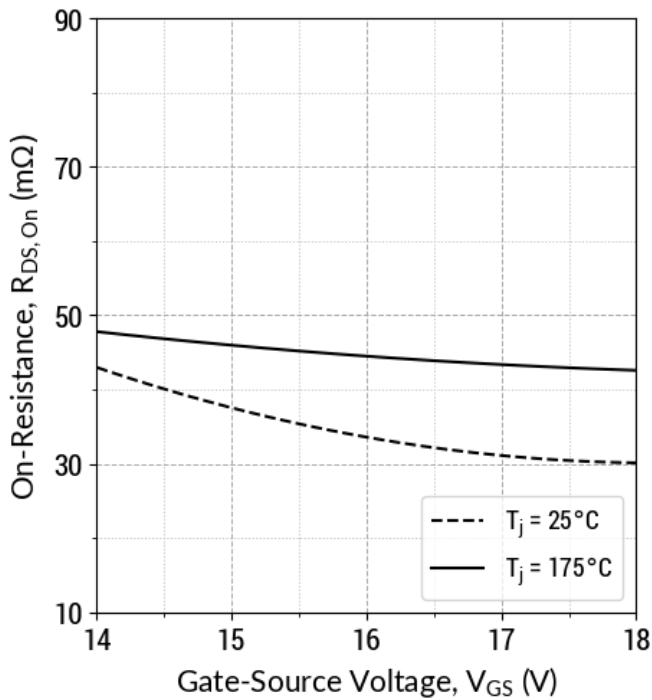
$R_{DS(ON)} = f(T_j, I_D); t_p = 50\ \mu\text{s}; V_{GS} = 18\text{ V}$

Fig 8: Typical Normalized $R_{DS(ON)}$ v/s Temperature



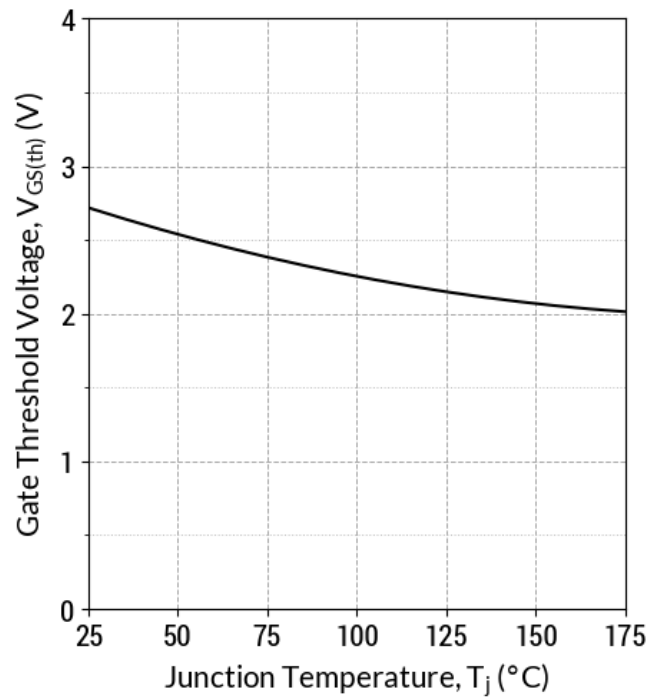
$R_{DS(ON)} = f(T_j); t_p = 50\ \mu\text{s}; I_D = 26\text{ A}$

Fig 9: Typical $R_{DS(ON)}$ v/s Gate Voltage



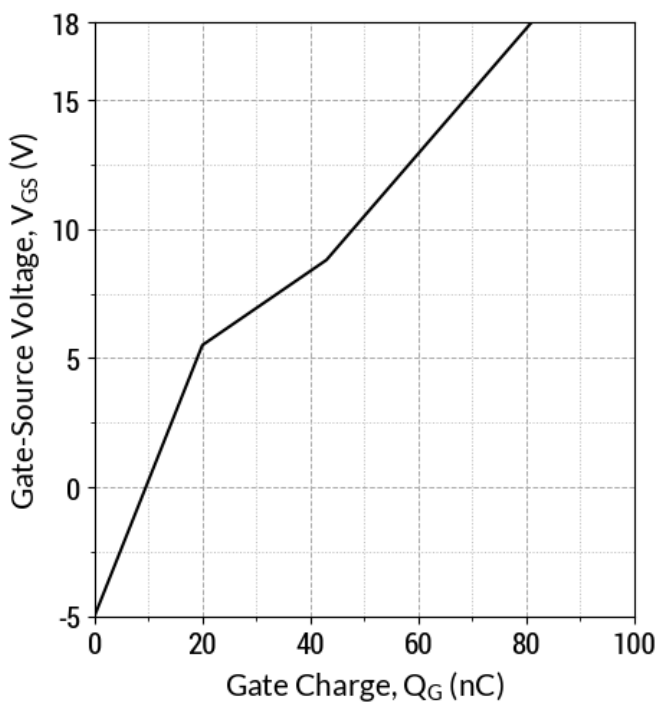
$R_{DS(ON)} = f(T_j, V_{GS}); t_p = 50 \mu\text{s}; I_D = 26 \text{ A}$

Fig 10: Typical Threshold Voltage Characteristics



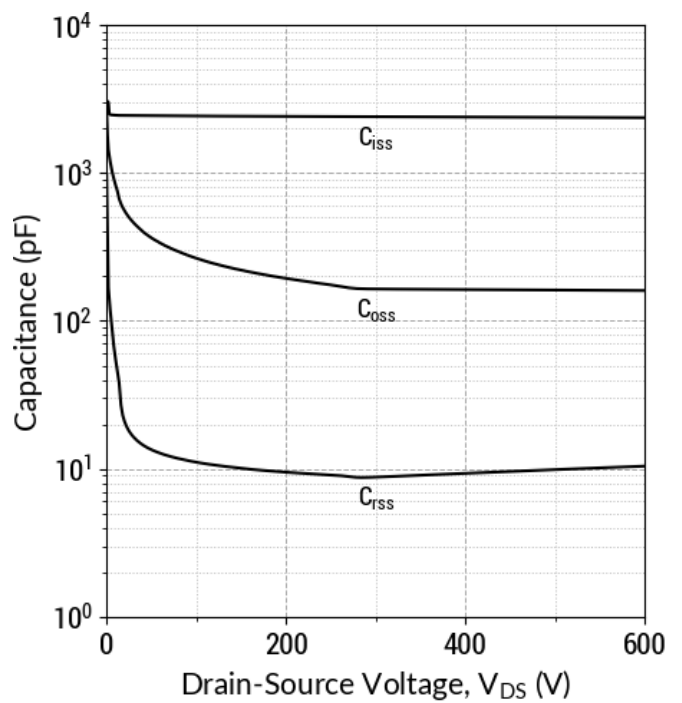
$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 12 \text{ mA}$

Fig 11: Typical Gate Charge Characteristics



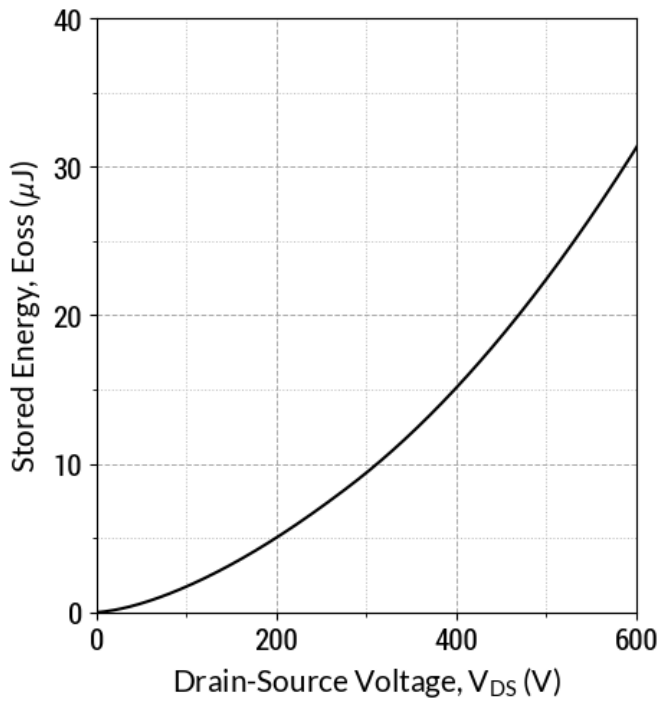
$I_D = 26 \text{ A}; V_{DS} = 400 \text{ V}; T_c = 25^\circ\text{C}$

Fig 12: Typical Capacitance v/s Drain-Source Voltage



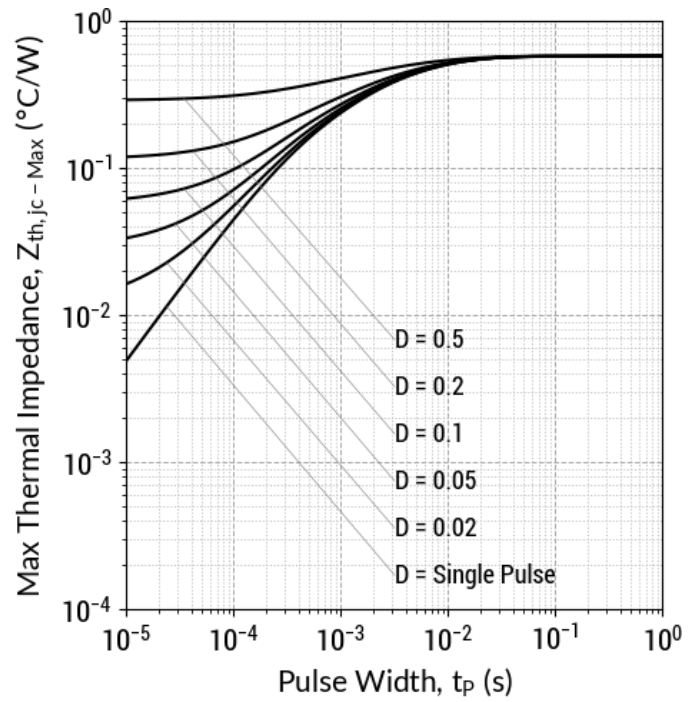
$f = 500 \text{ KHz}; V_{AC} = 25 \text{ mV}$

Fig 13: Output Capacitor Stored Energy



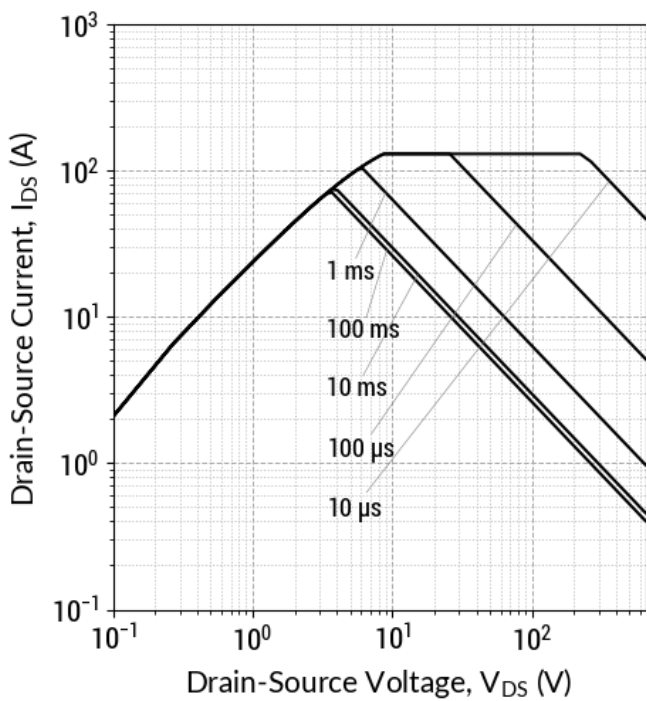
$E_{oss} = f(V_{DS})$

Fig 14: Max. Transient Thermal Impedance



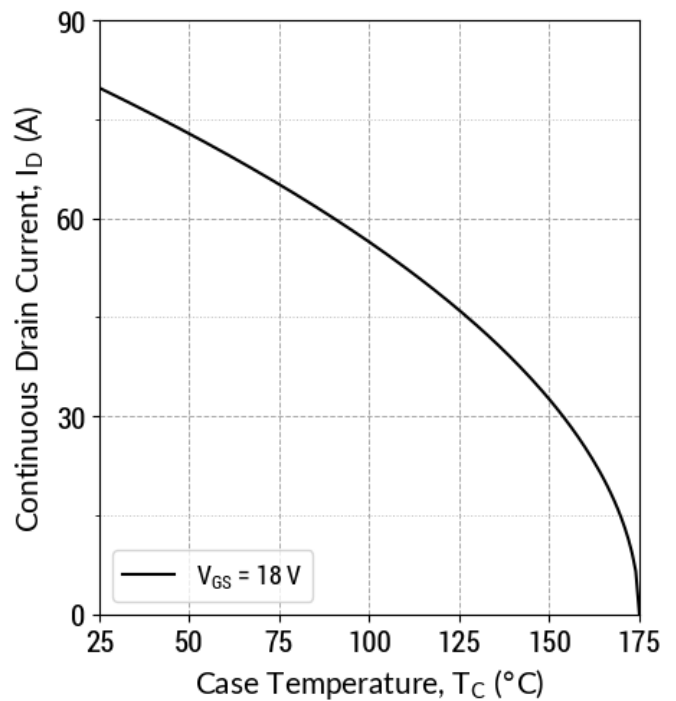
$Z_{th,jc} = f(t_p, D); D = t_p/T$

Fig 15: Safe Operating Area ($T_c = 25^{\circ}C$)



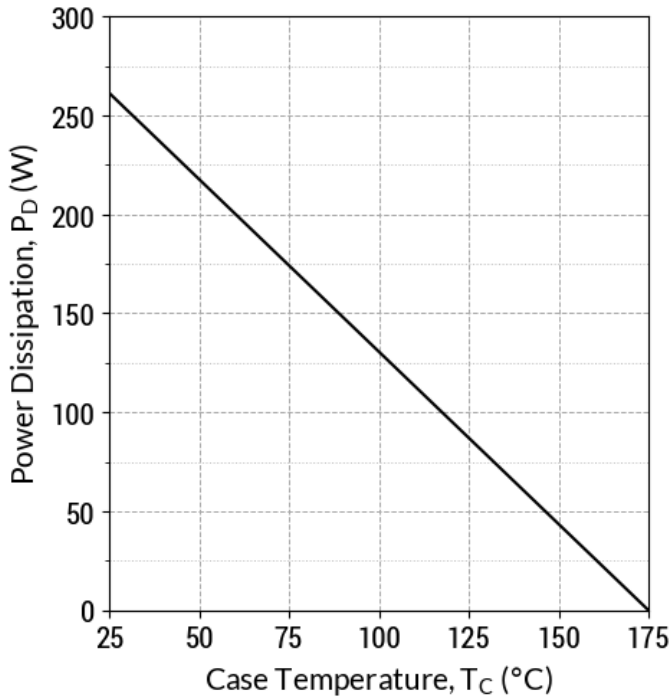
$I_D = f(V_{DS}, t_p); T_j \leq 175^{\circ}C; D = 0$

Fig 16: Current De-rating Curve



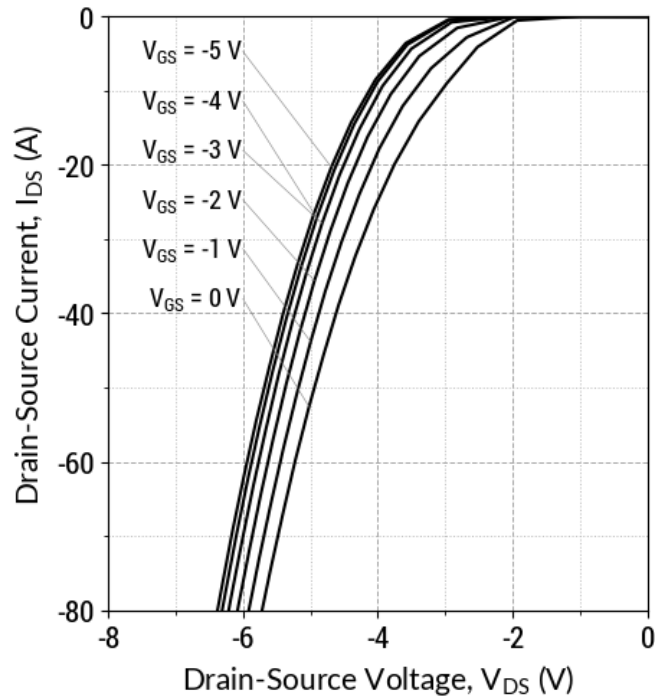
$I_D = f(T_C); T_j \leq 175^{\circ}C$

Fig 17: Power De-rating Curve



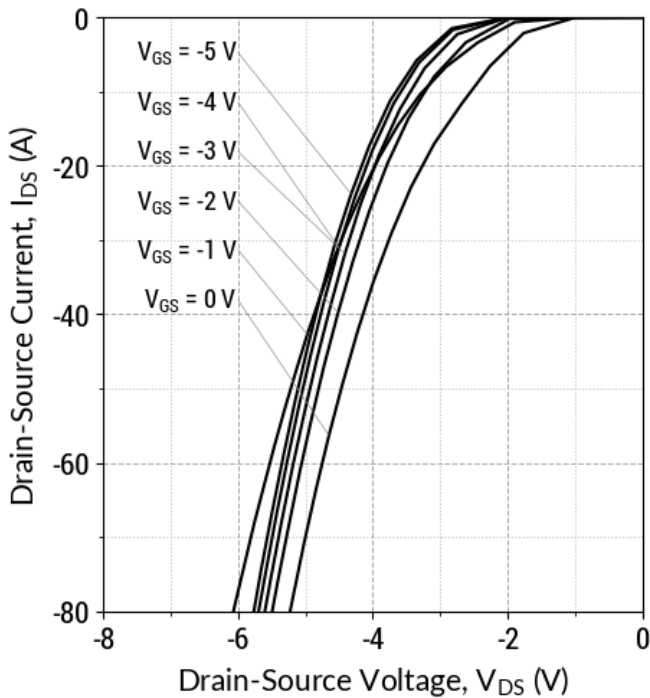
$P_D = f(T_C); T_j \leq 175^\circ\text{C}$

Fig 18: Typical Body Diode Characteristics ($T_j = 25^\circ\text{C}$)



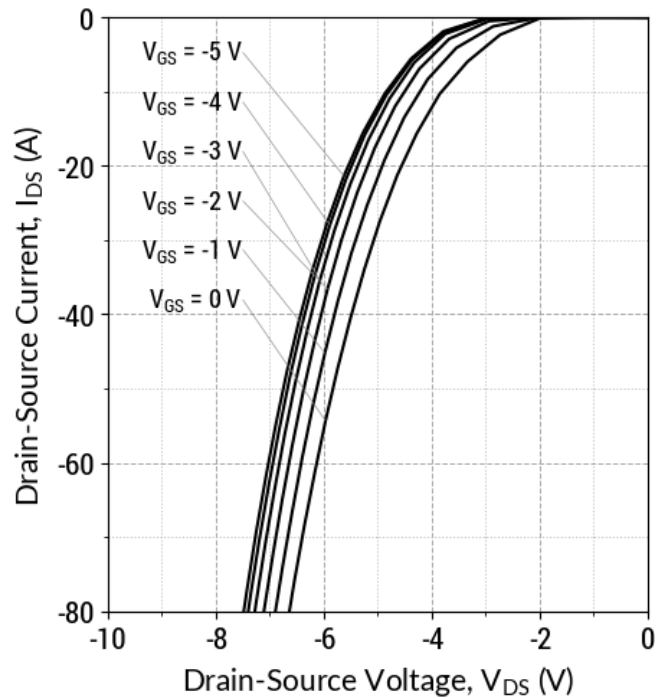
$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$

Fig 19: Typical Body Diode Characteristics ($T_j = 175^\circ\text{C}$)



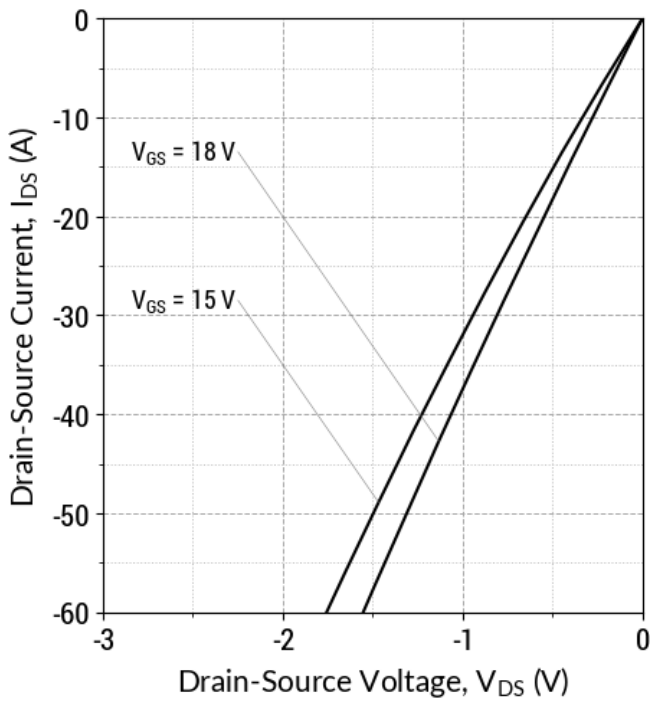
$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$

Fig 20: Typical Body Diode Characteristics ($T_j = -55^\circ\text{C}$)



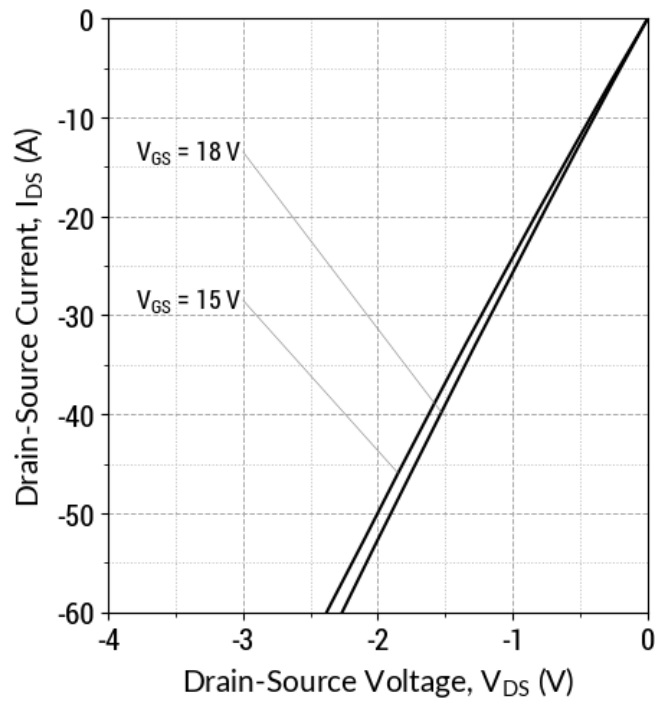
$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$

Fig 21: Typical Third Quadrant Characteristics ($T_j = 25^\circ\text{C}$)



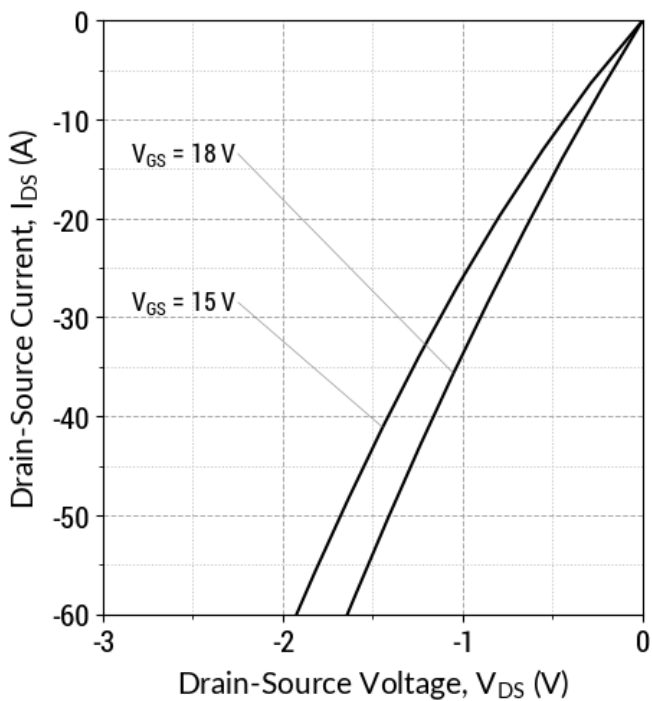
$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$

Fig 22: Typical Third Quadrant Characteristics ($T_j = 175^\circ\text{C}$)



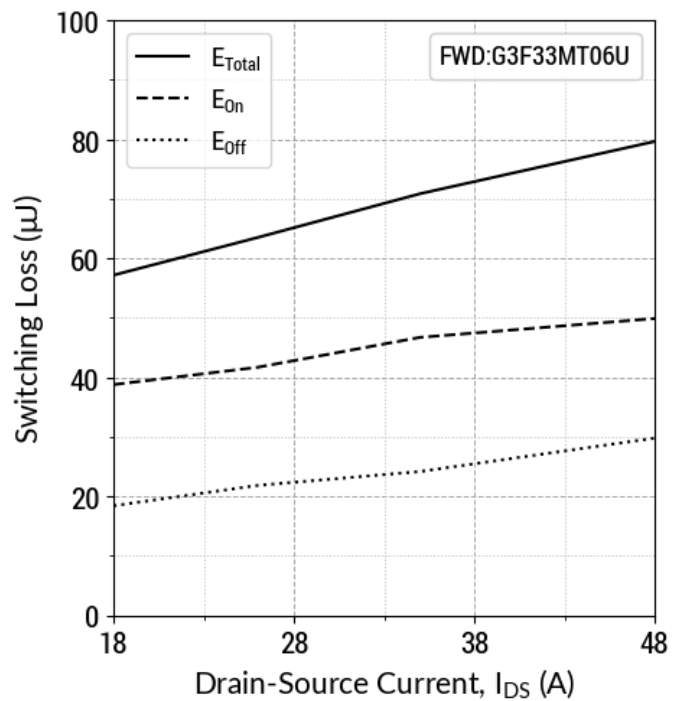
$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$

Fig 23: Typical Third Quadrant Characteristics ($T_j = -55^\circ\text{C}$)



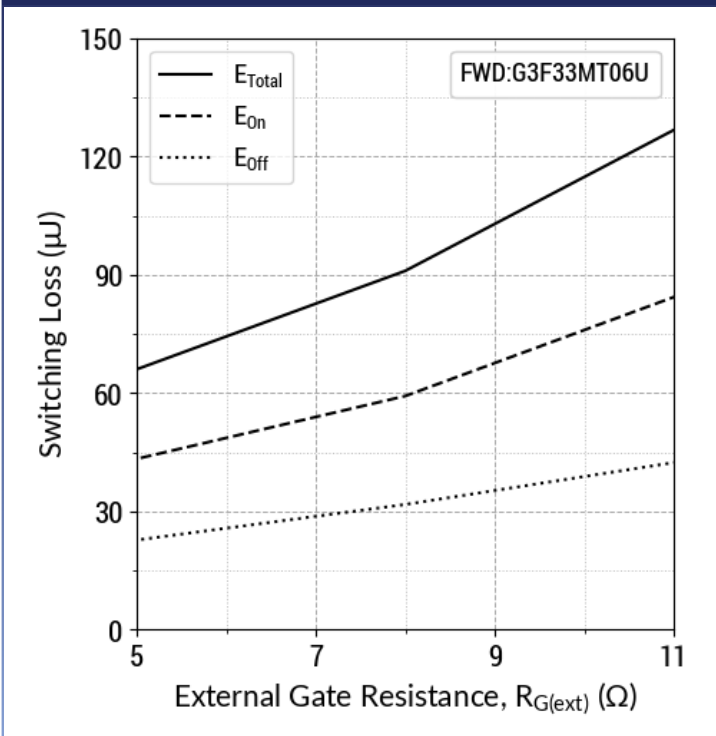
$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$

Fig 24: Inductive Switching Energy v/s Drain Current ($V_{DD} = 400\text{V}$)



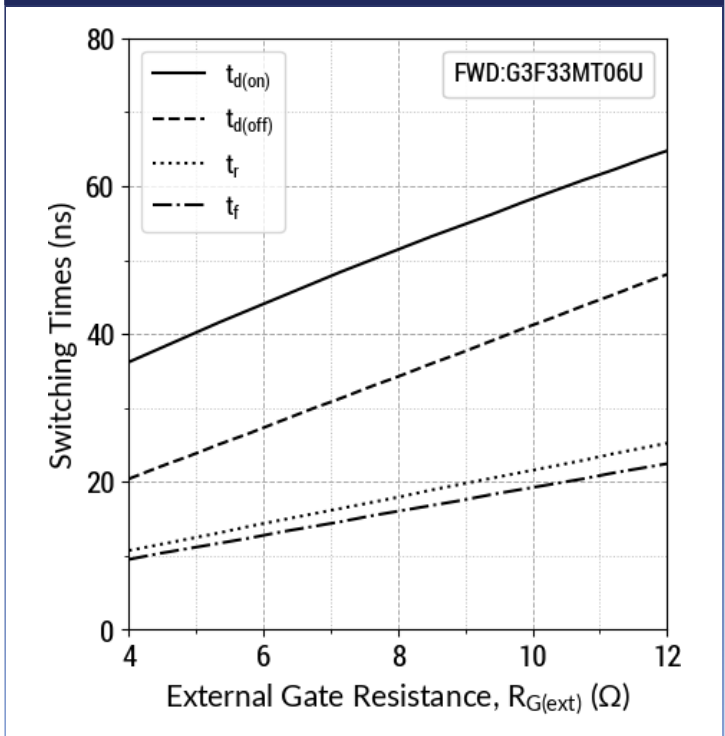
$T_j = 25^\circ\text{C}; V_{GS} = -5/+18\text{V}; R_{G(ext)} = 4.7 \Omega; L = 60.0 \mu\text{H}$

Fig 25: Inductive Switching Energy v/s $R_{G(ext)}$
($V_{DD} = 400V$)



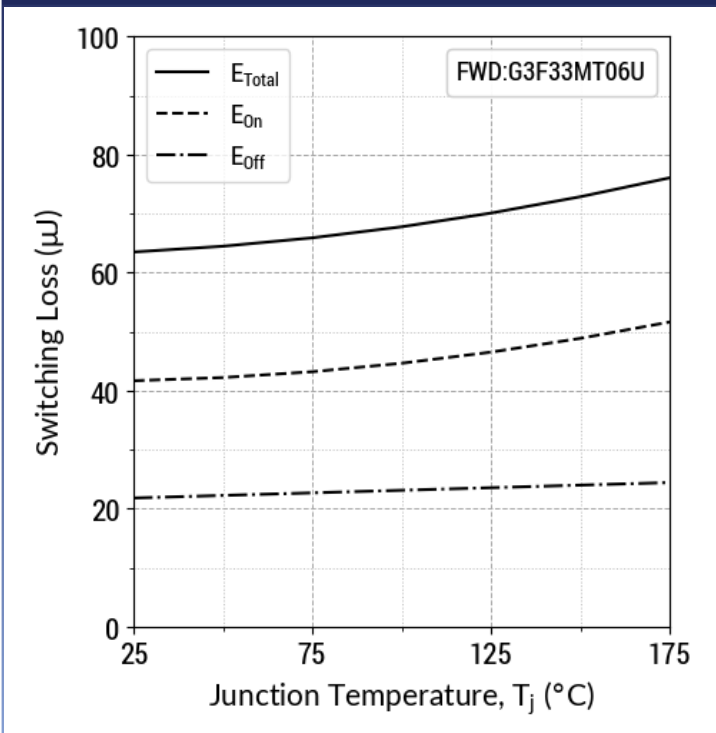
$T_j = 25^\circ C$; $V_{GS} = -5/+18V$; $I_{DS} = 26 A$; $L = 60.0\mu H$

Fig 26: Switching Time v/s $R_{G(ext)}$
($V_{DD} = 400V$)



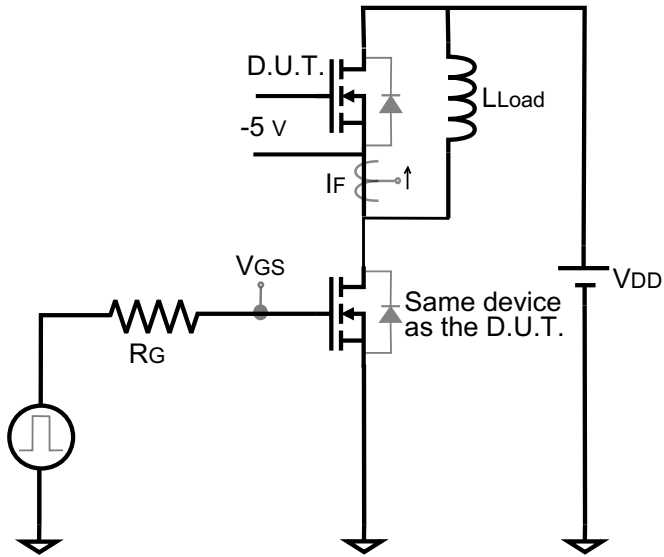
$T_j = 25^\circ C$; $V_{GS} = -5/+18V$; $I_{DS} = 26 A$; $L = 60.0\mu H$

Fig 27: Inductive Switching Energy v/s Temperature
($V_{DD} = 400V$)

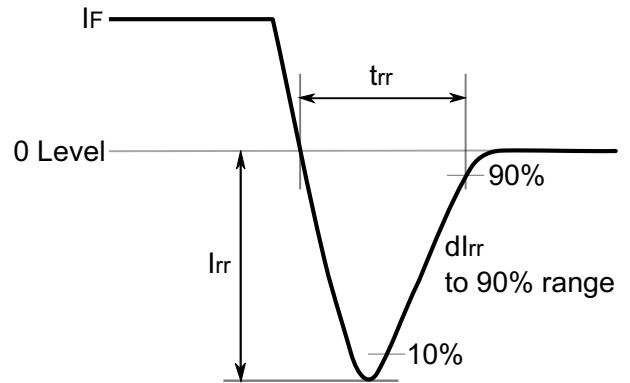


$T_j = 25^\circ C$; $V_{GS} = -5/+18V$; $R_{G(ext)} = 4.7 \Omega$; $I_{DS} = 26 A$; $L = 60.0\mu H$

Reverse Recovery Circuit

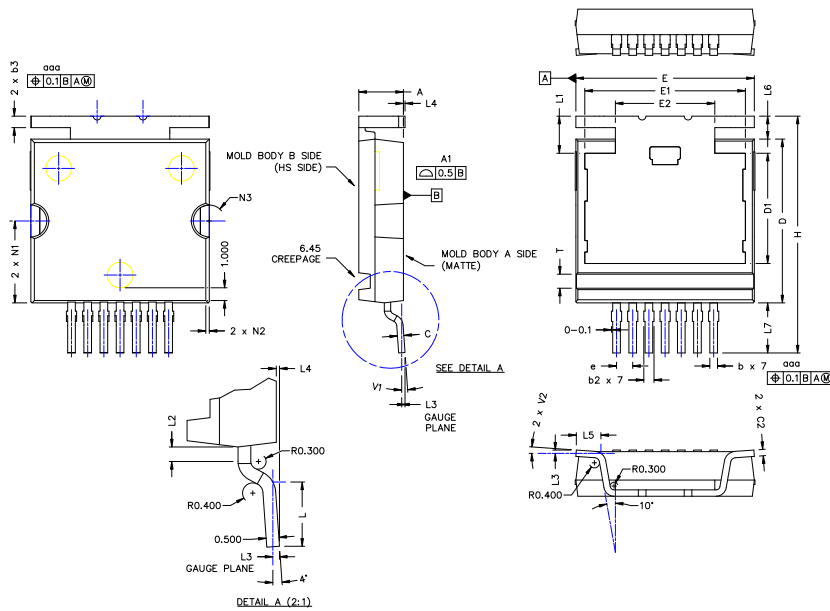


Reverse Recovery Waveform



Package Dimensions

HV-T2PAK Package Outline



SYM	MIN	NOM	MAX
A	-	3.50	-
A1	-	-	0.05
b	-	0.60	-
b2	-	0.80	-
b3	-	0.90	-
c	-	0.50	-
c2	-	0.50	-
D	-	12.85	-
D1	8.55	8.65	8.75
E	13.90	14.00	14.10
E1	12.50	12.60	12.70
E2	-	7.80	-
e	-	1.27	-
H	18.38	18.58	18.78
aaa	-	-	0.10
L	2.42	2.52	2.62
L1	-	2.95	-
L2	0.47	0.57	0.67
L3	-	0.26	-
L4	0.075	0.125	0.175
L5	1.83	1.93	2.03
L6	1.70	1.80	1.90
L7	3.83	3.93	4.03
N1	-	6.43	-
N2	-	0.30	-
N3	-	1.25	-
T	-	1.1	-
V1	0°	4°	8°
V2	0°	4°	8°

- NOTES:
- ALL DIMENSIONS IN MILLIMETERS.
 - ALL METAL SURFACES WITH TIN PLATED EXCEPT AREA OF CUT AND HEATSINK.
 - ALL DIMENSIONS ARE PARTIAL AND SUBJECT TO CHANGE UPON DESIGN REVIEW.
 - DIMENSIONS EXCLUDED TIN PLATING THICKNESS.
GENERAL TIN PLATING THICKNESS: 15±5 UM.
 - GENERAL RADIUS OF EDGE AND CORNER: R IS 0.2 MM.
 - MOLD BODY A SIDE: Ra: 0.8 ~ 1.2 UM.
 - MOLD BODY B SIDE (HS SIDE): Ra: 0.8 ~ 1.2 UM.
 - UNLESS OTHERWISE SPECIFIED.
DECIMAL ANGULAR
X.X±0.1 X±1°
X.XX±0.05 X.XX±0.1°
X.XXX±0.025

NOTE

- CONTROLLED DIMENSION IS MILLIMETER.
- DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

Revision History

- Rev 24/Sep: Preliminary Specification

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