650 V 42 mΩ SiC MOSFET

Silicon Carbide MOSFET

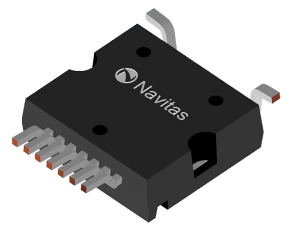
Trench-Assisted Planar Technology

V_{DS}	=	650 V
$R_{DS(ON)}$(Typ.)	=	42 mΩ
I_D (T_C = 100°C)	=	39 A

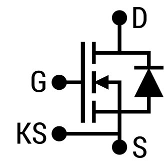
Features

- Gen3F (3rd Generation) Technology
- Most Stable $R_{DS(ON)}$ over Temperature
- Low C_{OSS}, C_{RSS} and Balanced C_{ISS}/C_{RSS}
- Lower Q_{GD} and Balanced $R_{G(INT)}$
- Electromagnetically Optimized Design
- Robust Body Diode with Low V_F and Low Q_{RR}
- Superior Cost-Performance Index
- AEC-Q101 Qual in Progress and PPAP Capable

Package



HV-T2PAK



D = Drain (8-9, Tab)
G = Gate (1)
S = Source (3-7)
KS = Kelvin Source (2)

RoHS
REACH
AEC Q101

Advantages

- Leading Performance and Robustness
- Lowest Conduction Losses at all Temperatures
- Lesser Switching Spikes and Lower Losses
- Faster and More Efficient Switching
- Reduced Ringing
- Ease of Paralleling without Thermal Runaway
- Excellent Power Density and System Efficiency
- Enhanced System Reliability

Applications

- xEV - OBC & DC-DC
- EV Fast Charging Infrastructure
- Solar / PV
- Energy Storage System
- Server & Telecom Power Supply
- Uninterruptible Power Supply
- Motor Control
- Class D Amplifiers

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µA	650	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +22	V	
Gate-Source Voltage (Static)	$V_{GS(op)-ON}$ $V_{GS(op)-OFF}$	Recommended Operation	15 to 18 -5 to -3	V	Note 1
Continuous Drain Current	I_D	T_C = 25°C, V_{GS} = -5 / +18 V T_C = 100°C, V_{GS} = -5 / +18 V T_C = 135°C, V_{GS} = -5 / +18 V	56 39 29	A	Fig. 16
Pulsed Drain Current	$I_{D(pulse)}$	$t_P \leq$ 3µs, D ≤ 1%, V_{GS} = 18 V	100	A	Note 2
Power Dissipation	P_D	T_c = 25°C	187	W	Fig. 17
Non-Repetitive Avalanche Energy	E_{AS}	L = 36 mH, I_{AV} = 3 A	162	mJ	
Operating Junction and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

Note 1: This product can support 0V turn-off gate drive voltage with optimized PCB layout and gate drive circuit configuration.

Note 2: Pulse Width t_P Limited by $T_{j(max)}$

NOTE: This datasheet provides preliminary specifications. Parameters, conditions and values are subject to change.

Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	650			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V		1	100	µA	
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 22 V			100	nA	
		V_{DS} = 0 V, V_{GS} = -10 V			-100		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 8 mA	2.2	2.8	4.3	V	Note 3
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 20 A		10.8		S	Fig. 5
		V_{DS} = 10 V, I_D = 20 A, T_j = 175°C		10.5			
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 18 V, I_D = 20 A		42	54	mΩ	Fig. 5-9
		V_{GS} = 18 V, I_D = 20 A, T_j = 175°C		60			
		V_{GS} = 15 V, I_D = 20 A		55			
		V_{GS} = 15 V, I_D = 20 A, T_j = 175°C		68			
Input Capacitance	C_{iss}	V_{DS} = 400 V, V_{GS} = 0 V f = 500 KHz, V_{AC} = 25mV		1640		pF	Fig. 12
Output Capacitance	C_{oss}			112			
Reverse Transfer Capacitance	C_{rss}			5.6			
C_{oss} Stored Energy	E_{oss}			10		µJ	Fig. 13
C_{oss} Stored Charge	Q_{oss}			71		nC	
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			125		pF	Note 4
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			178			
Gate-Source Charge	Q_{gs}	V_{DS} = 400 V, V_{GS} = -5 / +18 V I_D = 20 A Per JEDEC JEP-192		13		nC	Fig. 11
Gate-Drain Charge	Q_{gd}			16			
Total Gate Charge	Q_g			55			
Internal Gate Resistance	$R_{G(int)}$	V_{GS} = 18 V, f = 1 MHz, V_{AC} = 25 mV		1.0		Ω	
Turn-On Switching Energy (Body Diode)	E_{On}	T_j = 25°C, V_{GS} = -5/+18V, $R_{G(ext)}$ = 6.8 Ω, L = 80.0 µH, I_D = 20 A, V_{DD} = 400 V		67		µJ	Fig. 24-27
Turn-Off Switching Energy (Body Diode)	E_{Off}			34			
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, V_{GS} = -5/+18V $R_{G(ext)}$ = 6.8 Ω, L = 80.0 µH, I_D = 20 A Timing relative to V_{DS}, Inductive load		21		ns	Fig. 26
Rise Time	t_r			9			
Turn-Off Delay Time	$t_{d(off)}$			16			
Fall Time	t_f			8			

Note 3: Tested after applying 30ms pulse at Vgs= +25V

Note 4: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400V.
$C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{OSS} while V_{DS} is rising from 0 to 400V.

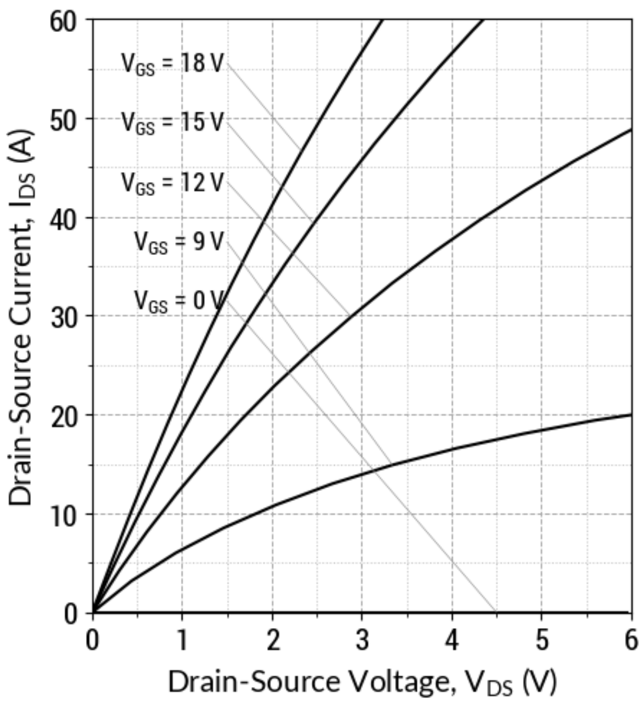
Reverse Diode Characteristics

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 10 A		4.4		V	Fig. 18-19
		V_{GS} = -5 V, I_{SD} = 10 A, T_j = 175°C		3.9			
Continuous Diode Forward Current	I_S	V_{GS} = -5 V, T_c = 25°C			30	A	
		V_{GS} = -5 V, T_c = 100°C			18		
Diode Pulse Current	$I_{S(pulse)}$	V_{GS} = -5 V		72		A	Note 2
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 20 A, V_R = 400 V dif/dt = 4800 A/µs, T_j = 25°C		8		ns	
Reverse Recovery Charge	Q_{rr}			83		nC	
Peak Reverse Recovery Current	I_{rrm}			17		A	
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 20 A, V_R = 400 V dif/dt = 4800 A/µs, T_j = 175°C		9.5		ns	
Reverse Recovery Charge	Q_{rr}			158		nC	
Peak Reverse Recovery Current	I_{rrm}			24		A	

Package Characteristics

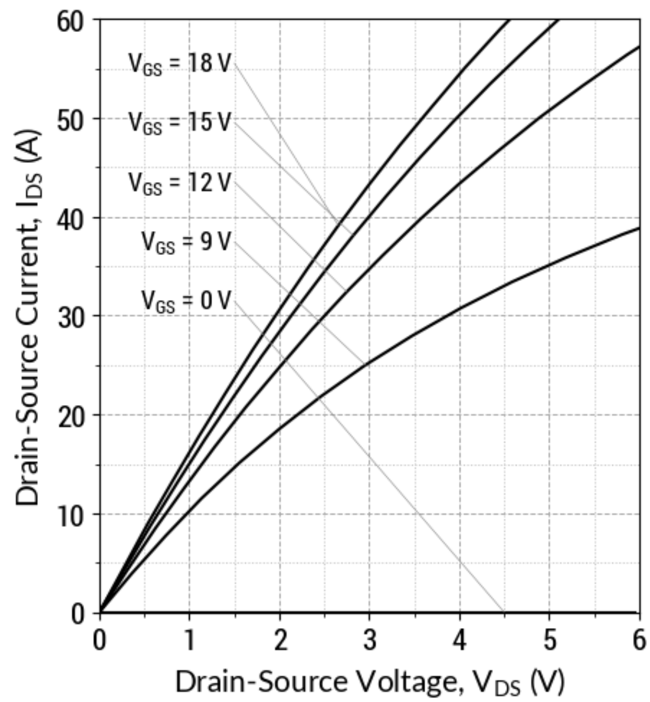
Parameter	Symbol	Conditions	Values	Unit	Note
Max Thermal Resistance, Junction - Case	$R_{thJC-Max}$	Maximum	0.8	°C/W	Fig. 14
Weight	W_T		1.5	g	
Moisture Sensitivity Level	MSL		1		
EMC Material Group			II		

Fig 1: Typical Output Characteristics (T_j = 25°C)



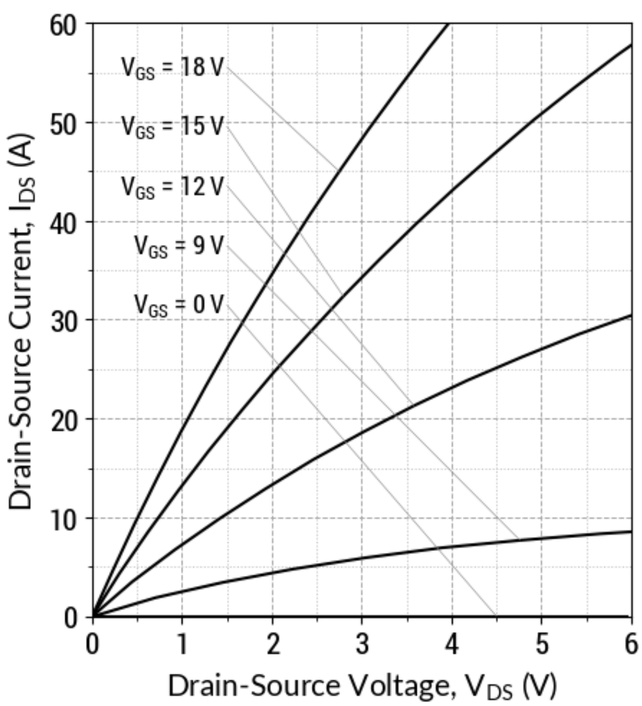
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 2: Typical Output Characteristics (T_j = 175°C)



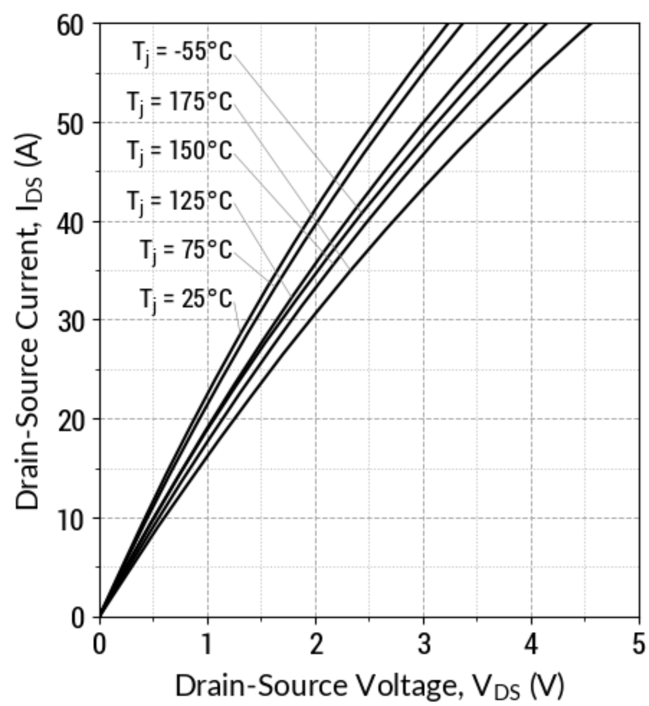
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 3: Typical Output Characteristics (T_j = -55°C)



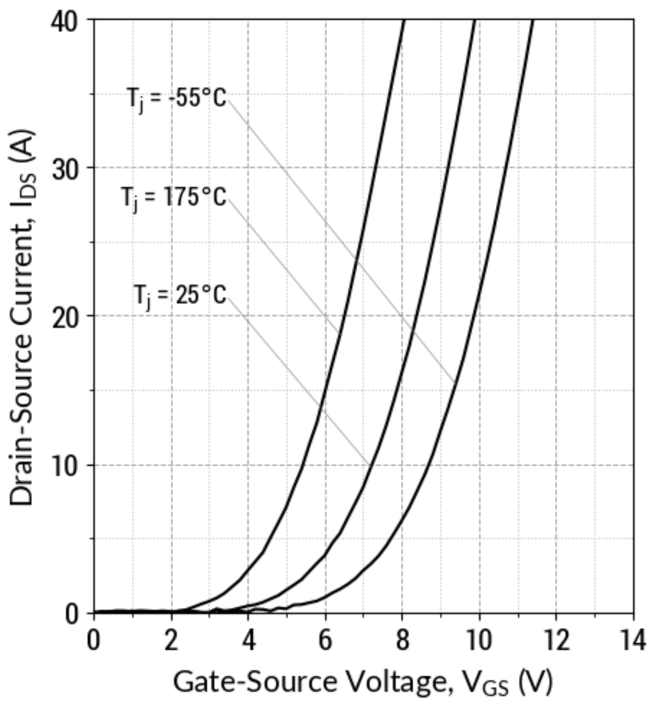
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 4: Typical Output Characteristics (V_{GS} = 18 V)



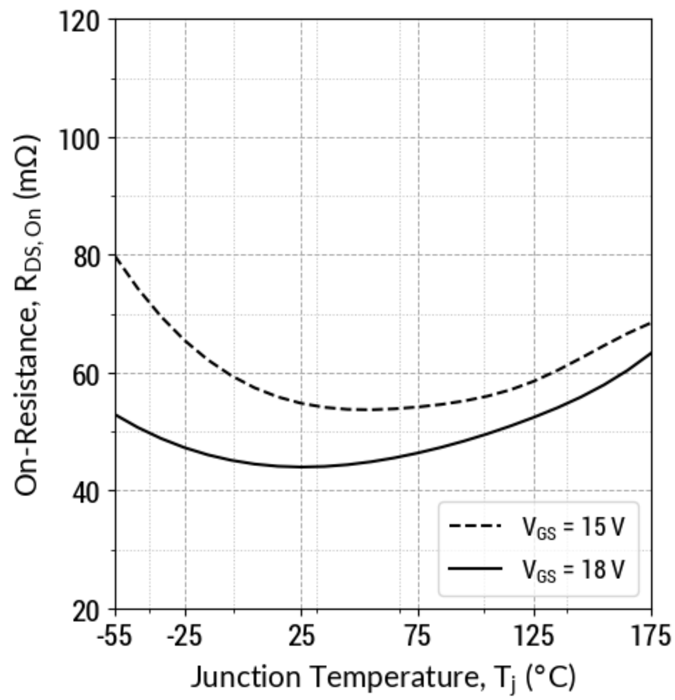
$I_D = f(V_{DS}, T_j)$; t_P = 50 µs

Fig 5: Typical Transfer Characteristics (V_{DS} = 10 V)



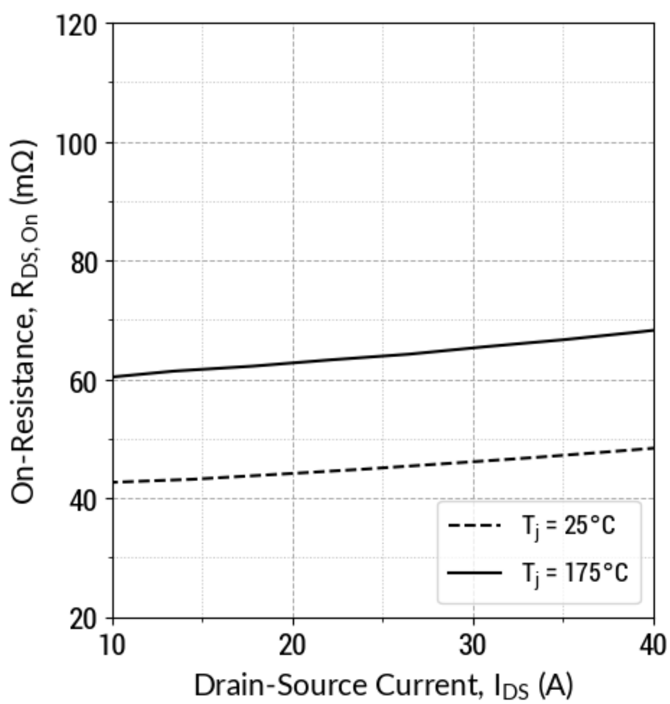
$I_D = f(V_{GS}, T_j)$; t_P = 100 µs

Fig 6: Typical $R_{DS(ON)}$ v/s Temperature



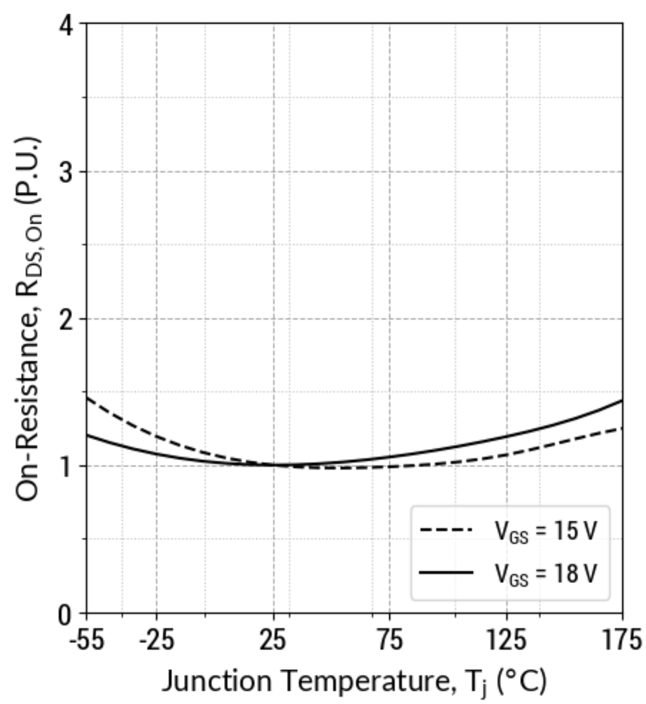
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 50 µs; I_D = 20 A

Fig 7: Typical $R_{DS(ON)}$ v/s Drain Current



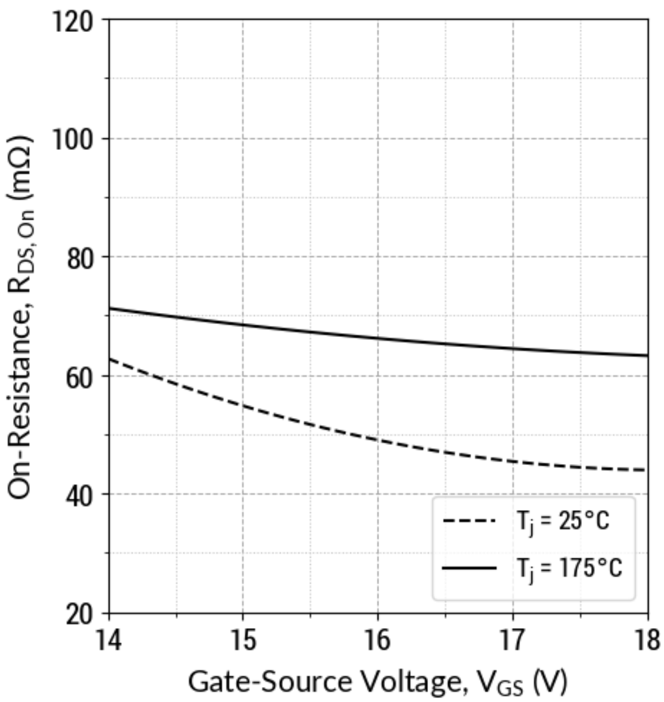
$R_{DS(ON)} = f(T_j, I_D)$; t_P = 50 µs; V_{GS} = 18 V

Fig 8: Typical Normalized $R_{DS(ON)}$ v/s Temperature



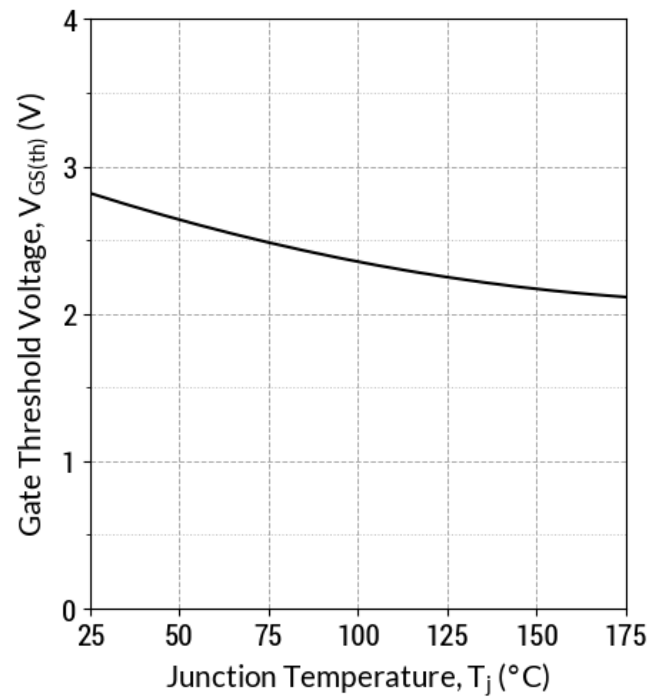
$R_{DS(ON)} = f(T_j)$; t_P = 50 µs; I_D = 20 A

Fig 9: Typical $R_{DS(ON)}$ v/s Gate Voltage



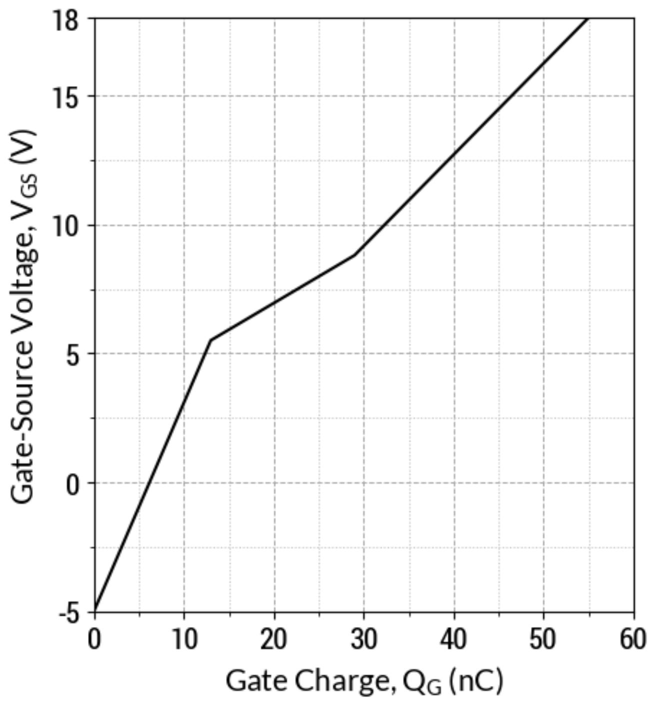
$R_{DS(ON)} = f(T_j,V_{GS})$; $t_P = 50$ µs; $I_D = 20$ A

Fig 10: Typical Threshold Voltage Characteristics



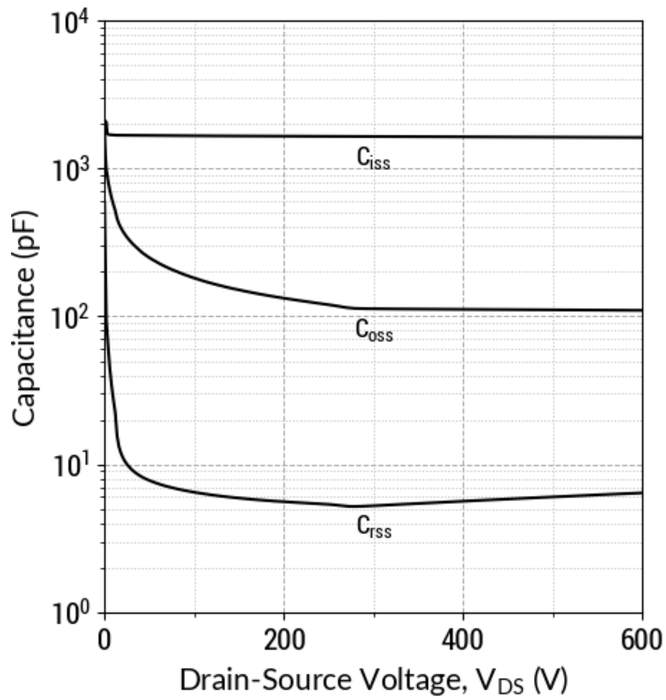
$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; $I_D = 8$ mA

Fig 11: Typical Gate Charge Characteristics



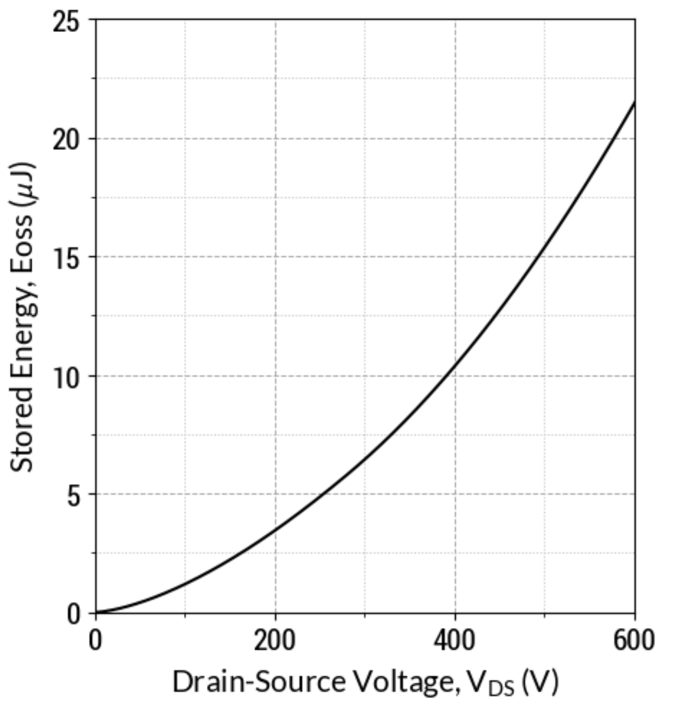
$I_D = 20$ A; $V_{DS} = 400$ V; $T_c = 25$°C

Fig 12: Typical Capacitance v/s Drain-Source Voltage



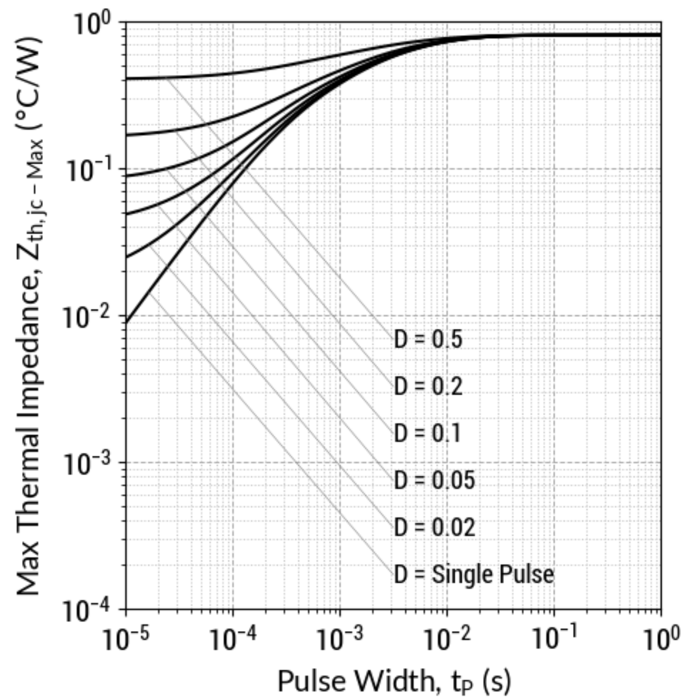
f = 500 KHz; $V_{AC} = 25$mV

Fig 13: Output Capacitor Stored Energy



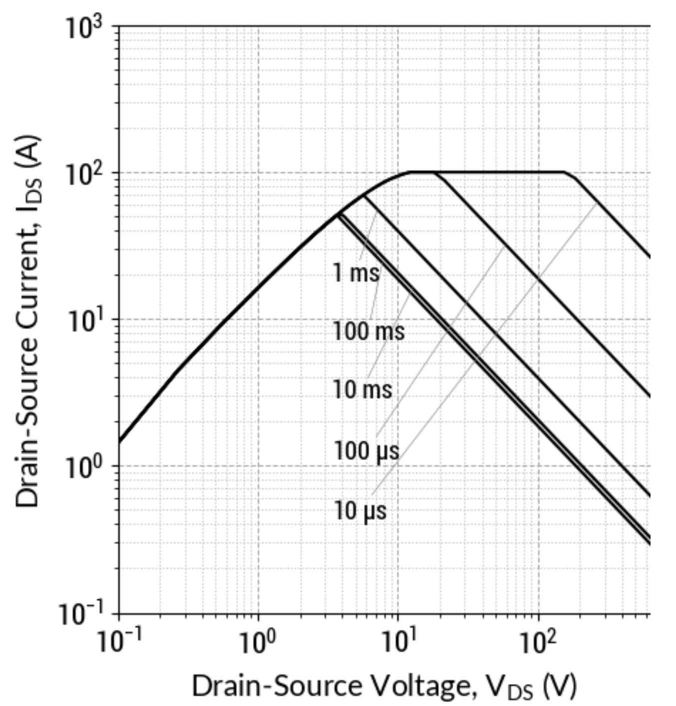
$E_{oss} = f(V_{DS})$

Fig 14: Max. Transient Thermal Impedance



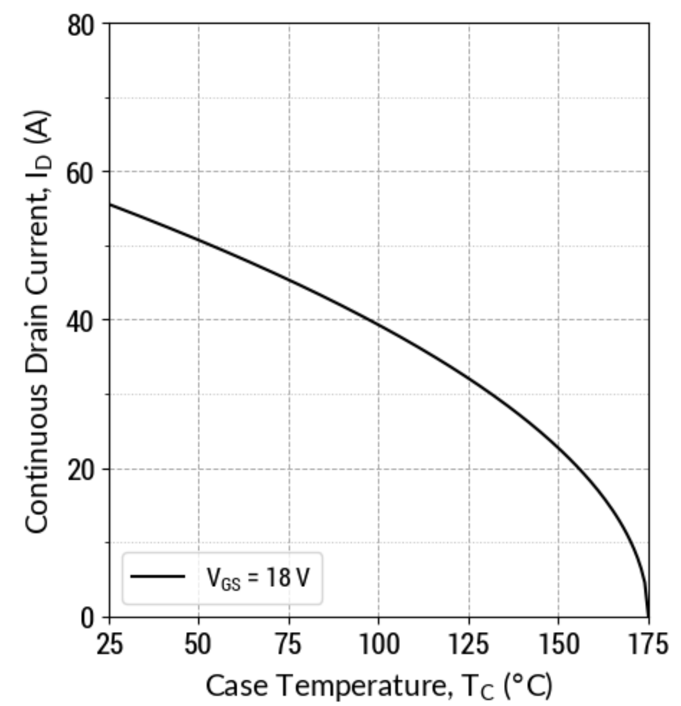
$Z_{th,jc} = f(t_P, D)$; $D = t_P/T$

Fig 15: Safe Operating Area (T_c = 25°C)



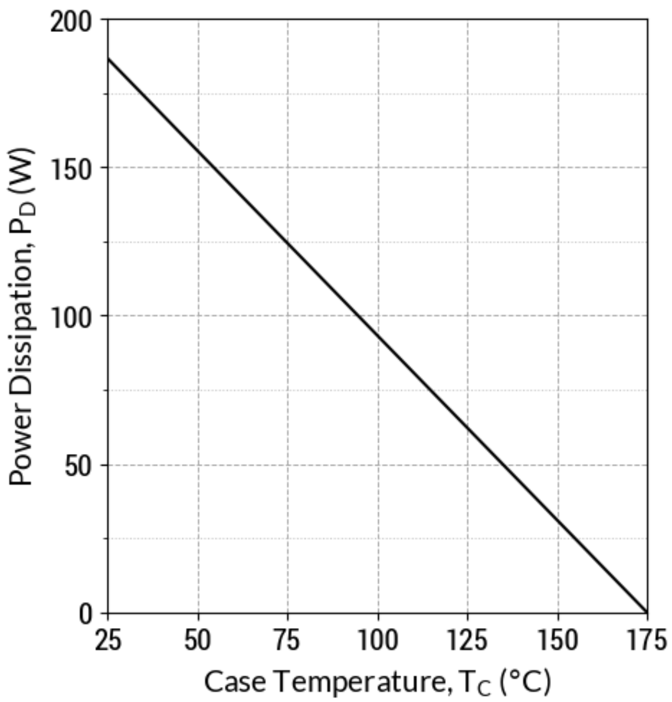
$I_D = f(V_{DS}, t_P)$; $T_j \leq 175°C$; $D = 0$

Fig 16: Current De-rating Curve



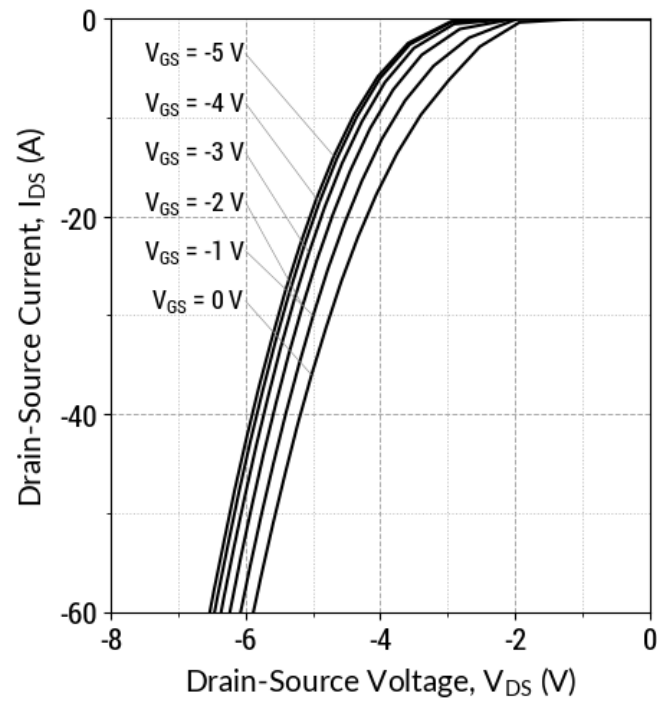
$I_D = f(T_C)$; $T_j \leq 175°C$

Fig 17: Power De-rating Curve



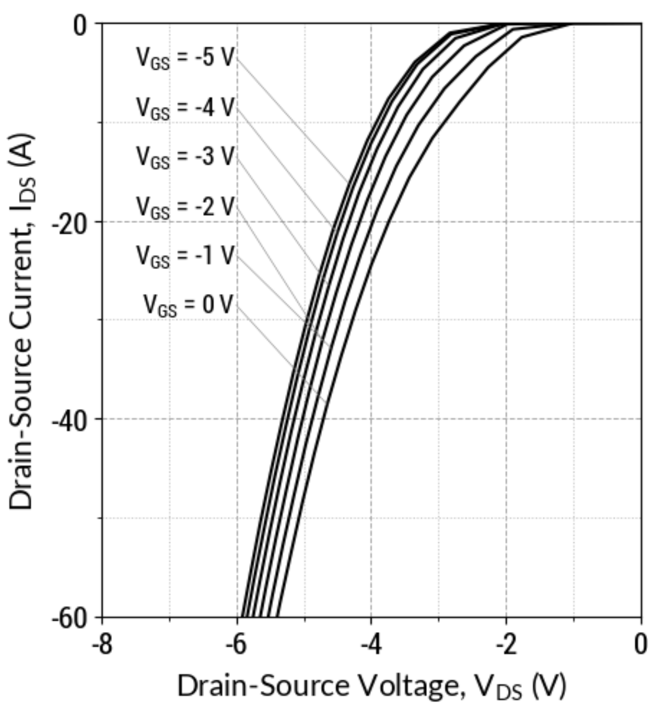
$P_D = f(T_C)$; $T_j \leq 175°C$

Fig 18: Typical Body Diode Characteristics (T_j = 25°C)



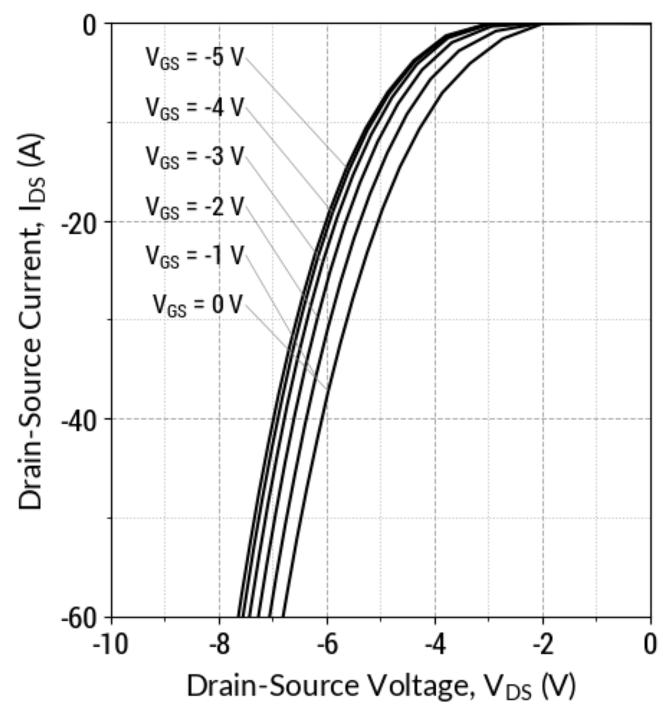
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 19: Typical Body Diode Characteristics (T_j = 175°C)



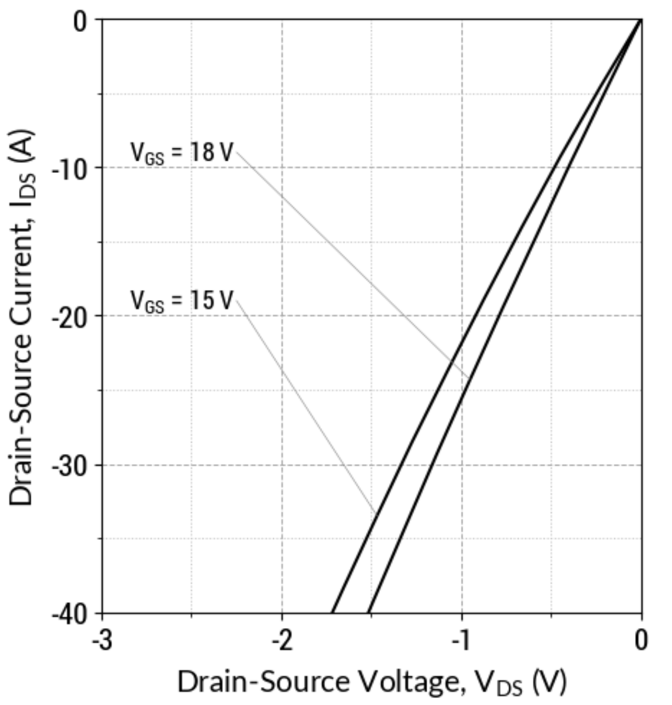
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 20: Typical Body Diode Characteristics (T_j = -55°C)



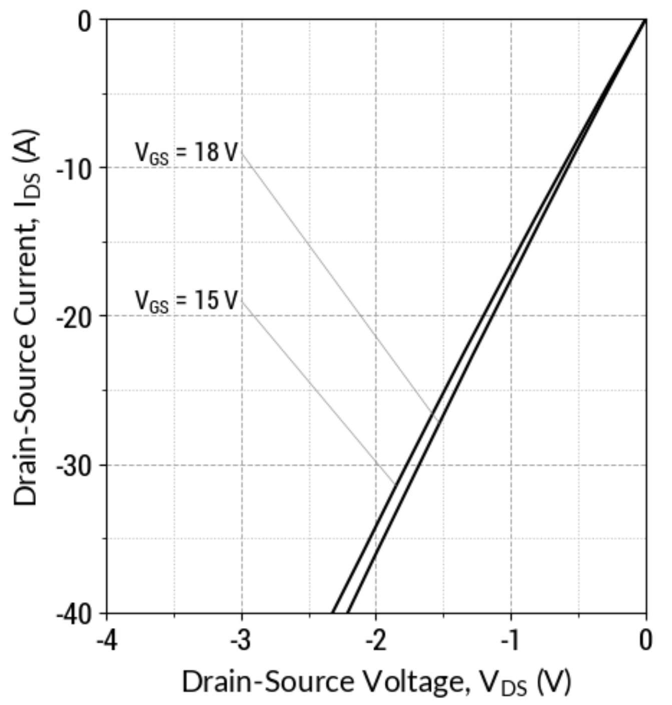
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 21: Typical Third Quadrant Characteristics (T_j = 25°C)



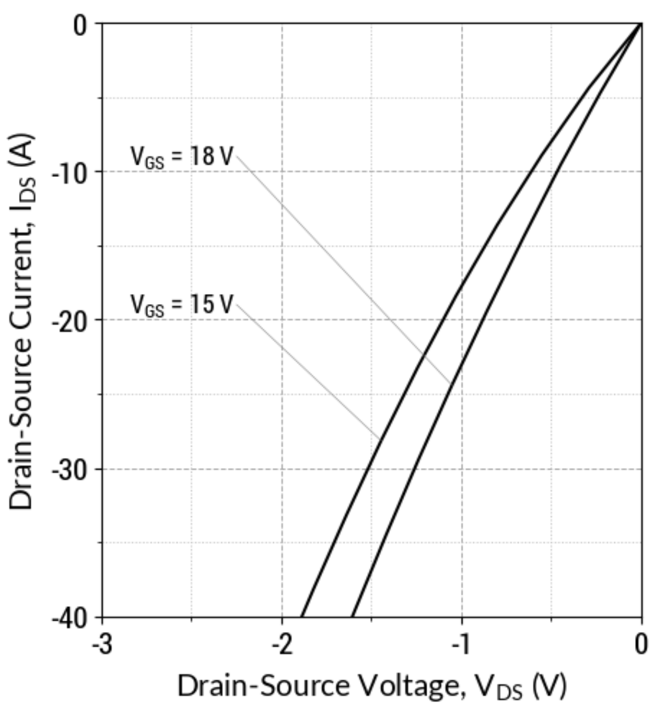
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 22: Typical Third Quadrant Characteristics (T_j = 175°C)



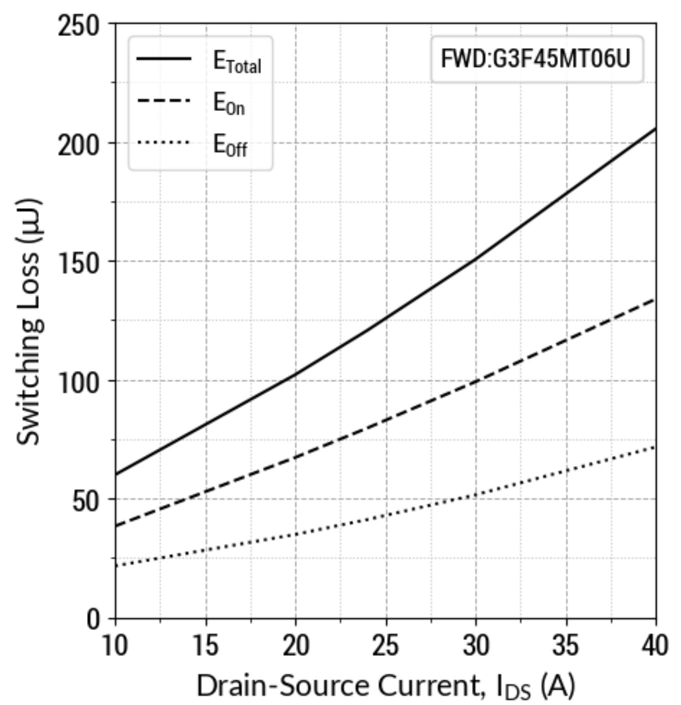
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 23: Typical Third Quadrant Characteristics (T_j = -55°C)



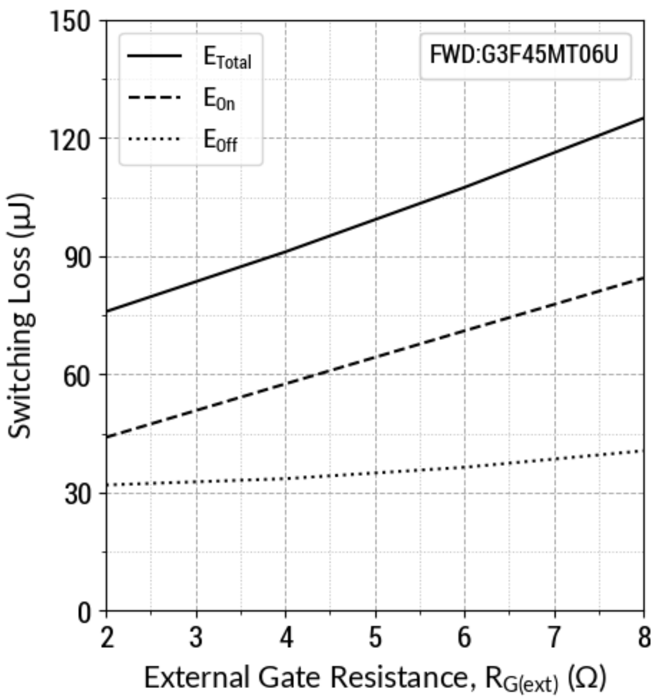
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 24: Inductive Switching Energy v/s Drain Current (V_{DD} = 400V)



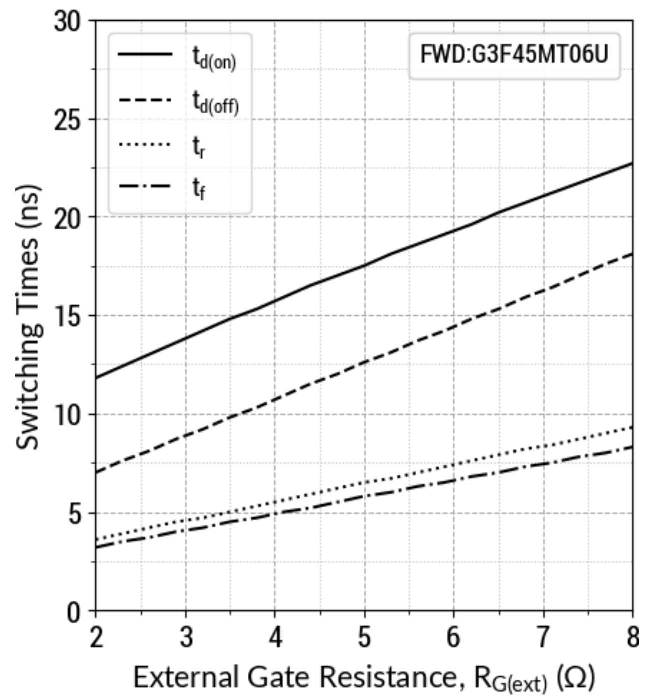
T_j = 25°C; V_{GS} = -5/+18V; $R_{G(ext)}$ = 6.8 Ω; L = 80.0µH

Fig 25: Inductive Switching Energy v/s $R_{G(ext)}$ (V_{DD} = 400V)



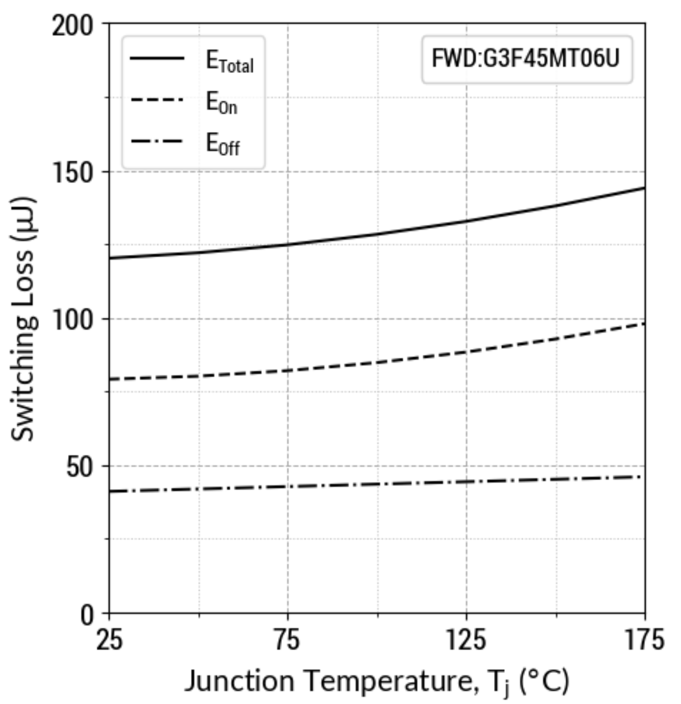
T_j = 25°C; V_{GS} = -5/+18V; I_{DS} = 20 A; L = 80.0µH

Fig 26: Switching Time v/s $R_{G(ext)}$ (V_{DD} = 400V)



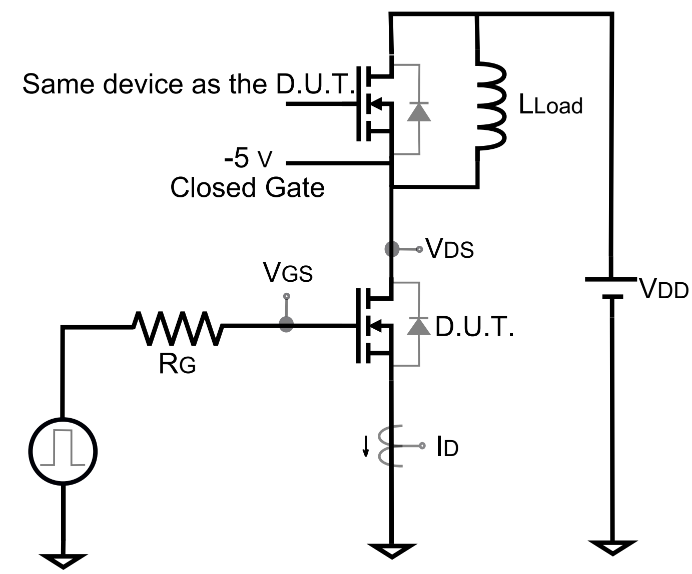
T_j = 25°C; V_{GS} = -5/+18V; I_{DS} = 20 A; L = 80.0µH

Fig 27: Inductive Switching Energy v/s Temperature (V_{DD} = 400V)



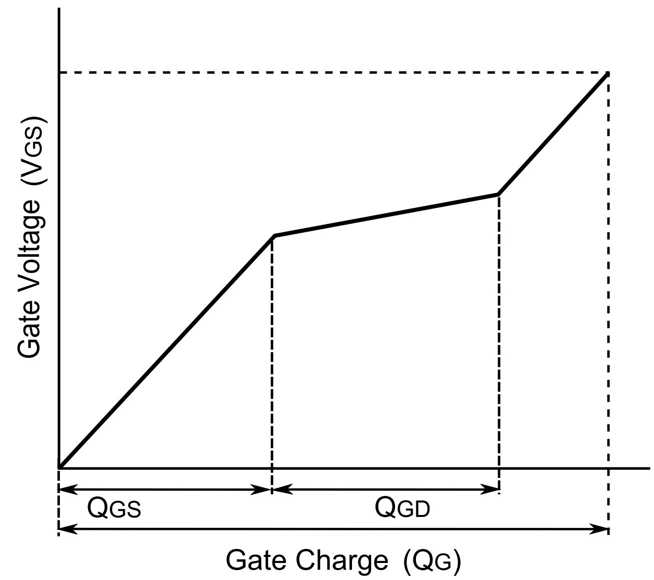
T_j = 25°C; V_{GS} = -5/+18V; $R_{G(ext)}$ = 6.8 Ω; I_{DS} = 20 A; L = 80.0µH

Dynamic Test Circuit

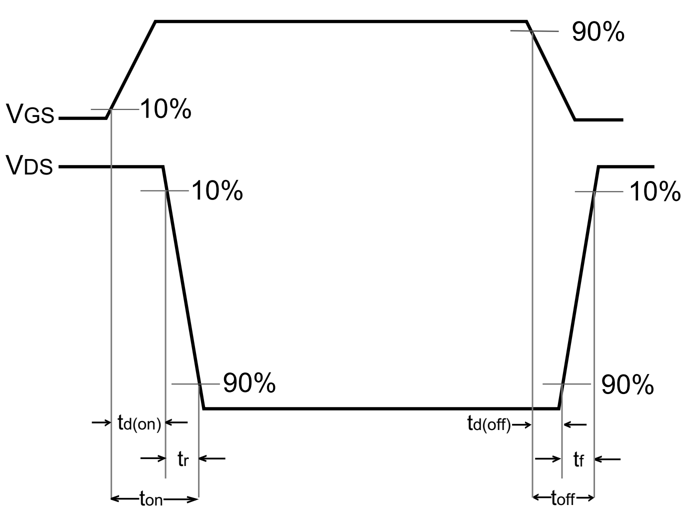


Note: Gate Charge, Switching Time and Energy Circuit

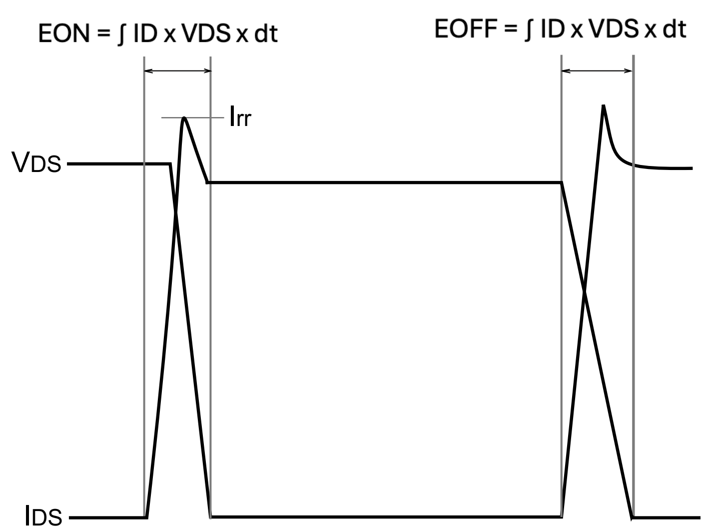
Gate Charge Waveform



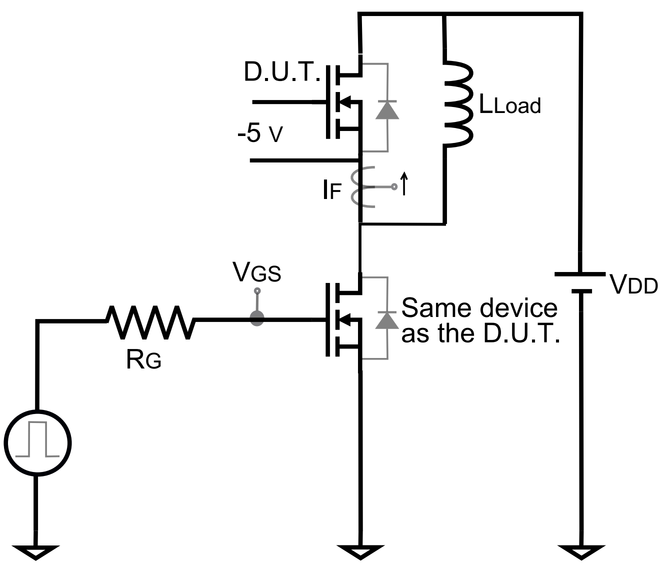
Switching Time Waveform



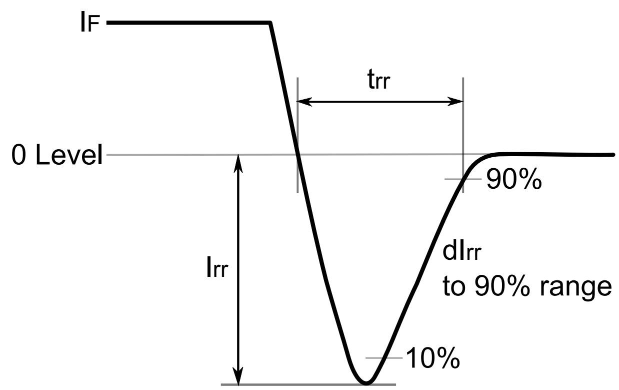
Switching Energy Waveform



Reverse Recovery Circuit

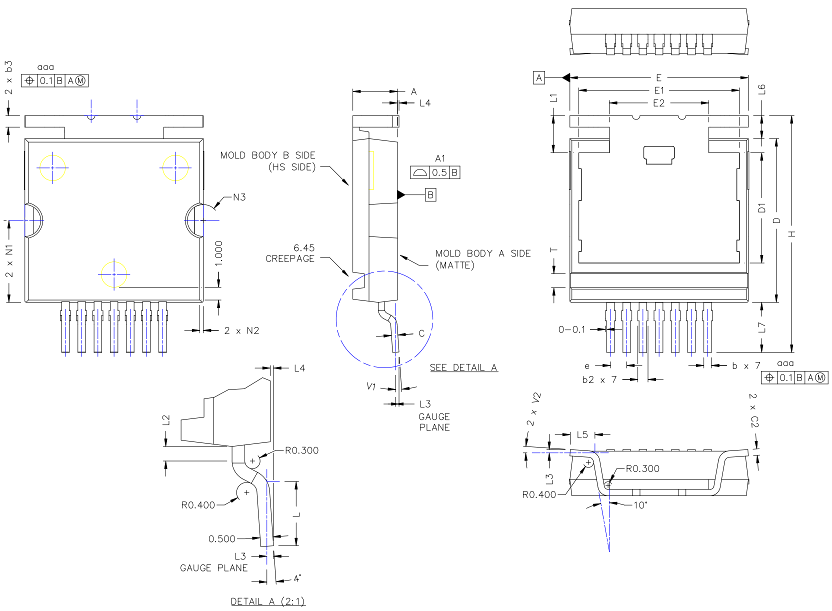


Reverse Recovery Waveform



Package Dimensions

HV-T2PAK Package Outline



SYM	MIN	NOM	MAX
A	–	3.50	–
A1	–	–	0.05
b	–	0.60	–
b2	–	0.80	–
b3	–	0.90	–
c	–	0.50	–
c2	–	0.50	–
D	–	12.85	–
D1	8.55	8.65	8.75
E	13.90	14.00	14.10
E1	12.50	12.60	12.70
E2	–	7.80	–
e	–	1.27	–
H	18.38	18.58	18.78
aaa	–	–	0.10
L	2.42	2.52	2.62
L1	–	2.95	–
L2	0.47	0.57	0.67
L3	–	0.26	–
L4	0.075	0.125	0.175
L5	1.83	1.93	2.03
L6	1.70	1.80	1.90
L7	3.83	3.93	4.03
N1	–	6.43	–
N2	–	0.30	–
N3	–	1.25	–
T	–	1.1	–
V1	0°	4°	8°
V2	0°	4°	8°

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. ALL METAL SURFACES WITH TIN PLATED EXCEPT AREA OF CUT AND HEATSINK.
3. ALL DIMENSIONS ARE PARTIAL AND SUBJECT TO CHANGE UPON DESIGN REVIEW.
4. DIMENSIONS EXCLUDED TIN PLATING THICKNESS.
   GENERAL TIN PLATING THICKNESS: 15±5 UM.
5. GENERAL RADIUS OF EDGE AND CORNER: R IS 0.2 MM.
6. MOLD BODY A SIDE: Ra: 0.8 ~ 1.2 UM.
7. MOLD BODY B SIDE (HS SIDE): Ra: 0.8 ~ 1.2 UM.
8. UNLESS OTHERWISE SPECIFIED.

DECIMAL	ANGULAR
X.X±0.1	X±1°
X.XX±0.05	X.X±0.1°
X.XXX±0.025	

NOTE

1. CONTROLLED DIMENSION IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

Revision History

• Rev 24/Aug: Preliminary Specification

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