650 V 55 mΩ SiC MOSFET

Silicon Carbide MOSFET

Trench-Assisted Planar Technology

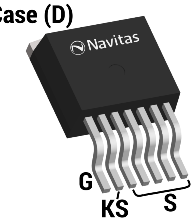
V_{DS}	=	650 V
$R_{DS(ON)}$(Typ.)	=	55 mΩ
$I_{D\,(T_C = 100°C)}$	=	31 A

Features

- Gen3F (3rd Generation) Technology
- Most Stable $R_{DS(ON)}$ over Temperature
- Low C_{OSS}, C_{RSS} and Balanced C_{ISS}/C_{RSS}
- Lower Q_{GD} and Balanced $R_{G(INT)}$
- Electromagnetically Optimized Design
- Robust Body Diode with Low V_F and Low Q_{RR}
- 100% Avalanche (UIL) Tested
- AEC-Q101 Qualified

Package

Case (D)



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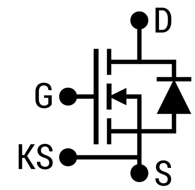


D = Drain
G = Gate
S = Source
KS = Kelvin Source

RoHS
REACH
AEC Q101

Advantages

- Superior Performance and Robustness
- Lowest Conduction Losses at all Temperatures
- Lesser Switching Spikes and Lower Losses
- Faster and More Efficient Switching
- Reduced Ringing
- Ease of Paralleling without Thermal Runaway
- Excellent Power Density and System Efficiency
- Enhanced System Reliability

Applications

- xEV - DC-DC
- Server & Telecom Power Supply
- Solar / PV
- Energy Storage System
- Uninterruptible Power Supply
- Class D Amplifiers

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µA	650	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +22	V	
Gate-Source Voltage (Static)	$V_{GS(op)-ON}$ $V_{GS(op)-OFF}$	Recommended Operation	15 to 18 -5 to -3	V	Note 1
Continuous Drain Current	I_D	T_C = 25°C, V_{GS} = -5 / +18 V T_C = 100°C, V_{GS} = -5 / +18 V T_C = 135°C, V_{GS} = -5 / +18 V	44 31 23	A	Fig. 16
Pulsed Drain Current	$I_{D(pulse)}$	$t_P \le 3$µs, D ≤ 1%, V_{GS} = 18 V	75	A	Note 2
Power Dissipation	P_D	T_c = 25°C	155	W	Fig. 17
Non-Repetitive Avalanche Energy	E_{AS}	L = 36 mH, I_{AV} = 3 A	162	mJ	
Operating Junction and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

Note 1: This product can support 0V turn-off gate drive voltage with optimized PCB layout and gate drive circuit configuration.

Note 2: Pulse Width t_P Limited by $T_{j(max)}$

Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	650			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V		1	50	µA	
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 22 V			100	nA	
		V_{DS} = 0 V, V_{GS} = -10 V			-100		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 7 mA	2.2	2.7	4.3	V	Note 3
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 15 A		7.8		S	Fig. 5
		V_{DS} = 10 V, I_D = 15 A, T_j = 175°C		7.9			
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 18 V, I_D = 15 A		55	75	mΩ	Fig. 5-9
		V_{GS} = 18 V, I_D = 15 A, T_j = 175°C		78			
		V_{GS} = 15 V, I_D = 15 A		68			
		V_{GS} = 15 V, I_D = 15 A, T_j = 175°C		83			
Input Capacitance	C_{iss}	V_{DS} = 400 V, V_{GS} = 0 V f = 500 KHz, V_{AC} = 25mV		1322		pF	Fig. 12
Output Capacitance	C_{oss}			90			
Reverse Transfer Capacitance	C_{rss}			4.5			
C_{oss} Stored Energy	E_{oss}			8		µJ	Fig. 13
C_{oss} Stored Charge	Q_{oss}			57		nC	
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			100		pF	Note 4
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			142			
Gate-Source Charge	Q_{gs}	V_{DS} = 400 V, V_{GS} = -5 / +18 V I_D = 15 A Per JEDEC JEP-192		11		nC	Fig. 11
Gate-Drain Charge	Q_{gd}			13			
Total Gate Charge	Q_g			45			
Internal Gate Resistance	$R_{G(int)}$	V_{GS} = 18 V, f = 1 MHz, V_{AC} = 25 mV		1.8		Ω	
Turn-On Switching Energy (Body Diode)	E_{On}	T_j = 25°C, V_{GS} = -5/+18V, $R_{G(ext)}$ = 10 Ω, L = 80.0 µH, I_D = 15 A, V_{DD} = 400 V		52		µJ	Fig. 24-27
Turn-Off Switching Energy (Body Diode)	E_{Off}			27			
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, V_{GS} = -5/+18V $R_{G(ext)}$ = 10 Ω, L = 80.0 µH, I_D = 15 A Timing relative to V_{DS}, Inductive load		25		ns	Fig. 26
Rise Time	t_r			11			
Turn-Off Delay Time	$t_{d(off)}$			21			
Fall Time	t_f			9			

Note 3: Tested after applying 30ms pulse at Vgs= +25V

Note 4: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400V.
$C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{OSS} while V_{DS} is rising from 0 to 400V.

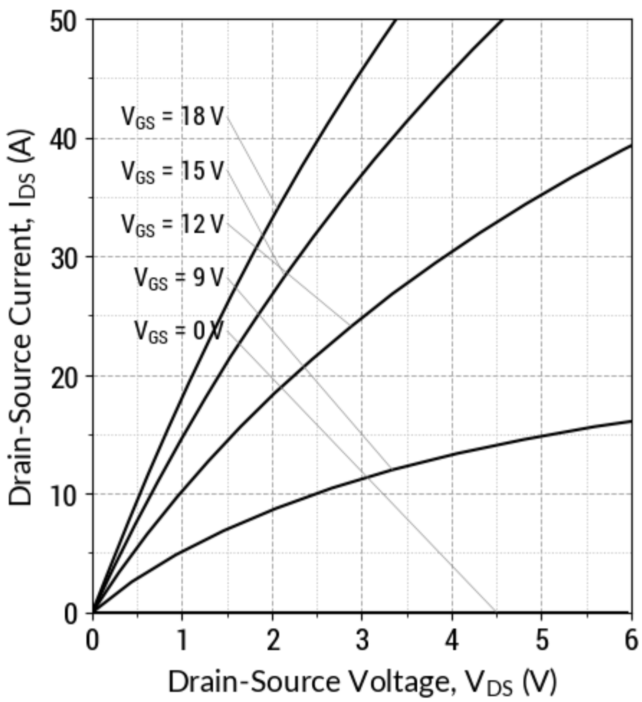
Reverse Diode Characteristics

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 7 A		4.4		V	Fig. 18-19
		V_{GS} = -5 V, I_{SD} = 7 A, T_j = 175°C		3.9			
Continuous Diode Forward Current	I_S	V_{GS} = -5 V, T_c = 25°C			25	A	
		V_{GS} = -5 V, T_c = 100°C			15		
Diode Pulse Current	$I_{S(pulse)}$	V_{GS} = -5 V		60		A	Note 2
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 15 A, V_R = 400 V dif/dt = 6000 A/µs, T_j = 25°C		5.9		ns	
Reverse Recovery Charge	Q_{rr}			61		nC	
Peak Reverse Recovery Current	I_{rrm}			12		A	
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 15 A, V_R = 400 V dif/dt = 6000 A/µs, T_j = 175°C		7		ns	
Reverse Recovery Charge	Q_{rr}			116		nC	
Peak Reverse Recovery Current	I_{rrm}			17.5		A	

Package Characteristics

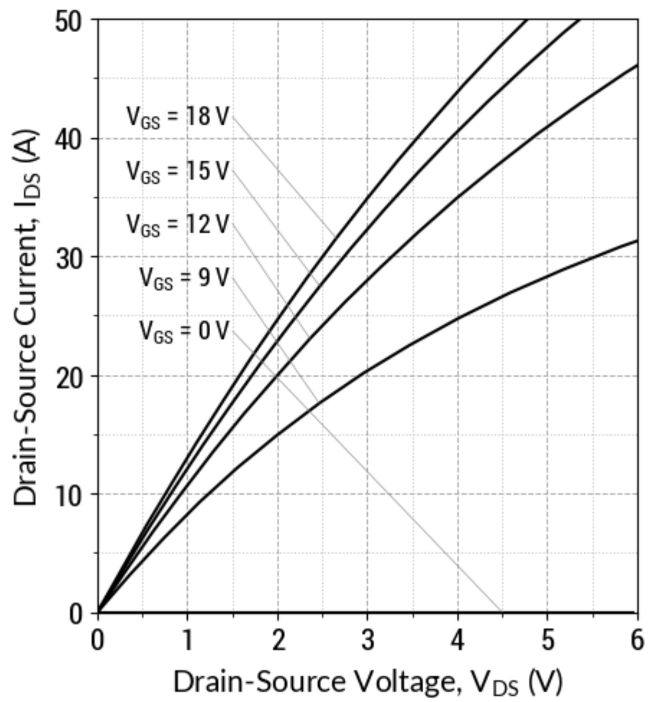
Parameter	Symbol	Conditions	Values	Unit	Note
Max Thermal Resistance, Junction - Case	$R_{thJC-Max}$	Maximum	0.96	°C/W	Fig. 14
Weight	W_T		1.45	g	
Moisture Sensitivity Level	MSL		1		
EMC Material Group			II		

Fig 1: Typical Output Characteristics (T_j = 25°C)



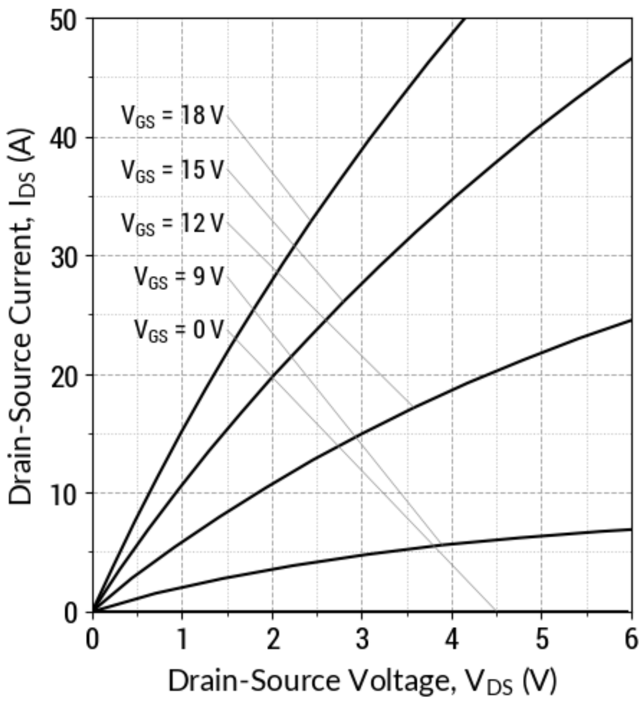
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 2: Typical Output Characteristics (T_j = 175°C)



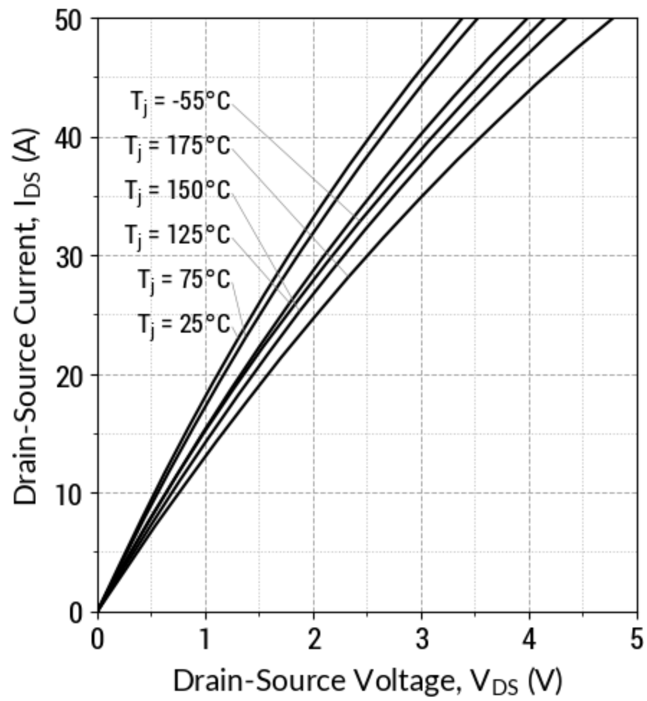
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 3: Typical Output Characteristics (T_j = -55°C)



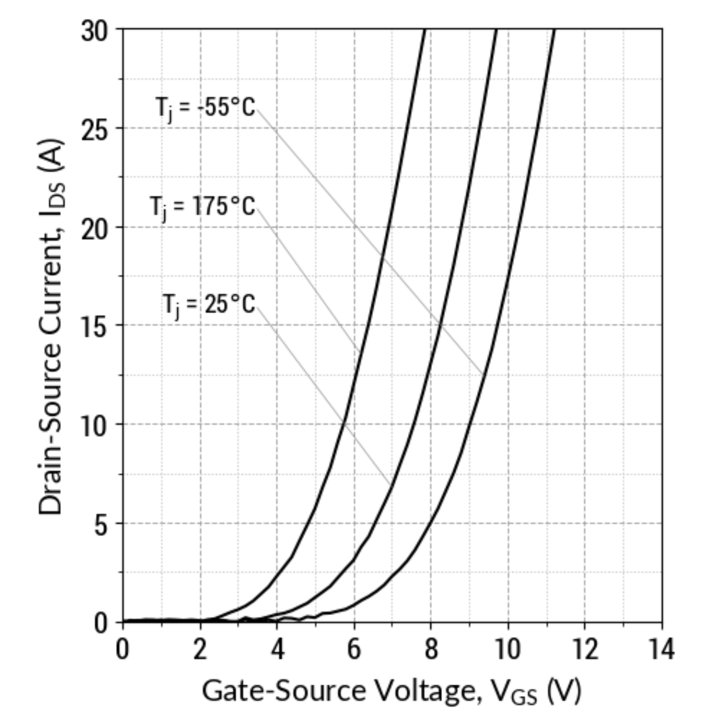
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 4: Typical Output Characteristics (V_{GS} = 18 V)



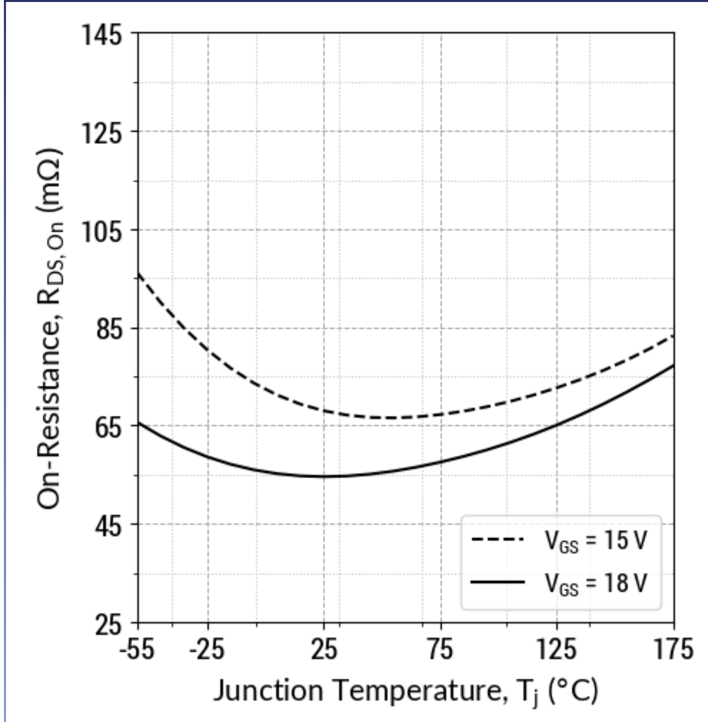
$I_D = f(V_{DS}, T_j)$; t_P = 50 µs

Fig 5: Typical Transfer Characteristics (V_{DS} = 10 V)



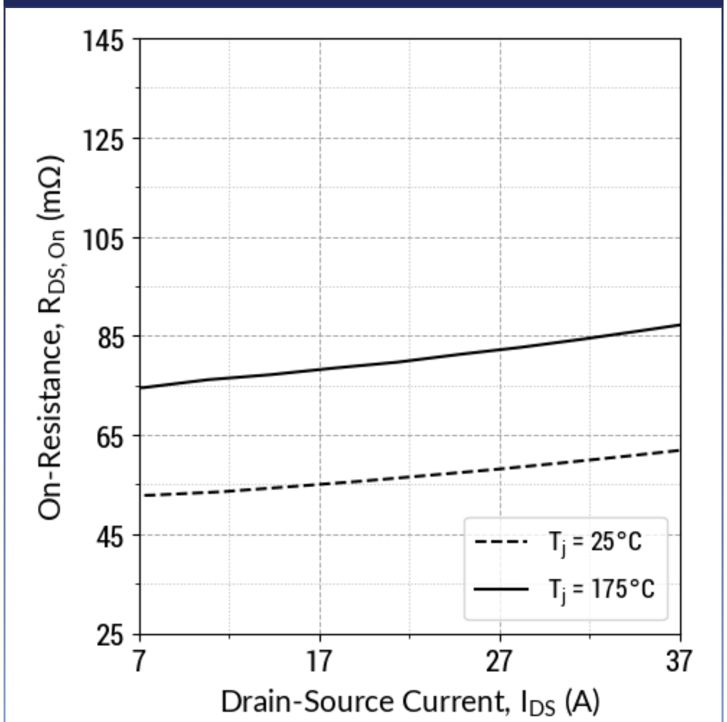
$I_D = f(V_{GS}, T_j)$; t_P = 100 µs

Fig 6: Typical $R_{DS(ON)}$ v/s Temperature



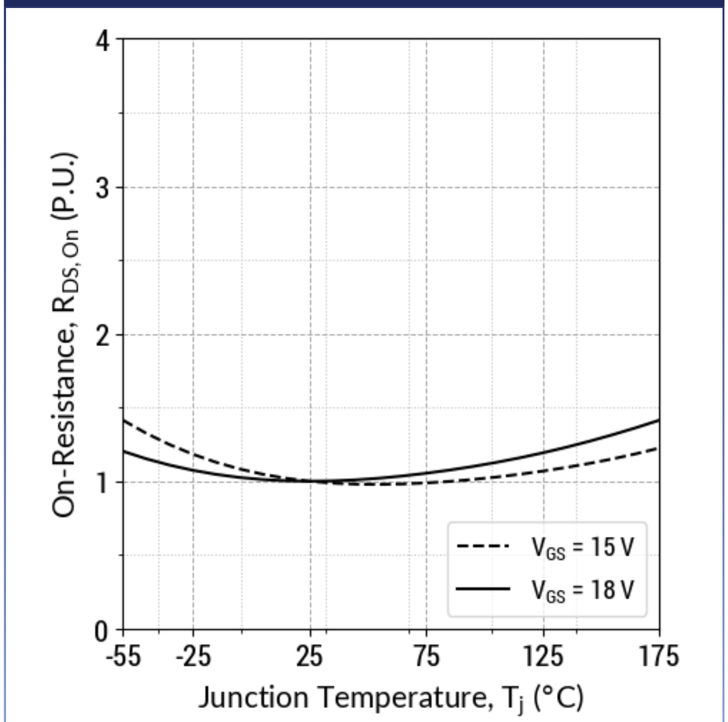
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 50 µs; I_D = 15 A

Fig 7: Typical $R_{DS(ON)}$ v/s Drain Current



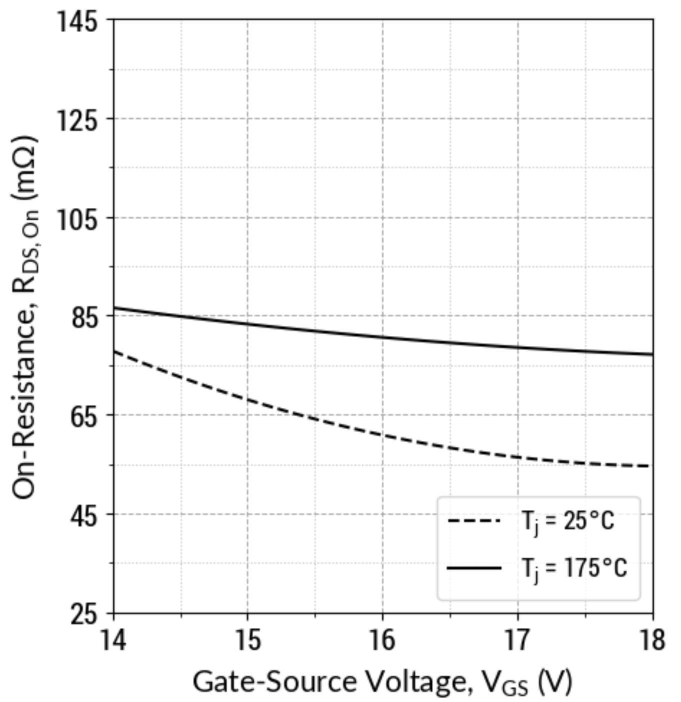
$R_{DS(ON)} = f(T_j, I_D)$; t_P = 50 µs; V_{GS} = 18 V

Fig 8: Typical Normalized $R_{DS(ON)}$ v/s Temperature



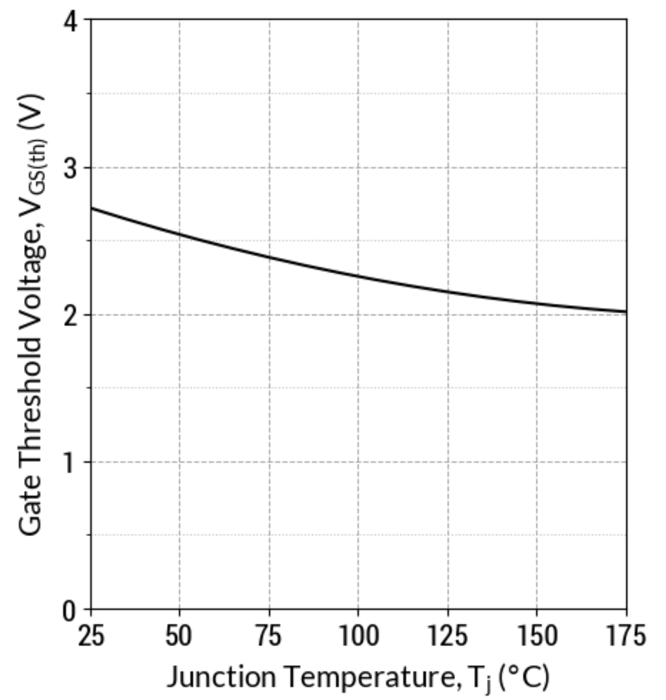
$R_{DS(ON)} = f(T_j)$; t_P = 50 µs; I_D = 15 A

Fig 9: Typical $R_{DS(ON)}$ v/s Gate Voltage



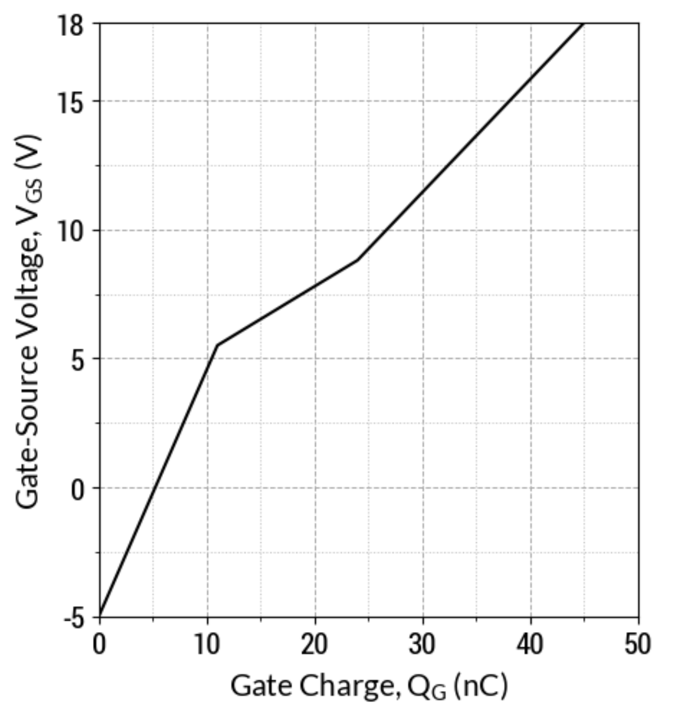
$R_{DS(ON)} = f(T_j, V_{GS})$; $t_P = 50\ \mu s$; $I_D = 15\ A$

Fig 10: Typical Threshold Voltage Characteristics



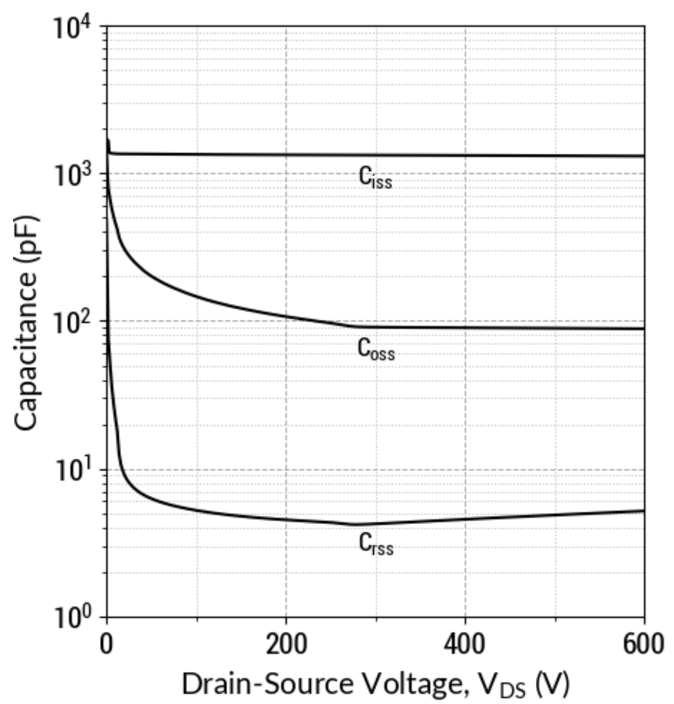
$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; $I_D = 7\ mA$

Fig 11: Typical Gate Charge Characteristics



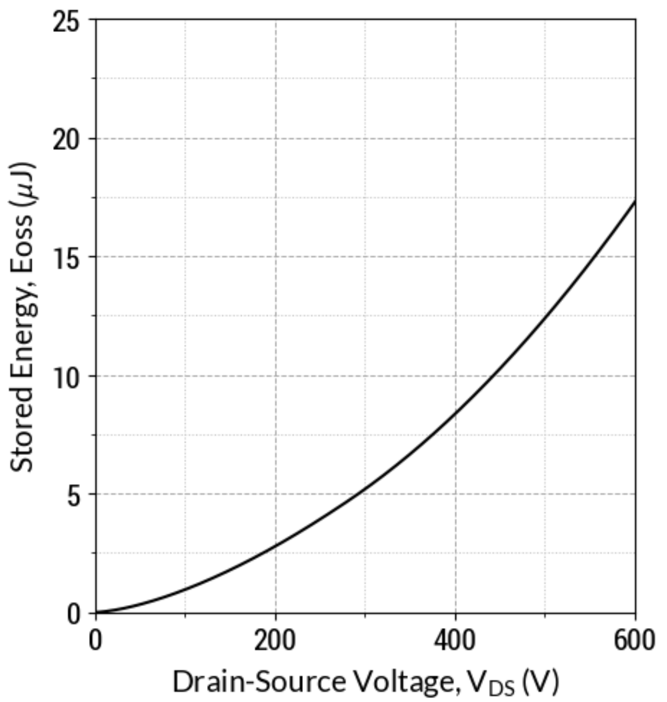
$I_D = 15\ A$; $V_{DS} = 400\ V$; $T_c = 25°C$

Fig 12: Typical Capacitance v/s Drain-Source Voltage



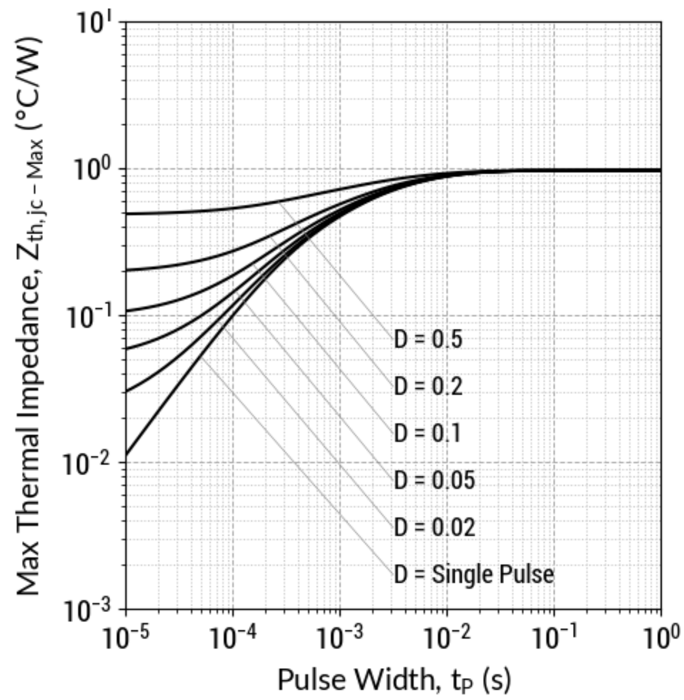
f = 500 KHz; $V_{AC} = 25mV$

Fig 13: Output Capacitor Stored Energy



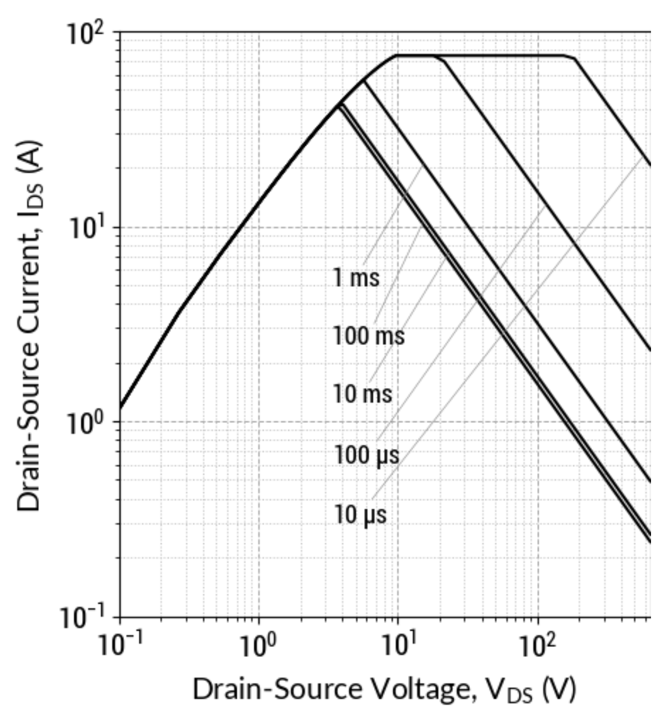
$E_{oss} = f(V_{DS})$

Fig 14: Max. Transient Thermal Impedance



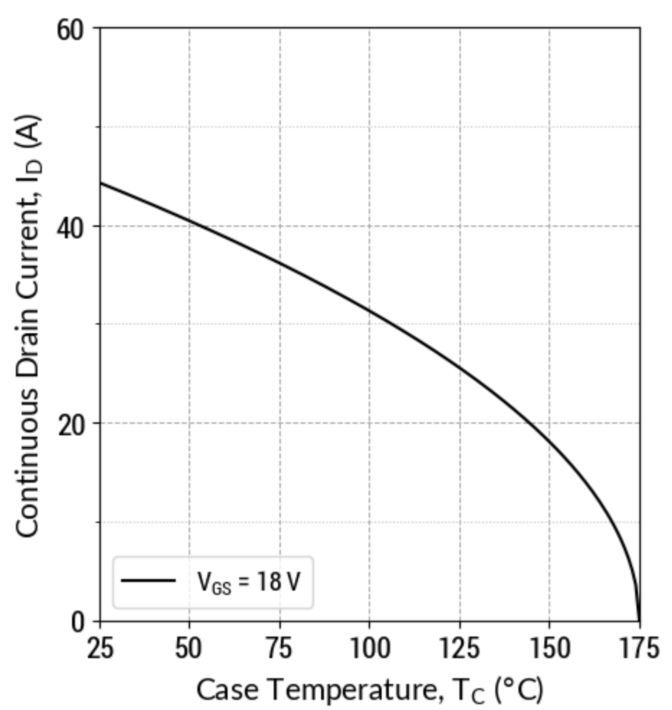
$Z_{th,jc} = f(t_P, D)$; $D = t_P/T$

Fig 15: Safe Operating Area (T_c = 25°C)



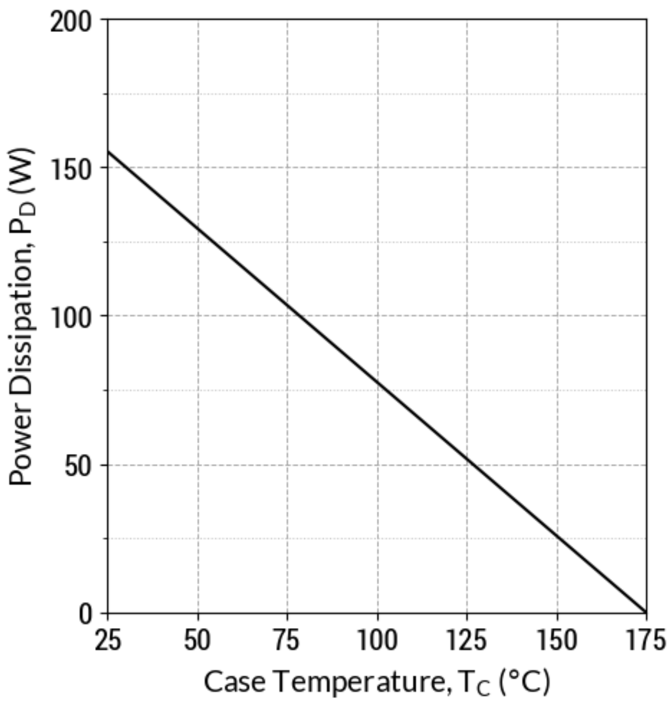
$I_D = f(V_{DS}, t_P)$; $T_j \leq 175°C$; $D = 0$

Fig 16: Current De-rating Curve



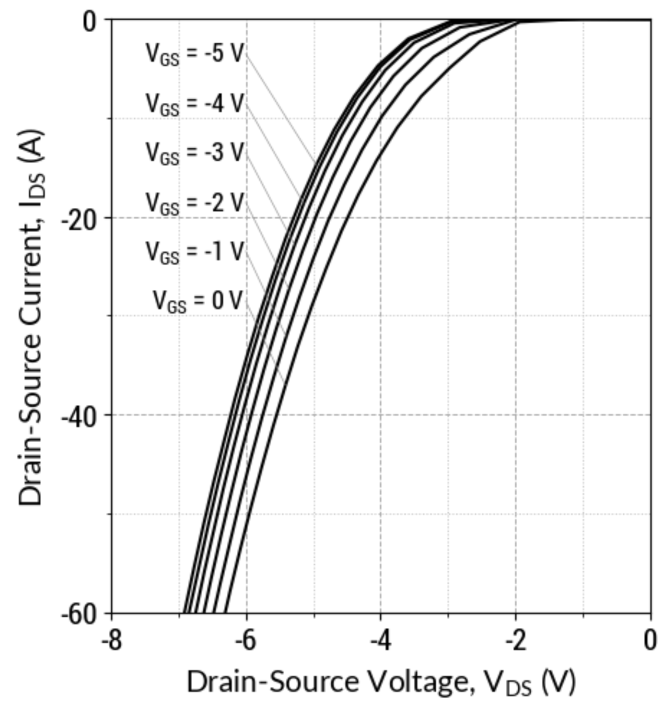
$I_D = f(T_C)$; $T_j \leq 175°C$

Fig 17: Power De-rating Curve



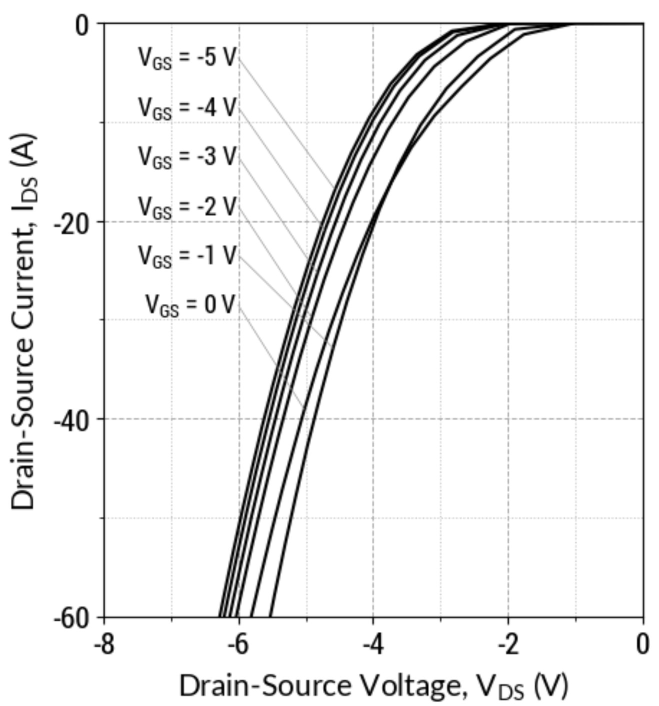
$P_D = f(T_C)$; $T_j \leq 175°C$

Fig 18: Typical Body Diode Characteristics (T_j = 25°C)



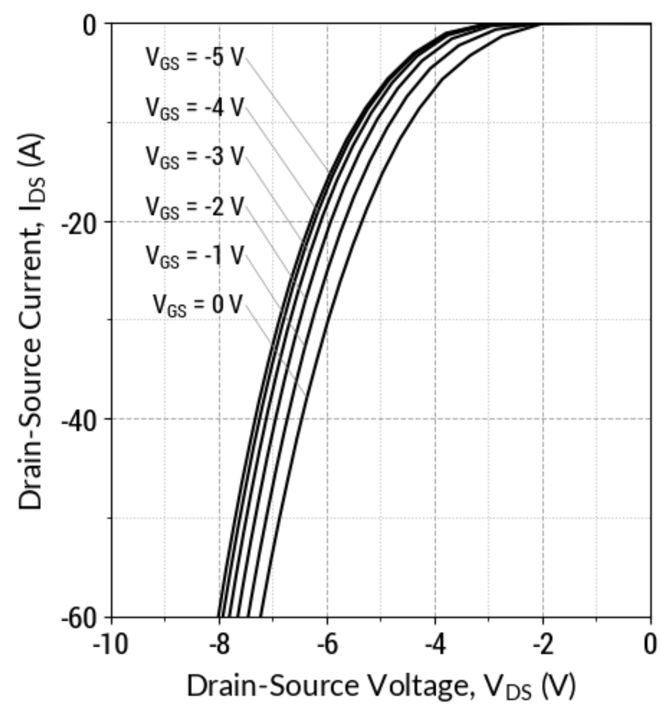
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 19: Typical Body Diode Characteristics (T_j = 175°C)



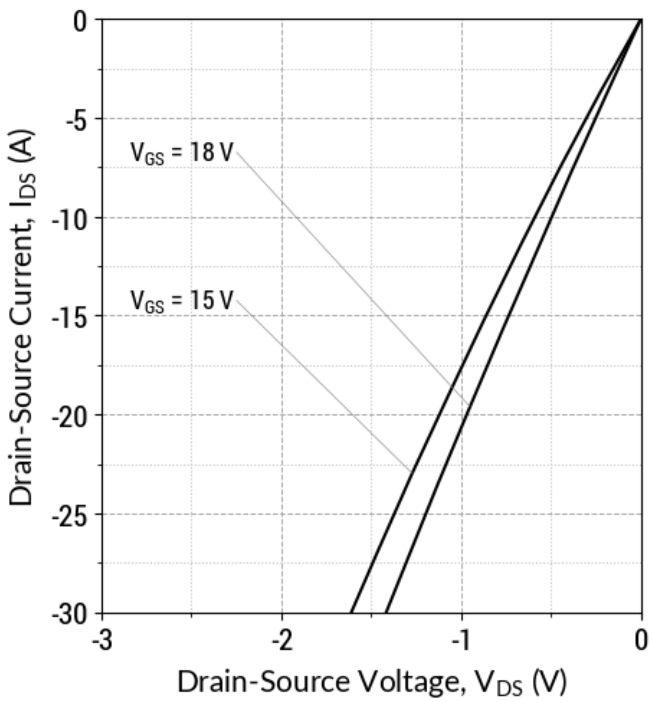
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 20: Typical Body Diode Characteristics (T_j = -55°C)



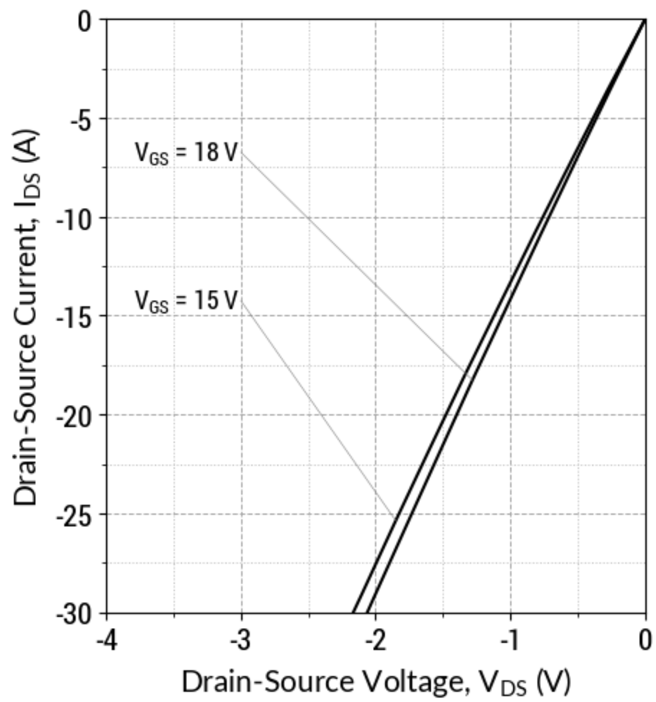
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 21: Typical Third Quadrant Characteristics (T_j = 25°C)



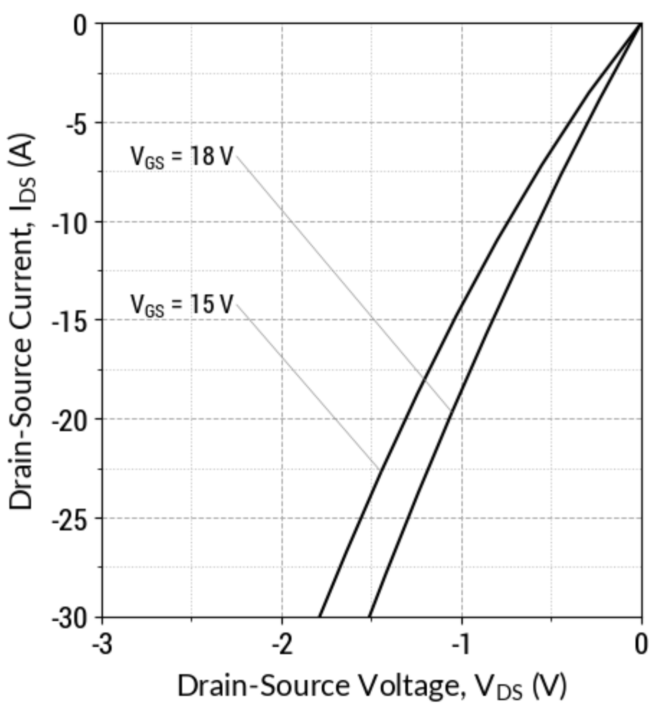
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 22: Typical Third Quadrant Characteristics (T_j = 175°C)



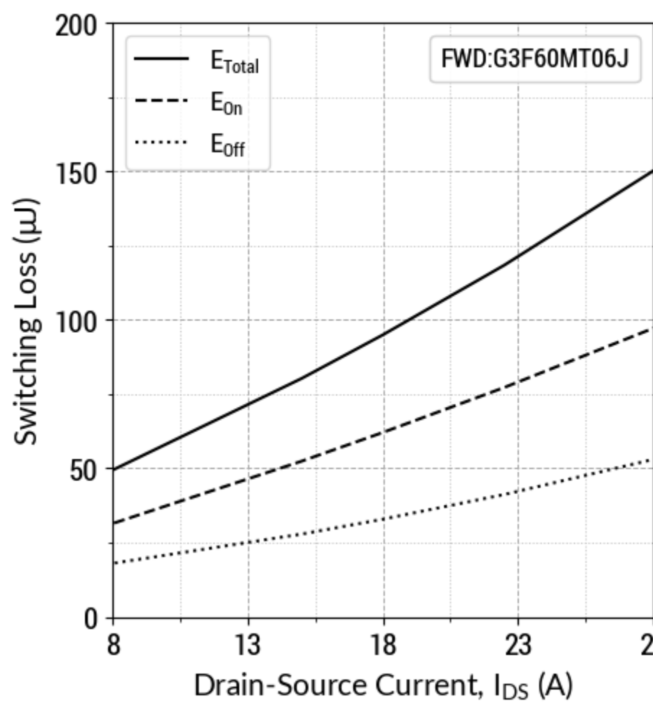
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 23: Typical Third Quadrant Characteristics (T_j = -55°C)



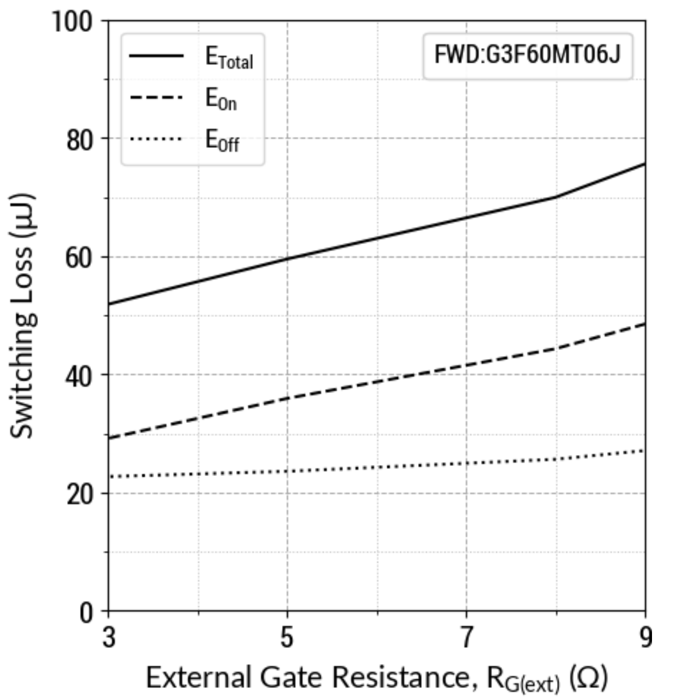
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 24: Inductive Switching Energy v/s Drain Current (V_{DD} = 400V)



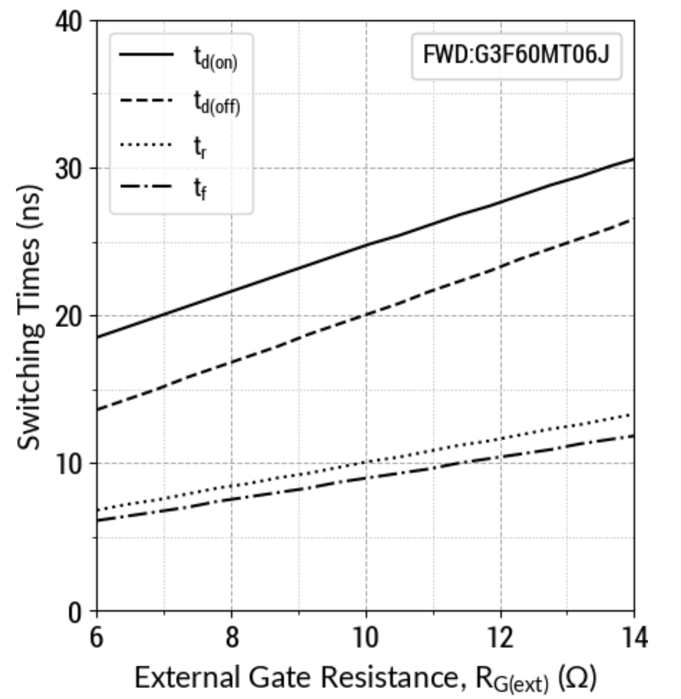
T_j = 25°C; V_{GS} = -5/+18V; $R_{G(ext)}$ = 10 Ω; L = 80.0µH

Fig 25: Inductive Switching Energy v/s $R_{G(ext)}$ (V_{DD} = 400V)



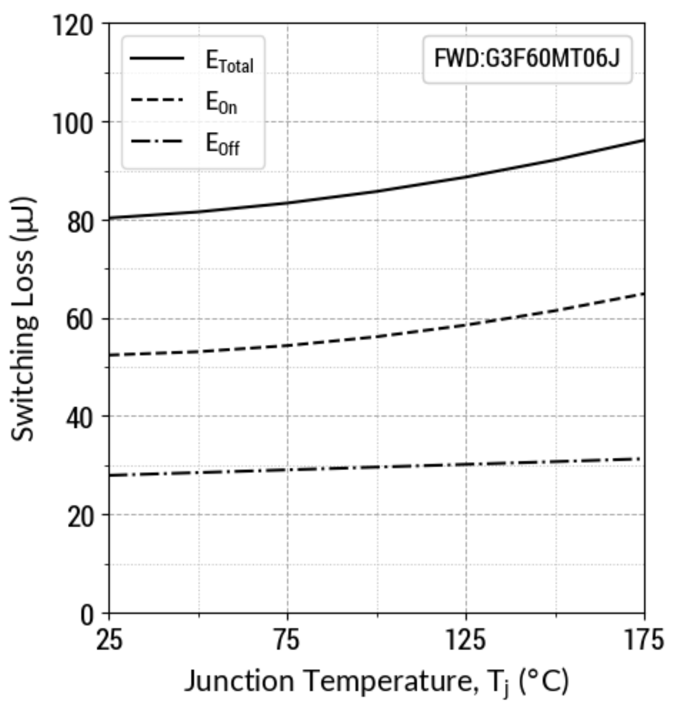
T_j = 25°C; V_{GS} = -5/+18V; I_{DS} = 15 A; L = 80.0µH

Fig 26: Switching Time v/s $R_{G(ext)}$ (V_{DD} = 400V)



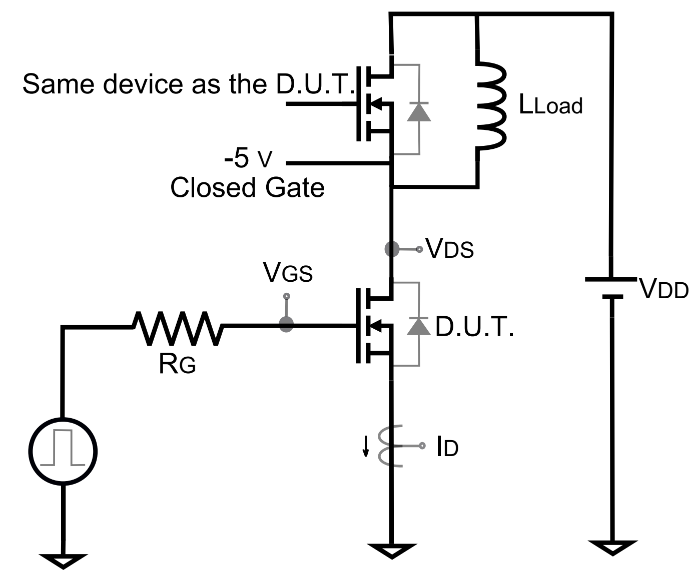
T_j = 25°C; V_{GS} = -5/+18V; I_{DS} = 15 A; L = 80.0µH

Fig 27: Inductive Switching Energy v/s Temperature (V_{DD} = 400V)



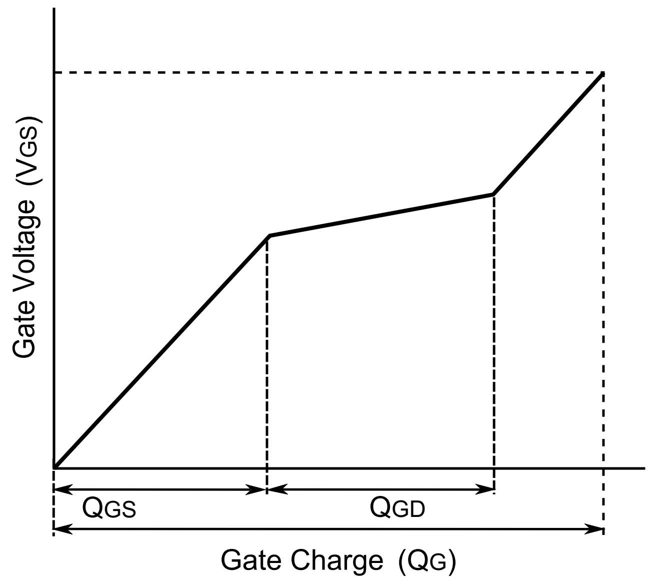
T_j = 25°C; V_{GS} = -5/+18V; $R_{G(ext)}$ = 10 Ω; I_{DS} = 15 A; L = 80.0µH

Dynamic Test Circuit

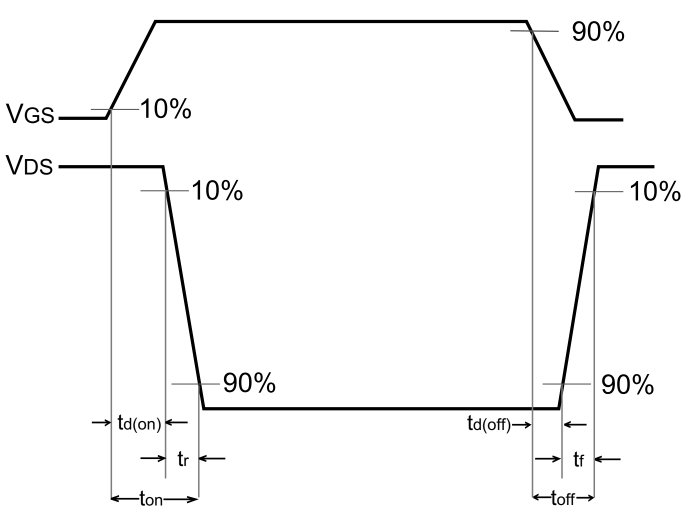


Note: Gate Charge, Switching Time and Energy Circuit

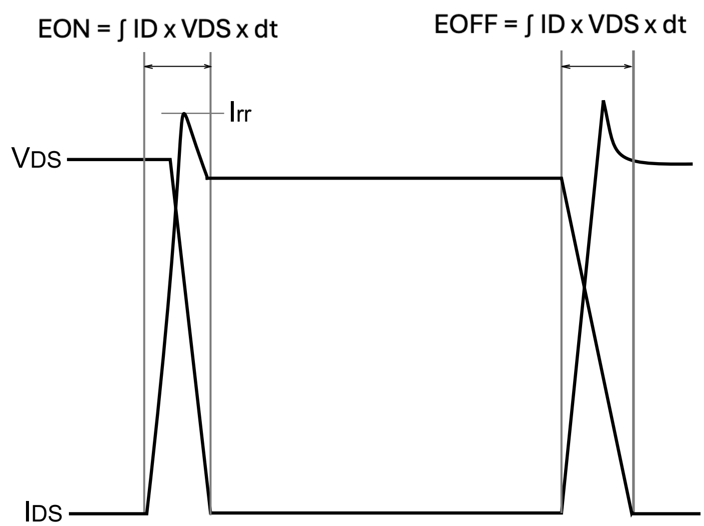
Gate Charge Waveform



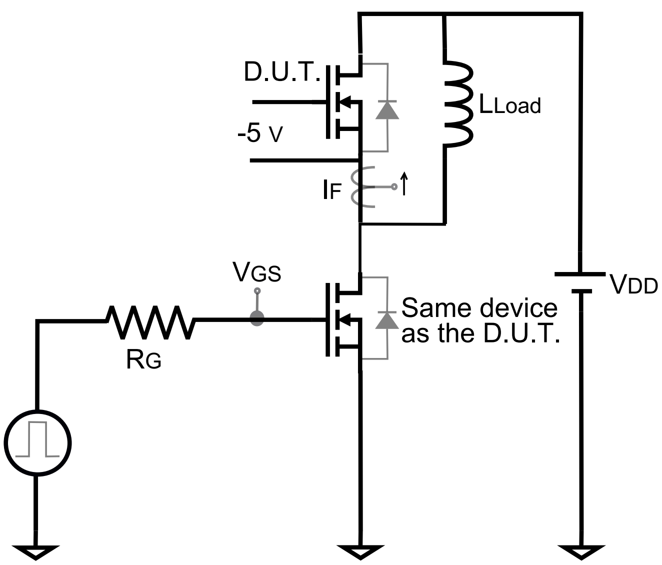
Switching Time Waveform



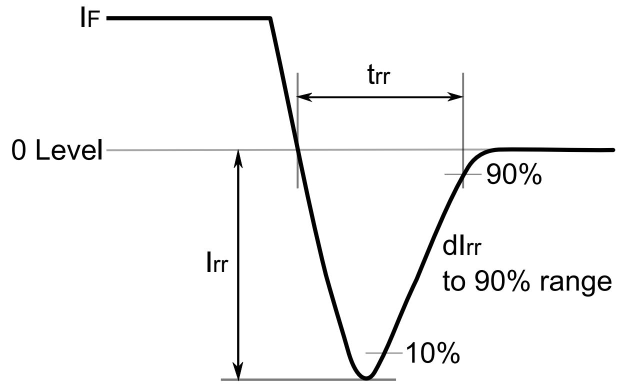
Switching Energy Waveform



Reverse Recovery Circuit

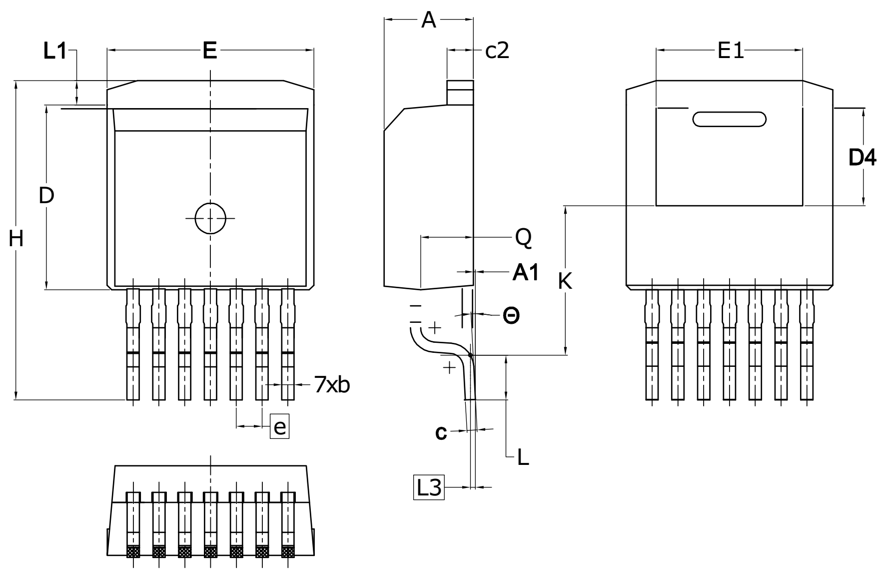


Reverse Recovery Waveform



Package Dimensions

TO-263-7 Package Outline



Note:
1. All Dimensions Are In mm.
2. Dimension D & E Do Not Include Mold Flash.
These Dimensions Are Measured At The Outermost
Extreme Of The Plastic Body.
3. Thermal Pad Contour Optional Within Dimensions E, L1, D4 & E1.
4. Dimension D4 & E1 Establish A Minmum Mounting Surface for
The Thermal Pad.
5. ■ is Exposed Cu.
6. There Is Exposed Cu and Molding Flash Bleeding At The Pin Which Is Close To Package.

SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.25
b	0.50	0.70
c	0.45	0.60
c2	1.20	1.40
D	8.93	9.23
D4	4.65	4.95
E	10.08	10.28
E1	6.82	7.62
e	1.27 BSC	
H	15.00	16.00
K	7.30	
L	1.90	2.50
L1	1.00	1.40
L3	0.25 BSC	
Q	2.45	2.75
Θ	0°	7°

NOTE

1. CONTROLLED DIMENSION IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.
3. THE SOURCE AND KELVIN-SOURCE PINS ARE NOT INTERCHANGABLE. THEIR EXCHANGE MIGHT LEAD TO MALFUNCTION.

Revision History

• Rev 24/Aug: Initial Release (Rev 1.0)

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