GaNFast™ Power FET

1. Features

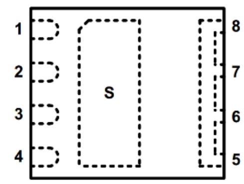
GaNFast™ Power IC

- eMode GaN power FET
- Low 120 mΩ resistance
- 10 MHz switching frequency capability
- Ultra-low gate charge
- Zero reverse recovery charge
- Low output charge
- 800 V Transient Voltage Rating
- 700 V Continuous Voltage Rating
- Source Kelvin (SK) pin for gate noise immunity
- Small, low-profile SMT PQFN
- 5x6 mm PCB footprint
- Minimized package inductance
- Low thermal resistance
- Bottom-side cooled

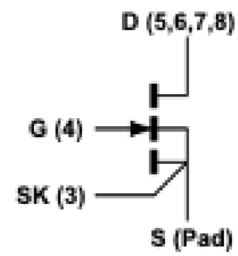
Environmental

- RoHS, Pb-free, REACH-compliant

PQFN 5x6 mm



Package Outline (Top View)



Simplified Schematic

2. Topologies / Applications

- AC-DC, DC-DC, DC-AC
- QR flyback, ACF, buck, boost, half bridge, full bridge, LLC resonant, Class D, PFC
- Wireless power
- LED lighting
- Solar Micro-inverters
- TV SMPS
- Server, Telecom

3. Description

This GaNFast™ power FET is a high performance eMode GaN FET that achieves excellent high-frequency and high efficiency operation. Features include a simple gate input and a Source Kelvin pin for noise immunity.

This GaN power FET combines the highest dV/dt immunity and industry-standard low-profile, low-inductance, bottom-side cooled SMT QFN packaging to enable designers to achieve simple, quick and reliable solutions.

Navitas' GaN technology extends the capabilities of traditional topologies such as flyback, half-bridge, buck/boost, LLC and other resonant converters to reach MHz+ frequencies with very high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

4. Table of Contents

5. Specifications

5.1. Absolute Maximum Ratings(1)

(with respect to Source (pad) unless noted)

SYMBOL	PARAMETER	MAX	UNITS
$V_{DS(TRAN)}$	Transient Drain-to-Source Voltage(2)	800	V
$V_{DS(CONT)}$	Continuous Drain-to-Source Voltage	-7 to +700	V
V_{GS}	Continuous Gate-to-Source Voltage	-10 to +7	V
V_{TGS}	Transient Gate-to-Source Voltage(3)	-20 to +10	V
I_D	Continuous Drain Current (@ T_C = 25ºC)	13	A
I_D	Continuous Drain Current (@ T_C = 100ºC)	8	A
I_D PULSE	Pulsed Drain Current (10 µs @ T_J = 25°C)	26	A
dV/dt	Slew Rate on Drain-to-Source	200	V/ns
T_J	Operating Junction Temperature	-55 to 150	ºC
T_{STOR}	Storage Temperature	-55 to 150	ºC

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2) VDS (TRAN) allows for surge ratings during non-repetitive events that are < 100 µs (for example start-up, line interruption) and repetitive events that are < 100 ns (for example repetitive leakage inductance spikes).

(3) < 1 µs

5.2. Thermal Resistance

SYMBOL	PARAMETER	TYP	UNITS
$R_{\theta JC}$	Junction-to-Case	1.7	ºC/W
$R_{\theta JA}$ (4)	Junction-to-Ambient	41.5	ºC/W

(4) R_θ measured on DUT mounted on 40mm x 40mm FR4 PCB (1 layer 2 oz Cu)

5.3. Electrical Characteristics

Typical conditions: V_{DS} = 400 V, F_{SW} = 1 MHz, T_{AMB} = 25 ºC, I_D = 4.5 A (or specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
GaN FET Characteristics						
I_{DSS}	Drain-Source Leakage Current		0.3	25	µA	V_{DS} = 700 V, V_{GS} = 0 V
I_{DSS}	Drain-Source Leakage Current		8		µA	V_{DS} = 700 V, V_{GS} = 0 V, T_C = 150 ºC
I_{GSS}	Gate-Source Leakage Current		90		µA	V_{GS} = 7V, V_{DS} = 0V
$R_{DS(ON)}$	Drain-Source Resistance		120	170	mΩ	V_{GS} = 7 V, I_D = 4.5 A
$V_{GS(th)}$	Gate Threshold Voltage	1.0	1.7	2.8	V	I_D = 8 mA, V_{DS} = 0.1 V
V_{SD}	Source-Drain Reverse Voltage		3.3	5	V	V_{GS} = 0 V, I_{SD} =4.5 A
T_{ON}	Turn-On Delay Time		4		ns	V_{DS} = 400 V, V_{GS} = 5.2 V, I_D = 4.5 A, R_G = 10 Ω
T_{OFF}	Turn-Off Delay Time		6		ns	V_{DS} = 400 V, V_{GS} = 5.2 V, I_D = 4.5 A, R_G = 10 Ω
T_R	Turn-Off Rise Time		10		ns	V_{DS} = 400 V, V_{GS} = 5.2 V, I_D = 4.5 A, R_G = 10 Ω
T_F	Turn-On Fall Time		5		ns	V_{DS} = 400 V, V_{GS} = 5.2 V, I_D = 4.5 A, R_G = 10 Ω
Q_{RR}	Reverse Recovery Charge		0		nC	
R_G	Internal Gate Resistance		1		Ω	
C_{ISS}	Input Capacitance		89		pF	V_{DS} = 400 V, V_{GS} = 0 V
C_{OSS}	Output Capacitance		28		pF	V_{DS} = 400 V, V_{GS} = 0 V
C_{RSS}	Reverse Transfer Capacitance		0.36		pF	V_{DS} = 400 V, V_{GS} = 0 V
Q_G	Total Gate Charge		2.6		nC	V_{GS} = 0-7 V, I_D = 4.5 A, V_{DS} = 400 V
Q_{GD}	Gate-to-Drain Charge		0.7		nC	V_{GS} = 0-7 V, I_D = 4.5 A, V_{DS} = 400 V
Q_{GS}	Gate-to-Source Charge		0.4		nC	V_{GS} = 0-7 V, I_D =4.5 A, V_{DS} = 400 V
Q_{OSS}	Output Charge		21		nC	V_{GS} = 0 V, V_{DS} = 400 V
$C_{O(er)}$ (5)	Effective Output Capacitance, Energy Related		36		pF	V_{DS} = 400 V, V_{GS} = 0 V
$C_{O(tr)}$ (6)	Effective Output Capacitance, Time Related		51		pF	V_{DS} = 400 V, V_{GS} = 0 V

(5) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(6) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

5.4. Characteristic Graphs

(GaN FET, T_C = 25 ºC unless otherwise specified)

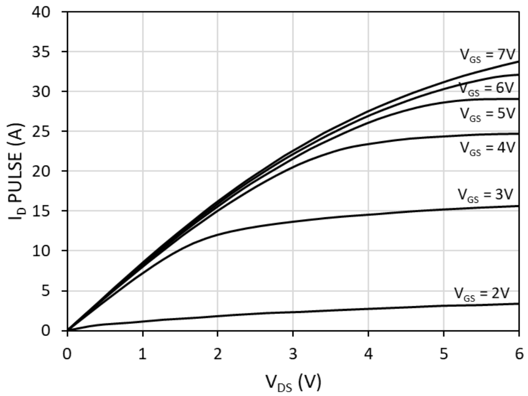


Fig. 1. Pulsed drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 25 °C

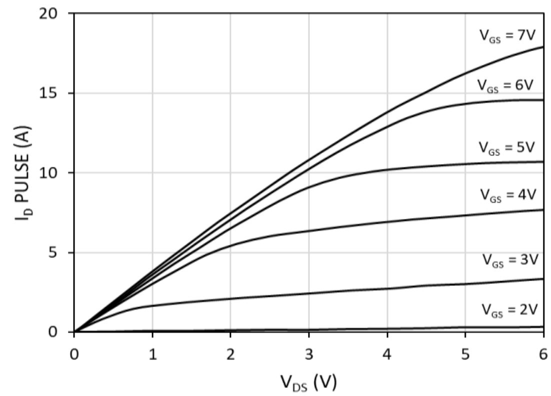


Fig. 2. Pulsed drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 150 °C

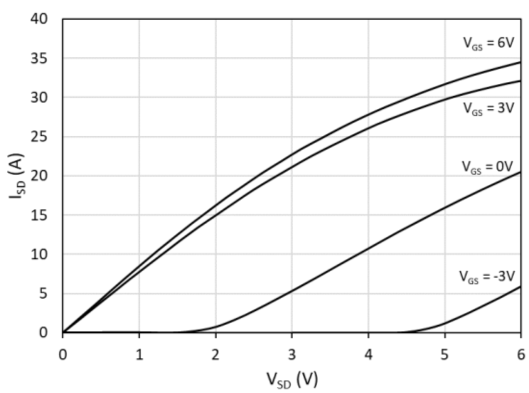


Fig. 3. Source-to-drain reverse conduction voltage at T = 25 °C

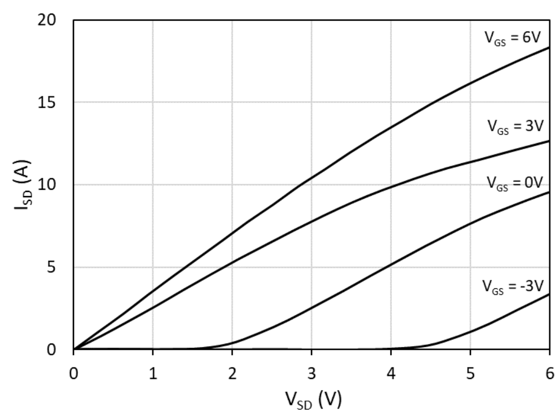


Fig. 4. Source-to-drain reverse conduction voltage at T = 150 °C

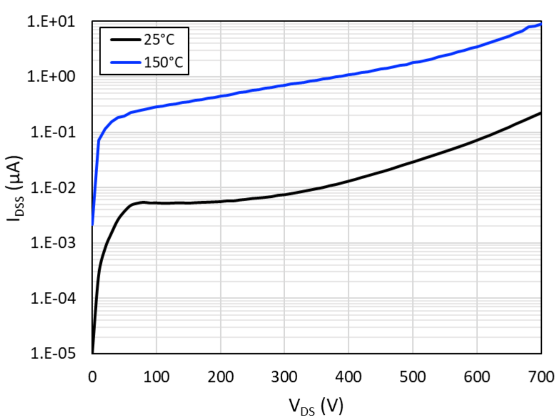


Fig. 5. Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS})

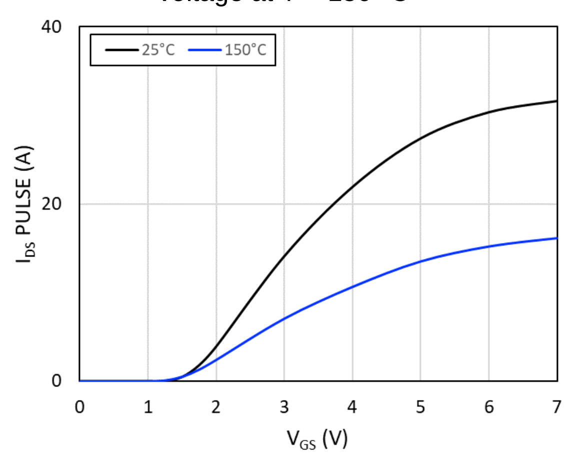


Fig. 6. Pulsed drain current (I_D PULSE) vs. gate-to-source voltage (V_{GS})

Characteristic Graphs (Cont.)

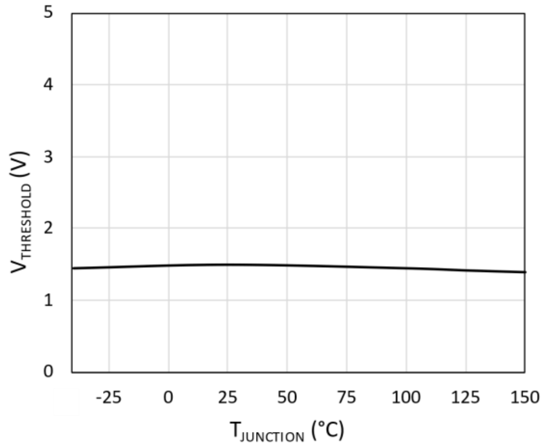


Fig. 7. Gate threshold voltage ($V_{GS(th)}$) vs. junction temperature (T_J)

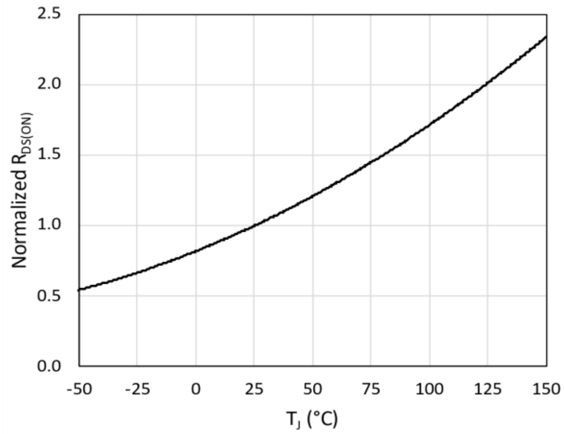


Fig. 8. Normalized on-resistance ($R_{DS(ON)}$) vs. junction temperature (T_J)

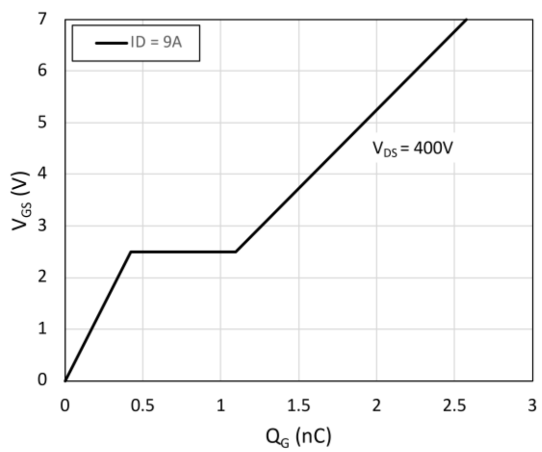


Fig. 9. Gate-to-source voltage (V_{GS}) vs. total gate Charge (Q_G)

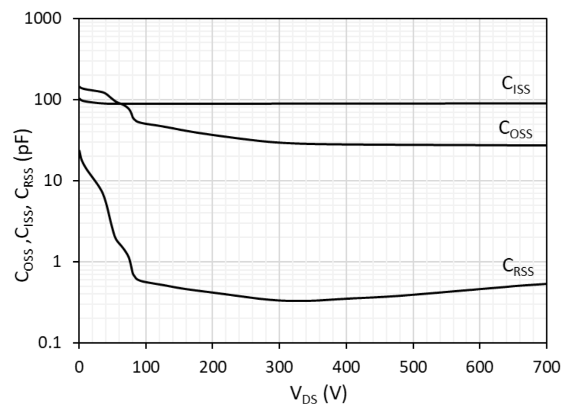


Fig. 10. Input Capacitance (C_{ISS}), Output capacitance (C_{OSS}), Reverse Transfer capacitance (C_{RSS}), vs. drain-to-source voltage (V_{DS})

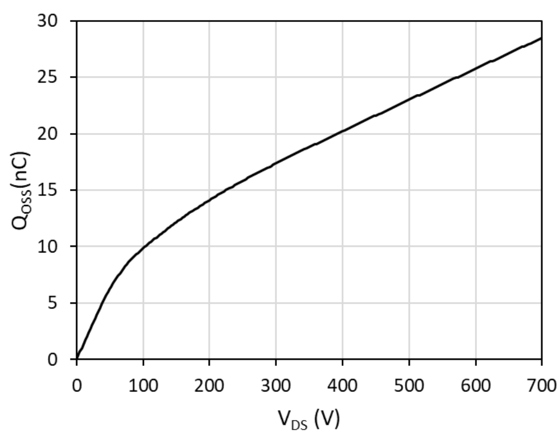


Fig. 11. Charge stored in output capacitance (Q_{OSS}) vs. drain-to-source voltage (V_{DS})

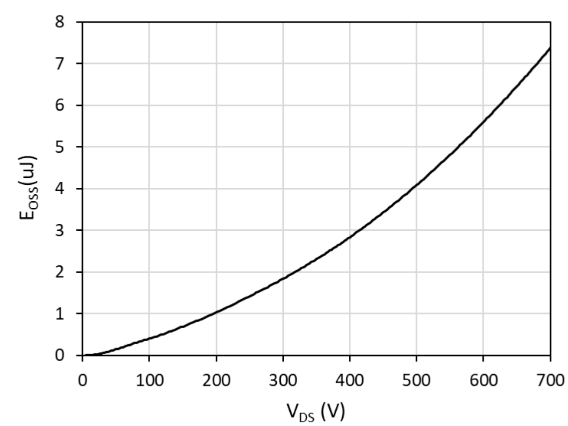


Fig. 12. Energy stored in output capacitance (E_{OSS}) vs. drain-to-source voltage (V_{DS})

Characteristic Graphs (Cont.)

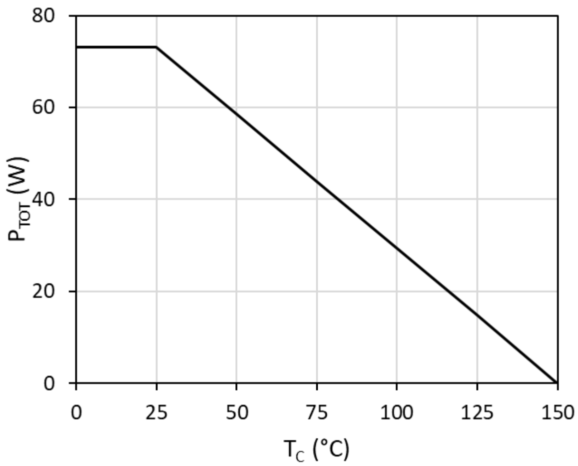


Fig. 13 Power Dissipation (PTOT) vs. case temperature

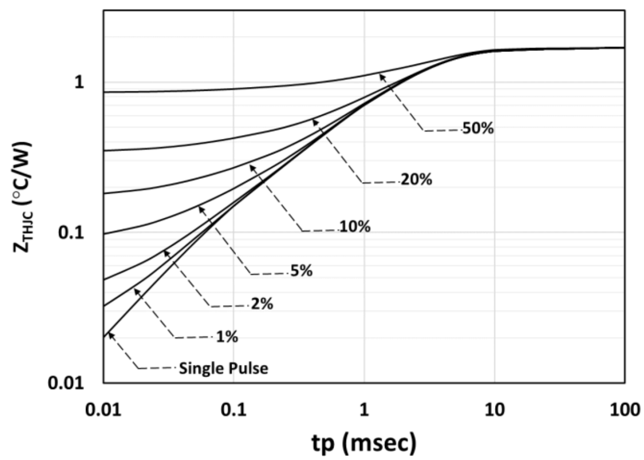


Fig. 14 Max. Thermal Transient Impedance (Z_{thJC}) vs. Pulse Width (t_P)

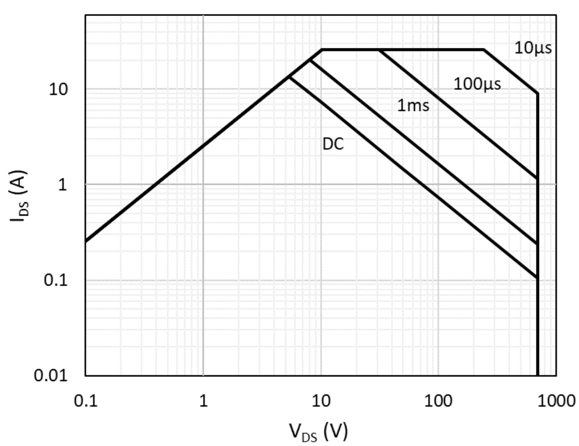
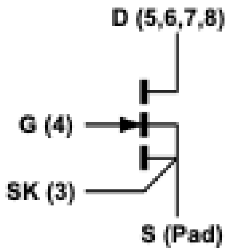
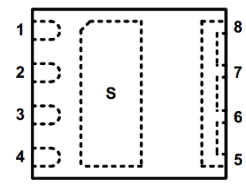


Fig. 15 Safe Operation Area (SOA) @ T_{CASE} = 25°C

Pin Configurations and Functions





Package Top View

Pin Number	Pin Name	Description
1, 2	NC	No connection, leave floating or connect to Source PAD
3	SK	Kelvin sense of FET source. Use for driver connection
4	G	Gate of power FET
5, 6, 7, 8	D	Drain of power FET
PAD	S	Source of power FET. Metal pad on bottom of package.

6. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications.

The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 16. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE}. The clamp circuit should be designed to control the magnitude of V_{SPIKE}. It is recommended to apply an 80% derating from $V_{DS(TRAN)}$ rating (800V) to 700V max for repetitive V_{DS} spikes under the worst case steady-state operating conditions. After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 16 as $V_{PLATEAU}$. It is recommended to design the system such that $V_{PLATEAU}$ follows a typical derating of 80% (560V) from $V_{DS\,(CONT)}$ (700V). Finally, $V_{DS(TRAN)}$ (800V) rating is also provided for events that occur on a non-repetitive basis, such as line surge, lightning strikes, start-up, over-current, short-circuit, load transient, and output voltage transition. 800V $V_{DS(TRAN)}$ ensures excellent device robustness and no-derating is needed for these non-repetitive events, assuming the surge duration is < 100 µs.

For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the $V_{PLATEAU}$ derating guideline (560V).

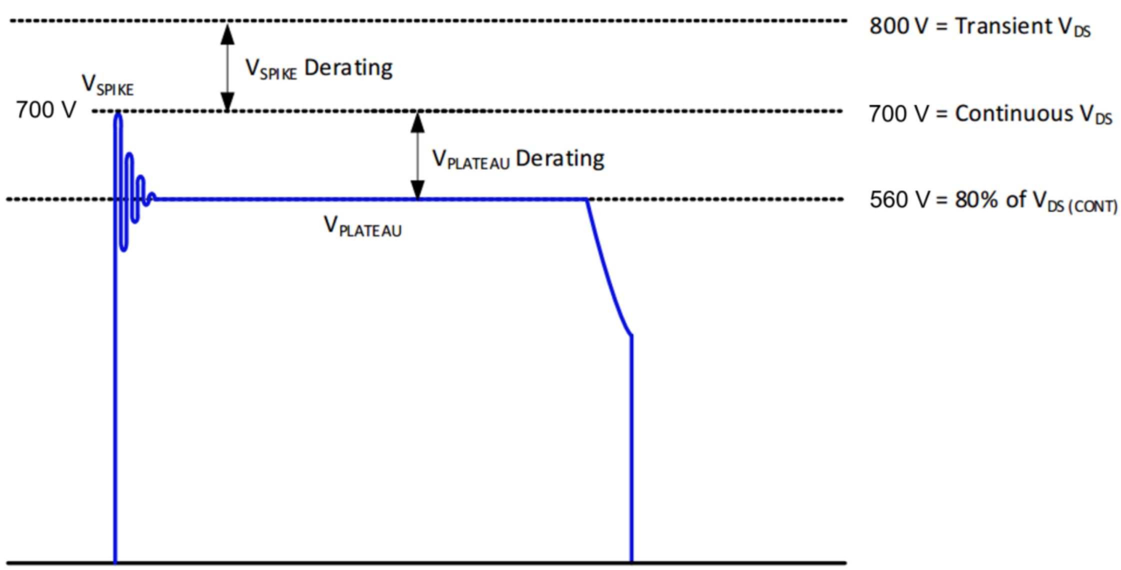
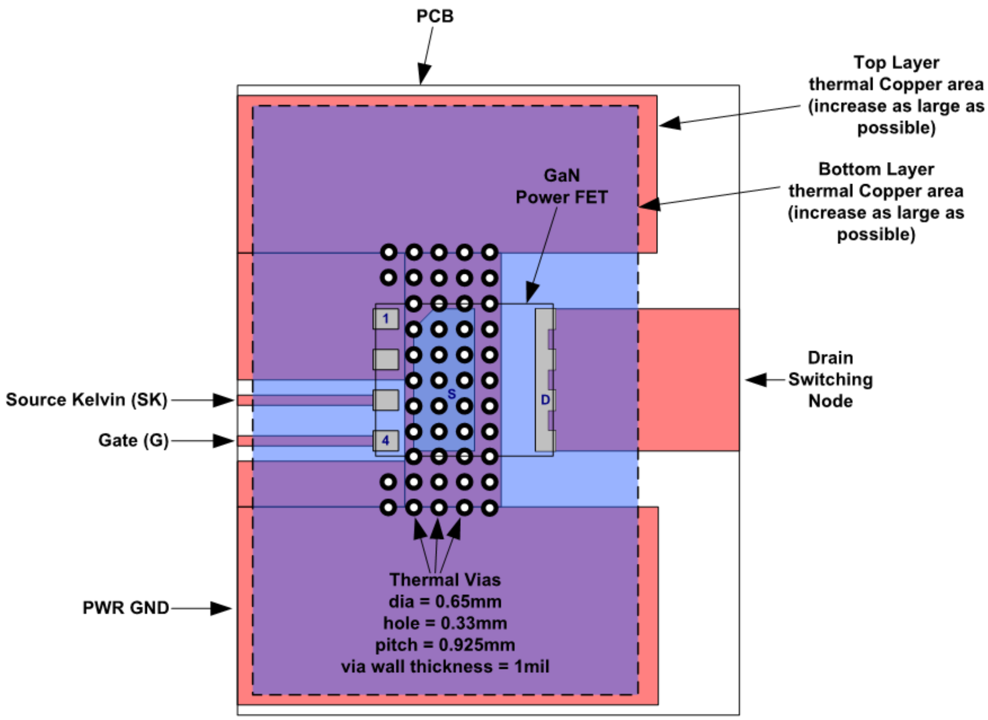


Fig. 176. QR flyback drain-to-source voltage stress diagram

7. PCB Layout Guidelines

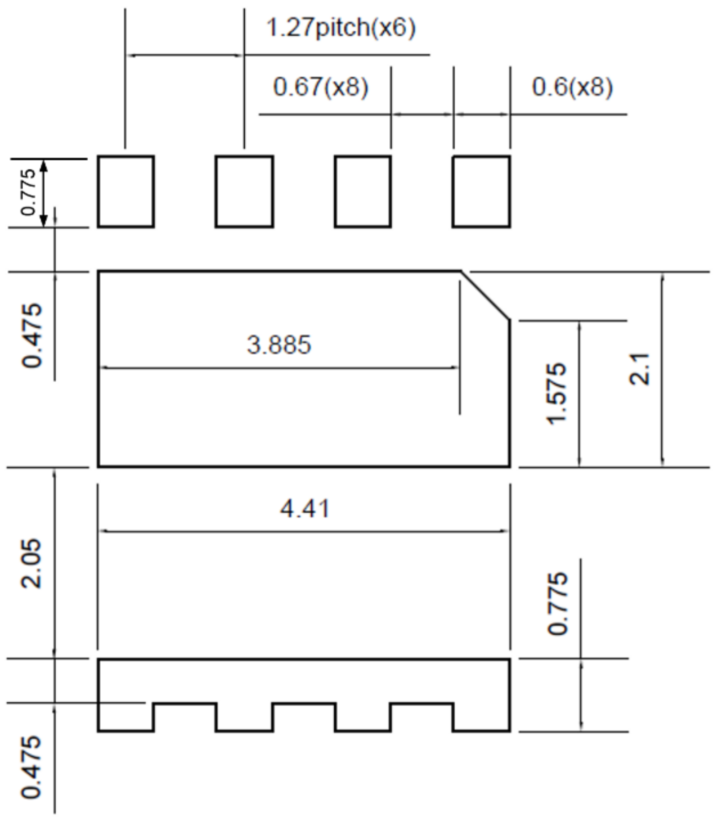
For best electrical and thermal results, the following PCB layout guidelines must be followed:

1) Route all connections on single layer. This allows for large thermal copper areas on other layers.
2) Place large copper areas on and around Source pad.
3) Place many thermal vias inside Source pad and inside source copper areas.
4) Place large as possible copper areas on all other layers (bottom, top, mid1, mid2).



(Top View)

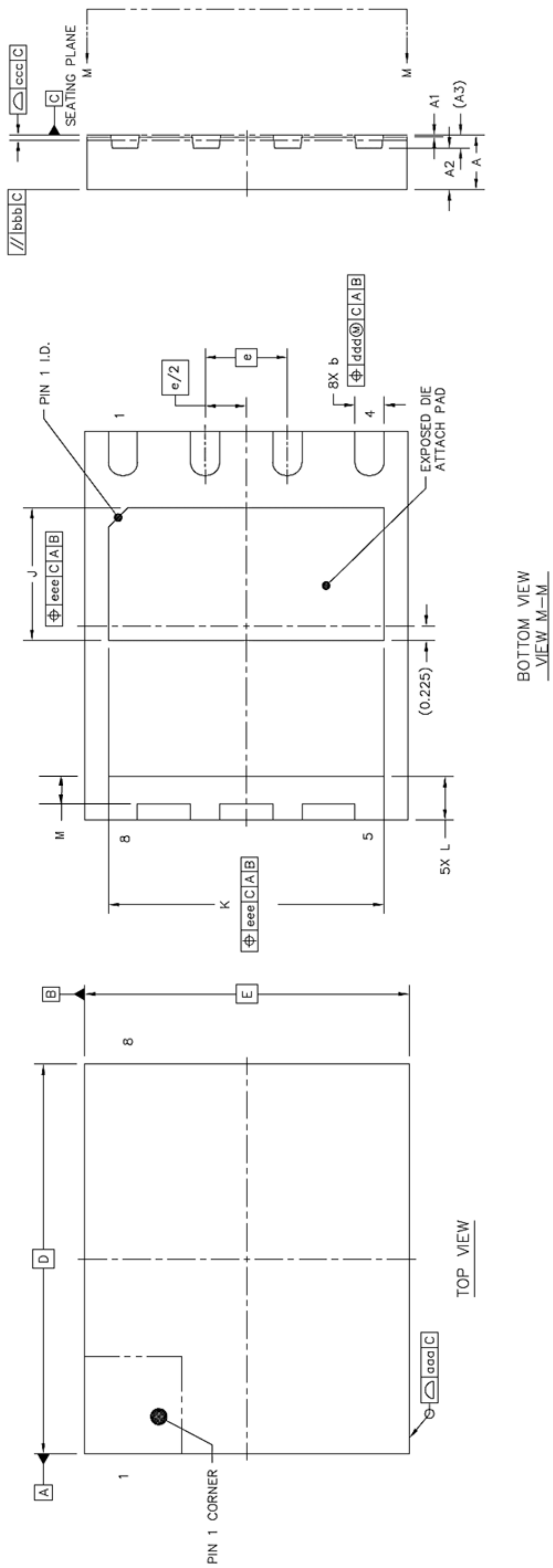
8. Recommended PCB Land Pattern



Top View

All dimensions are in mm

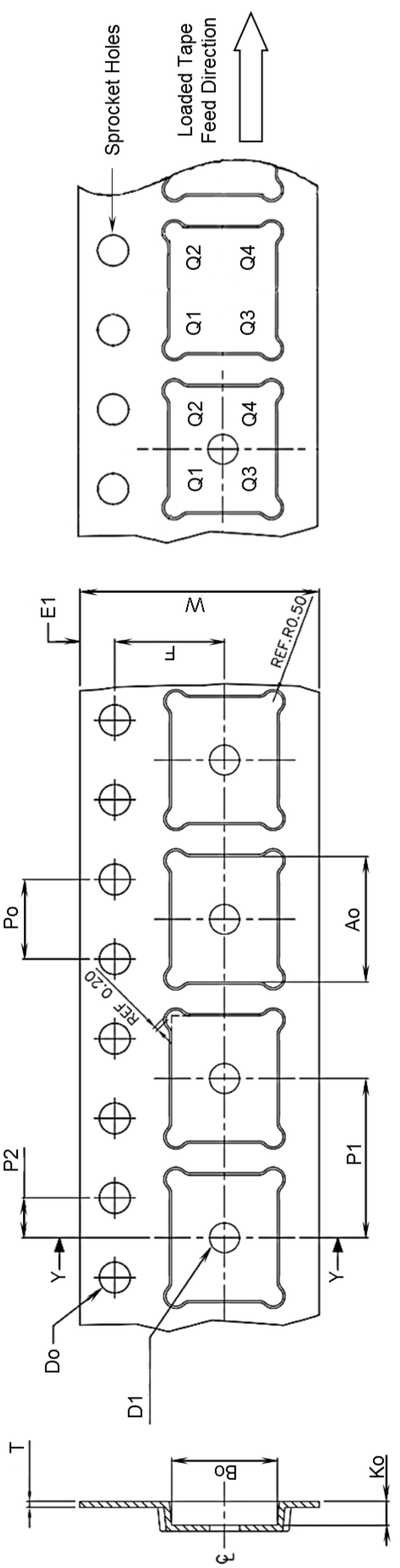
9. QFN Package Outline



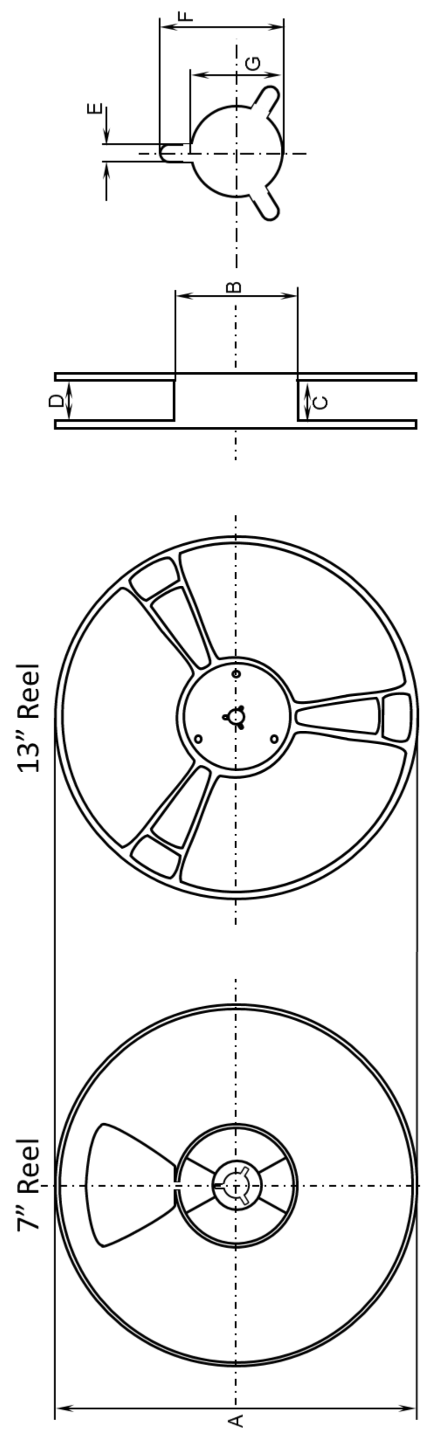
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A3	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		B	0.4	0.45	0.5
BODY SIZE	X	D		6 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		1.27 BSC	

		SYMBOL	MIN	NOM	MAX
EP SIZE	X	J	1.95	2.05	2.15
	Y	K	4.16	4.26	4.36
LEAD LENGTH		L	0.625	0.675	0.725
MERGED LEAD LENGTH		M		0.43	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

10. Tape and Reel Dimensions



Ao (mm)	Bo (mm)	Do (mm)	D1 (mm)	E1 (mm)	F (mm)	Ko (mm)	Po (mm)	P1 (mm)	P2 (mm)	T (mm)	W (mm)	Pin1 Quadrant
6.30 ± 0.1	5.30 ± 0.1	ϕ1.55 ± 0.05	min. ϕ1.50	1.75 ± 0.1	5.50 ± 0.1	1.20 ± 0.1	4.0 ± 0.1	8.00 ± 0.1	2.0 ± 0.1	0.30 ± 0.05	12.00 ± 0.1	Q1



	A (mm)	B (mm)	C (mm)	D (mm)	E (mm)	F (mm)	G (mm)
7" Reel	ϕ180.0 ± 1.5	ϕ62.0	12.4 $^{+2.0}_{-0.0}$	Max. 18.4	2.3 ± 0.2	17.3 ± 0.2	ϕ13.0 $^{+0.5}_{-0.2}$
13" Reel	ϕ330.0 ± 1.5	ϕ100.0 ± 1.5	12.4 $^{+2.0}_{-0.0}$	Max. 18.4	2.2 ± 0.2	17.2 ± 0.2	ϕ13.0 $^{+0.5}_{-0.2}$

11. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing (Tape & Reel)
NV6017C-RA	-55 °C to +150 °C T_{CASE}	-55 °C to +150 °C T_{CASE}	5 x 6 mm QFN	3	1,000 : 7" Reel
NV6017C	-55 °C to +150 °C T_{CASE}	-55 °C to +150 °C T_{CASE}	5 x 6 mm QFN	3	5,000 : 13" Reel

12. Revision History

Date	Status	Notes
Oct 10, 2023	**PRELIMINARY**	**First publication**
Mar 11, 2024	**PRELIMINARY**	**Graphs and Tables Updated**
Sept 5, 2024	**FINAL**	**EC table and Graphs Updated**

Additional Information

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