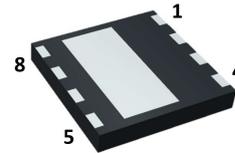


## GaNFast™ Power FET

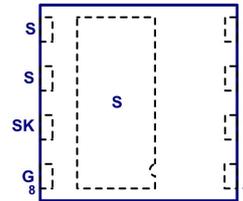
### 1. Features

#### GaNFast™ Power FET

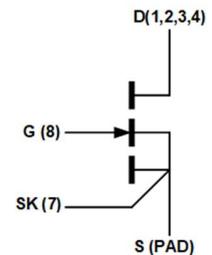
- eMode GaN power FET
- Low 50 mΩ resistance
- 10 MHz switching frequency capability
- Ultra-low gate charge
- Zero reverse recovery charge
- Low output charge
- 800 V Transient Voltage Rating
- 600 V Continuous Voltage Rating
- Source Kelvin (SK) pin for gate noise immunity
- Small, low-profile SMT PDFN
- 8x8 mm PCB footprint
- Minimized package inductance
- Low thermal resistance
- Bottom-side cooled



PDFN 8x8 mm



Package Outline (Top View)



Simplified Schematic

#### Environmental

- RoHS, Pb-free, REACH-compliant

### 2. Topologies / Applications

- AC-DC, DC-DC, DC-AC
- QR flyback, ACF, buck, boost, half bridge, full bridge, LLC resonant, Class D, PFC
- Wireless power
- LED lighting
- Solar Micro-inverters
- TV SMPS
- Server, Telecom

### 3. Description

This GaNFast™ power FET is a high performance eMode GaN FET that achieves excellent high-frequency and high efficiency operation. Features include a simple gate input and a Source Kelvin pin for noise immunity.

This GaN power FET combines the highest dV/dt immunity and industry-standard low-profile, low-inductance, bottom-side cooled SMT PDFN packaging to enable designers to achieve simple, quick and reliable solutions.

Navitas' GaN technology extends the capabilities of traditional topologies such as flyback, half-bridge, buck/boost, LLC and other resonant converters to reach MHz+ frequencies with very high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

#### 4. Table of Contents

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## 5. Specifications

### 5.1. Absolute Maximum Ratings<sup>(1)</sup>

(with respect to Source (pad) unless noted)

SYMBOL	PARAMETER	MAX	UNITS
$V_{DS(TRAN)}$	Transient Drain-to-Source Voltage <sup>(2)</sup>	800	V
$V_{DS(CONT)}$	Continuous Drain-to-Source Voltage	-7 to +600	V
$V_{GS}$	Continuous Gate-to-Source Voltage	-10 to +6.6	V
$V_{TGS}$	Transient Gate-to-Source Voltage <sup>(3)</sup>	-20 to +10	V
$I_D$	Continuous Drain Current (@ $T_C = 25^\circ\text{C}$ )	30	A
$I_D$	Continuous Drain Current (@ $T_C = 100^\circ\text{C}$ )	20	A
$I_D$ PULSE	Pulsed Drain Current (10 $\mu\text{s}$ @ $T_J = 25^\circ\text{C}$ )	60	A
$P_D$	Power Dissipation (@ $T_C = 25^\circ\text{C}$ )	135	W
dV/dt	Slew Rate on Drain-to-Source	200	V/ns
$T_J$	Operating Junction Temperature	-55 to 150	$^\circ\text{C}$
$T_{STOR}$	Storage Temperature	-55 to 150	$^\circ\text{C}$

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2)  $V_{DS(TRAN)}$  rating allows for surge ratings during non-repetitive events that are < 100 $\mu\text{s}$  (for example start-up, line interruption).  $V_{DS(TRAN)}$  rating allows for repetitive events that are < 100ns, with 80% derating required (for example repetitive leakage inductance spikes). Refer to Section 7 for detailed recommended design guidelines.

(3) < 1  $\mu\text{s}$

### 5.2. Thermal Resistance

SYMBOL	PARAMETER	TYP	UNITS
$R_{\theta JC}$ <sup>(4)</sup>	Junction-to-Case	0.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$ <sup>(4)</sup>	Junction-to-Ambient	43	$^\circ\text{C}/\text{W}$

(4)  $R_\theta$  measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

### 5.3. Electrical Characteristics

Typical conditions:  $V_{DS} = 400\text{ V}$ ,  $F_{SW} = 1\text{ MHz}$ ,  $T_{AMB} = 25\text{ °C}$ ,  $I_D = 12\text{ A}$  (or specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
<b>GaN FET Characteristics</b>						
$I_{DSS}$	Drain-Source Leakage Current		0.3	25	$\mu\text{A}$	$V_{DS} = 600\text{ V}$ , $V_{GS} = 0\text{ V}$
$I_{DSS}$	Drain-Source Leakage Current		35		$\mu\text{A}$	$V_{DS} = 600\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_C = 150\text{ °C}$
$I_{GSS}$	Gate-Source Leakage Current		120		$\mu\text{A}$	$V_{GS} = 6\text{ V}$
$R_{DS(ON)}$	Drain-Source Resistance		50	70	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$ , $I_D = 12\text{ A}$ , $T_J = 25\text{ °C}$
$R_{DS(ON)}$	Drain-Source Resistance		115		$\text{m}\Omega$	$V_{GS} = 6\text{ V}$ , $I_D = 12\text{ A}$ , $T_J = 150\text{ °C}$
$V_{GS(th)}$	Gate Threshold Voltage	1	1.7	2.8	V	$I_D = 24\text{ mA}$ , $V_{DS} = 0.1\text{ V}$
$V_{SD}$	Source-Drain Reverse Voltage		3.2	5	V	$V_{GS} = 0\text{ V}$ , $I_{SD} = 12\text{ A}$
$T_{ON}$	Turn-On Delay Time		5		ns	$V_{DS} = 400\text{ V}$ , $V_{GS} = 5.2\text{ V}$ , $I_D = 11\text{ A}$ , $R_G = 10\text{ }\Omega$
$T_{OFF}$	Turn-Off Delay Time		5		ns	$V_{DS} = 400\text{ V}$ , $V_{GS} = 5.2\text{ V}$ , $I_D = 11\text{ A}$ , $R_G = 10\text{ }\Omega$
$T_R$	Turn-Off Rise Time		10		ns	$V_{DS} = 400\text{ V}$ , $V_{GS} = 5.2\text{ V}$ , $I_D = 11\text{ A}$ , $R_G = 10\text{ }\Omega$
$T_F$	Turn-On Fall Time		7		ns	$V_{DS} = 400\text{ V}$ , $V_{GS} = 5.2\text{ V}$ , $I_D = 11\text{ A}$ , $R_G = 10\text{ }\Omega$
$Q_{RR}$	Reverse Recovery Charge		0		nC	
$R_G$	Internal Gate Resistance		0.5		$\Omega$	
$C_{ISS}$	Input Capacitance		227		pF	$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$
$C_{OSS}$	Output Capacitance		65		pF	$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$
$C_{RSS}$	Reverse Transfer Capacitance		0.94		pF	$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$
$Q_G$	Total Gate Charge		8.0		nC	$V_{GS} = 0\text{--}6\text{ V}$ , $I_D = 14.5\text{ A}$ , $V_{DS} = 400\text{ V}$
$Q_{GD}$	Gate-to-Drain Charge		2.7		nC	$V_{GS} = 0\text{--}6\text{ V}$ , $I_D = 14.5\text{ A}$ , $V_{DS} = 400\text{ V}$
$Q_{GS}$	Gate-to-Source Charge		1.1		nC	$V_{GS} = 0\text{--}6\text{ V}$ , $I_D = 14.5\text{ A}$ , $V_{DS} = 400\text{ V}$
$Q_{OSS}$	Output Charge		51		nC	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$
$C_{O(er)}^{(5)}$	Effective Output Capacitance, Energy Related		84		pF	$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$
$C_{O(tr)}^{(6)}$	Effective Output Capacitance, Time Related		126		pF	$V_{DS} = 400\text{ V}$ , $V_{GS} = 0\text{ V}$

(5)  $C_{O(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 400 V

(6)  $C_{O(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 400 V

### 5.4. Characteristic Graphs

(GaN FET,  $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

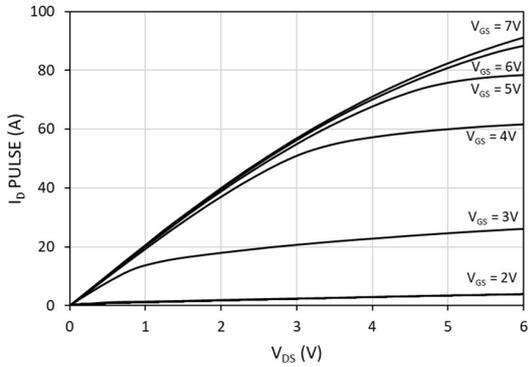


Fig. 1. Pulsed drain current ( $I_D \text{ PULSE}$ ) vs. drain-to-source voltage ( $V_{DS}$ ) at  $T = 25\text{ }^\circ\text{C}$

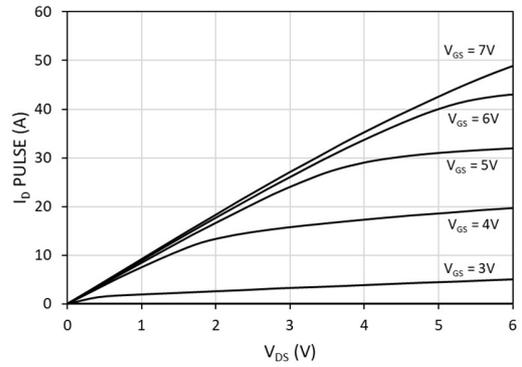


Fig. 2. Pulsed drain current ( $I_D \text{ PULSE}$ ) vs. drain-to-source voltage ( $V_{DS}$ ) at  $T = 150\text{ }^\circ\text{C}$

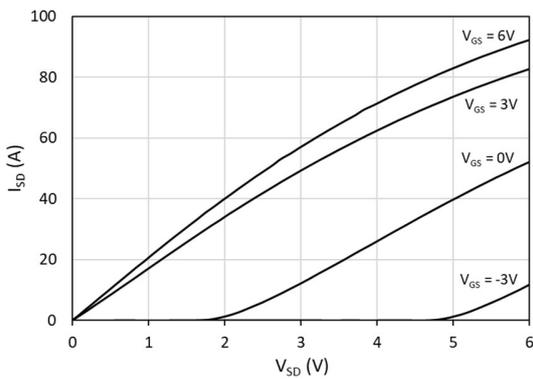


Fig. 3. Source-to-drain reverse conduction voltage at  $T = 25\text{ }^\circ\text{C}$

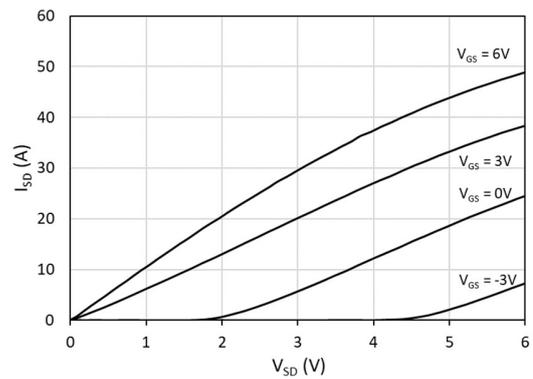


Fig. 4. Source-to-drain reverse conduction voltage at  $T = 150\text{ }^\circ\text{C}$

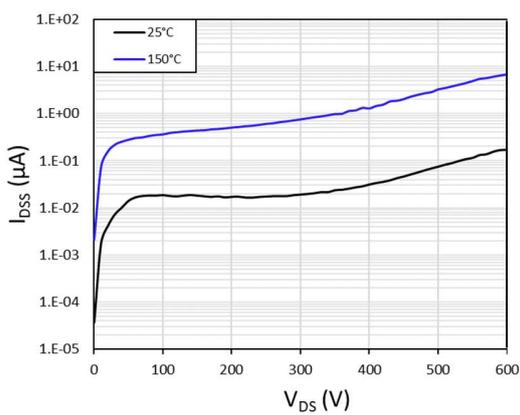


Fig. 5. Drain-to-source leakage current ( $I_{DSS}$ ) vs. drain-to-source voltage ( $V_{DS}$ )

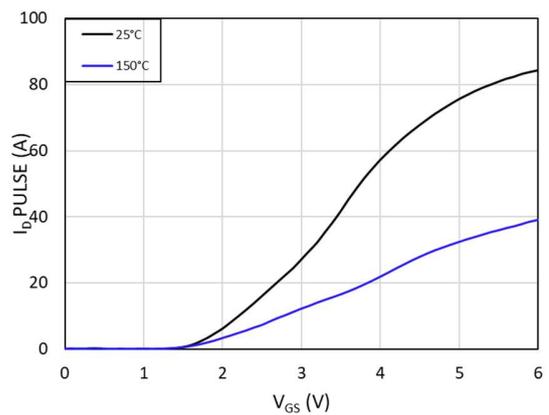


Fig. 6. Pulsed drain current ( $I_D \text{ PULSE}$ ) vs. gate-to-source voltage ( $V_{GS}$ )

Characteristic Graphs (Cont.)

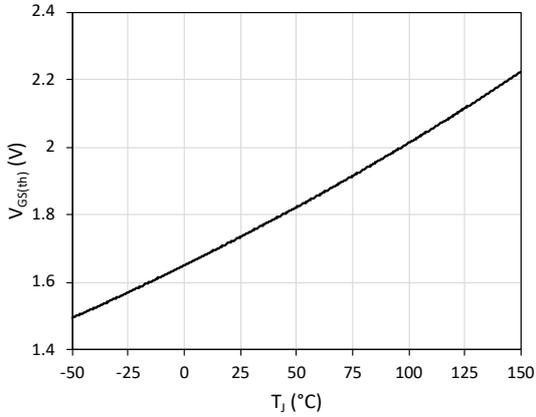


Fig. 7. Gate threshold voltage ( $V_{GS(th)}$ ) vs. junction temperature ( $T_J$ )

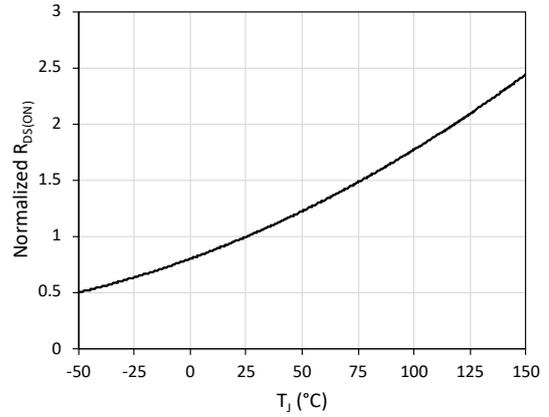


Fig. 8. Normalized on-resistance ( $R_{DS(ON)}$ ) vs. junction temperature ( $T_J$ )

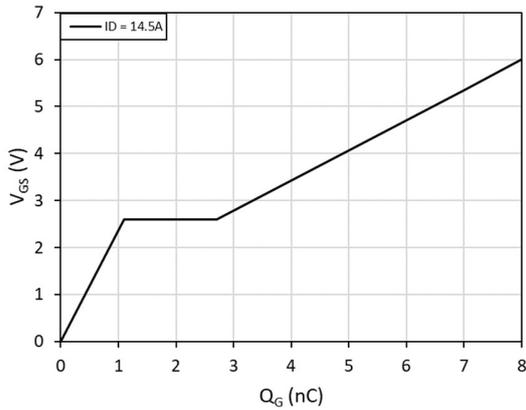


Fig. 9. Gate-to-source voltage ( $V_{GS}$ ) vs. total gate charge ( $Q_G$ )

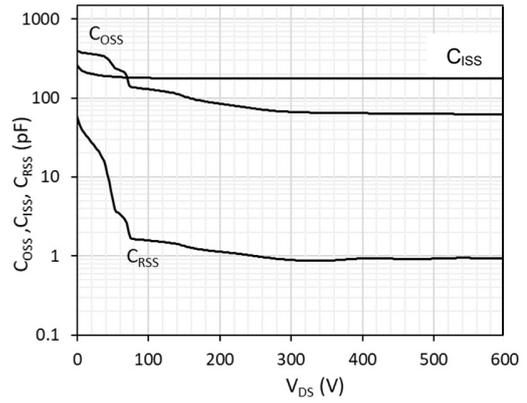


Fig. 10. Input capacitance ( $C_{ISS}$ ), Output capacitance ( $C_{OSS}$ ), Reverse Transfer capacitance ( $C_{RSS}$ ), vs drain-to-source voltage ( $V_{DS}$ )

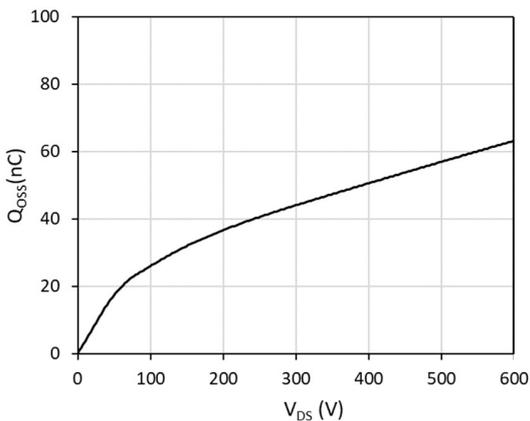


Fig. 11. Charge stored in output capacitance ( $Q_{OSS}$ ) vs drain-to-source voltage ( $V_{DS}$ )

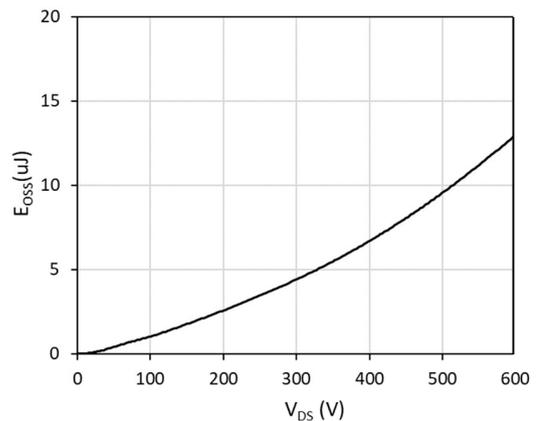


Fig. 12. Energy stored in output capacitance ( $E_{OSS}$ ) vs. drain-to-source voltage ( $V_{DS}$ )

Characteristic Graphs (Cont.)

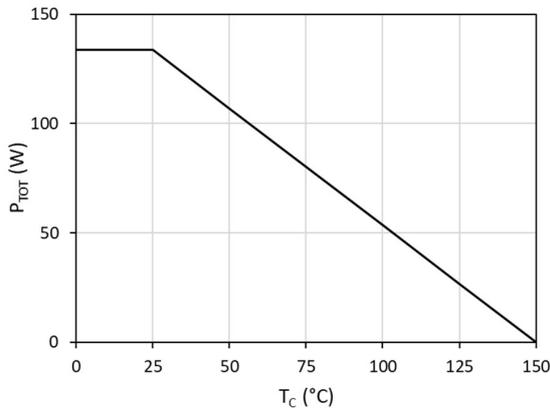


Fig. 13. Power Dissipation ( $P_{TOT}$ ) vs case temperature

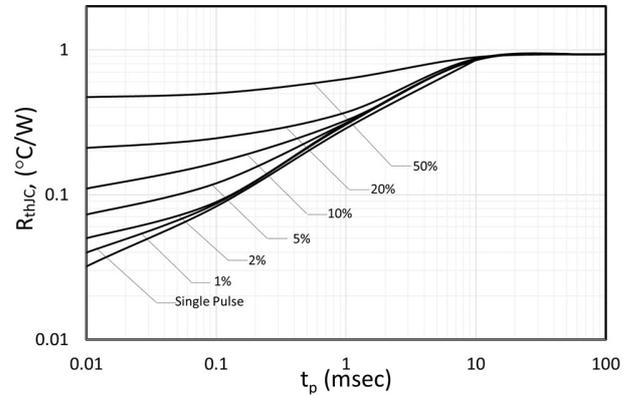


Fig. 14. Max. Thermal Transient Impedance ( $Z_{thJC}$ ) vs. Pulse Width ( $t_p$ )

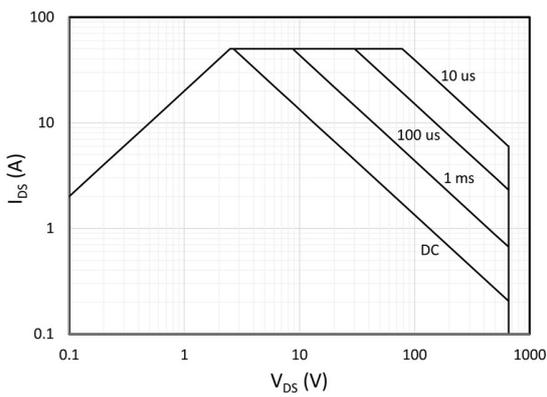
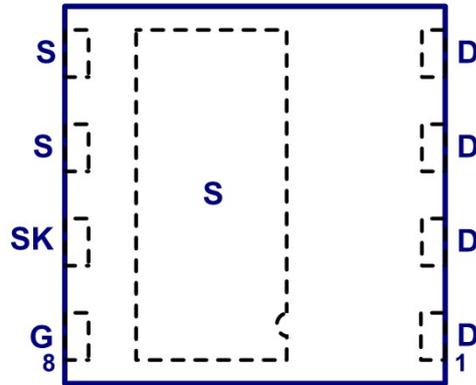
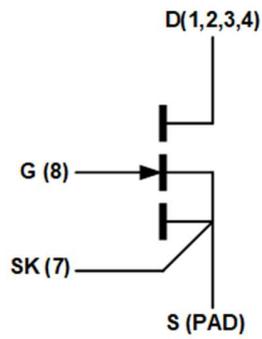


Fig. 15. Safe Operation Area (SOA) @  $T_{CASE} = 25^\circ C$

## 6. Pin Configurations and Functions



Package Top View

Pin Number	Pin Name	Description
5, 6	S	Source of power FET
7	SK	Kelvin sense of FET source. Use for driver connection
8	G	Gate of power FET
1, 2, 3, 4	D	Drain of power FET
PAD	S	Source of power FET. Metal pad on bottom of package.

## 7. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 16. When the device is switched off, the energy stored in the transformer leakage inductance will cause  $V_{DS}$  to overshoot to the level of  $V_{SPIKE}$ . The clamp circuit should be designed to control the magnitude of  $V_{SPIKE}$ . After dissipation of the leakage energy, the device  $V_{DS}$  will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 16 as  $V_{DS-OFF}$ .

- For repetitive events, 80% derating should be applied from  $V_{DS(TRAN)}$  rating (800V) to 640V max under the worst case operating conditions.
- It is recommended to design the system such that  $V_{DS-OFF}$  is derated 80% from the  $V_{DS(CONT)}$  (600V) max rating to 480V.
- For half-bridge based topologies, such as LLC,  $V_{DS}$  voltage is clamped to the bus voltage.  $V_{DS}$  should be designed such that it meets the  $V_{DS-OFF}$  derating guideline (520V).
- Non-repetitive events are infrequent, one-time conditions such as line surge, ESD, and lightning. No derating from the  $V_{DS(TRAN)}$  rating (800V) is needed for non-repetitive  $V_{SPIKE}$  durations  $< 100 \mu s$ . The  $V_{DS(TRAN)}$  rating (800V) allows for repetitive events that are  $< 100 ns$ , with 80% derating required (for example repetitive leakage inductance spikes).

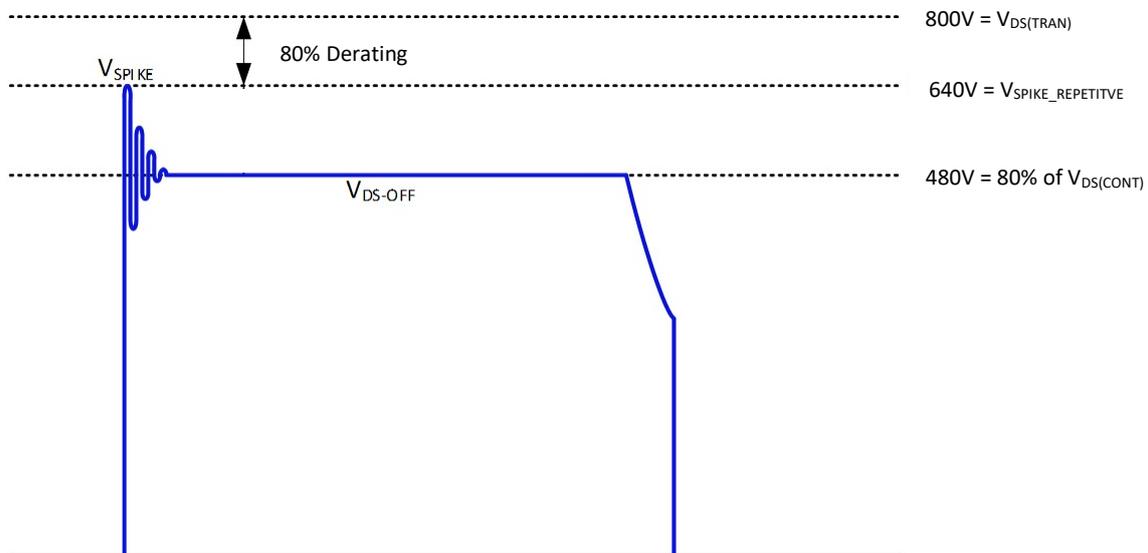
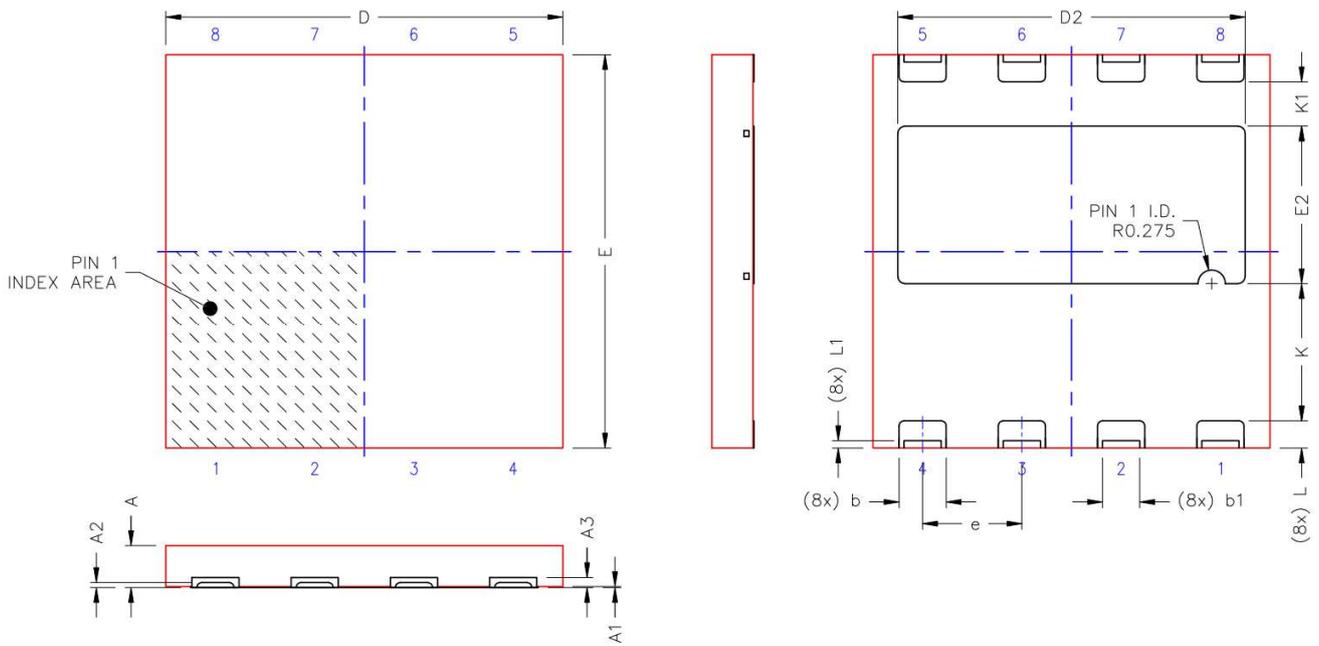


Fig. 16. QR flyback drain-to-source voltage stress diagram

### 8. DFN Package Outline



SYM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	-	0.05
A2	-	0.102 REF.	-
A3	-	0.203 REF.	-
b	0.90	0.95	1.00
b1	-	0.75 REF.	-
D	7.90	8.00	8.10
D2	6.95	7.00	7.05
E	7.90	8.00	8.10
E2	3.15	3.20	3.25
e	-	2.00 TYP.	-
K	-	2.80 REF.	-
K1	-	0.90 REF.	-
L	0.50	0.55	0.60
L1	-	0.15 REF.	-

**NOTES:**

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. MAXIMUM ALLOWABLE BURRS IS 0.050 MM IN ALL DIRECTIONS.

## 9. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing (Tape & Reel)
NV6029A	-55 °C to +150 °C T <sub>CASE</sub>	-55 °C to +150 °C T <sub>CASE</sub>	8 x 8 mm PDFN	3	3,000 : 13" Reel

## 10. Revision History

Date	Status	Notes
April 05, 2022	Final	First publication
July 27, 2022	Final	Add HV Timing Parameters
July 18, 2023	Final	Update package image with pinout (front page)
Aug 21, 2023	Final	Update ID and ID_pulse (Abs Max section)
Nov 3, 2023	Final	Update FET capacitance parameters (Crss, Coss, Ciss, Rg) Add FET RDSON @ Tj = 150C (typ)
Nov 27, 2023	Final	Add P <sub>D</sub> parameter to Abs Max Table
Apr. 17, 2024	Final	Update POD, update VDSmax footnote, update Section 7 Drain-to-Source Voltage Considerations, update 13" Reel to 3k
Feb. 7, 2025	Final	Update POD, update VDSmax(cont) = 600V, VGSmax(cont) = 6.6V, electrical parameters & characteristic curves for 600V, update Section 7 for 600V
Dec. 12, 2025	Final	Remove 7" reel in 9. Ordering information.

## Additional Information

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Contact [info@navitassemi.com](mailto:info@navitassemi.com)

