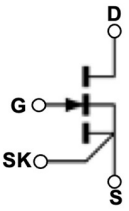
GaNFast™ Power FET

Top-cooled
TOLT-16L



1. Features

- eMode GaN power FET
  - V_{DS} 650V continuous / 800V transient
  - 11 mΩ $R_{DS(ON)\_TYP\_25C}$
  - TOLT-16L thermally-enhanced, top-cooled
  - Zero reverse-recovery charge
  - Up to 2 MHz operation
  - V_{DS} dV/dt immunity up to 200 V/ns
- RoHS, Pb-free, REACH-compliant

2. Applications / Topologies

- Residential Solar Micro Inverters and ESS
- AC-DC, DC-DC, DC-AC topologies
- CCM BTP PFC and LLC topologies

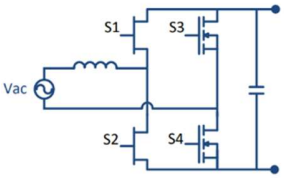
3. Description

NV6066 is a high performance eMode GaNFET that achieves excellent high-frequency and high efficiency operation. Features include Source Kelvin for minimized gate loop inductance and improved noise immunity.

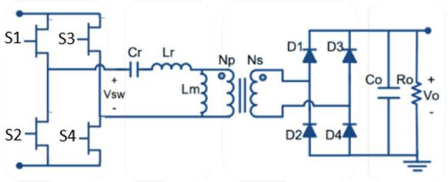
NV6066 also implements a thermally-enhanced top-cooled SMD with gull wing leads for superior board level temp cycling.

NV6066 is the ideal choice for topologies utilizing MHz+ F_{SW} for high efficiency LLC and other ZVS topologies, to achieve unprecedented power density and cost-effective system BOM, in Consumer, Enterprise, and Solar segments.

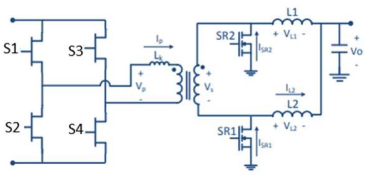
4. Typical Application Circuits



BTP PFC



CLLC or LLC



PSFB or DAB

5. Table of Contents

6. Absolute Maximum Ratings(Note 1) (with respect to Source, T_{CASE} = 25°C, unless specified)

Symbol	Parameter	Max	Units
$V_{DS\_(CONT)}$	Continuous Drain-to-Source voltage	-7 to +650	V
$V_{DS\_(TRAN)}$	Transient Drain-to-Source voltage (Note 2)	800	V
V_{GS}	Continuous Gate-to-Source Voltage	-10 to +7.0	V
$V_{GS\_(TRAN)}$	Transient Gate-to-Source Voltage	-20 to +10	V
$I_{DS\_(CONT)}$	Continuous current (T_{CASE} = 25 °C) Continuous current (T_{CASE} = 100 °C)	170 105	A
$I_{DS\_(PULSE)}$	Pulsed current (10 µs @ T_{JUNC} = 25 °C) Pulsed current (10 µs @ T_{JUNC} = 150 °C)	330 150	A
dV/dt	Drain-to-Source Slew Rate	200	V/ns
T_{JUNC}	Operating Junction Temperature	-40 to +150	°C
T_{STOR}	Storage temperature	-55 to +150	°C

(1) Absolute Maximum Ratings are stress ratings, and subjecting devices to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS\_(TRAN)}$ allows for surge ratings during non-repetitive events that are < 100 µs. Refer to Application Section for recommended design guidelines.

7. Thermal Resistance

Symbol	Parameter	Typ	Units
$R_{\theta\_JUNC-CASE}$	Junction-to-Case Thermal Resistance	0.13	°C/W

8. Electrical Characteristics

Conditions unless specified: V_{DS} = 400V, V_{GS} = 6.0V, T_{CASE} = 25°C, I_{DS} = 35A

Symbol	Parameter	Min	Typ	Max	Units	Conditions
GaN Switch Characteristics						
I_{DSS}	Drain-Source leakage current		3	100	µA	V_{DS} = 650 V, V_{GS} = 0 V
I_{DSS}	Drain-Source leakage current		45		µA	V_{DS} = 650 V, V_{GS} = 0V, T_{JUNC} = 150 °C
I_{GSS}	Gate-Source leakage current		300		µA	V_{GS} = 6.0V
$R_{DS(ON)}$	Drain-Source resistance		11	15	mΩ	V_{GS} = 6.0V, I_{DS} = 35A
$V_{GS(th)}$	Gate Threshold voltage		1.5	2.8	V	I_{DS} = 100mA, V_{DS} = 0.1V
V_{SD}	Source-Drain Reverse voltage		3.3	5	V	V_{GS} = 0V, I_{SD}=35A
Q_{RR}	Reverse recovery charge		Zero		nC	
R_G	Internal Gate Resistance		0.3		Ω	
C_{ISS}	Input capacitance		1080		pF	V_{DS} = 400 V, V_{GS} = 0V
C_{OSS}	Output capacitance		260		pF	V_{DS} = 400V, V_{GS} = 0V
C_{RSS}	Reverse Transfer capacitance		1.8		pF	V_{DS} = 400V, V_{GS} = 0V
Q_{GATE}	Total Gate charge		29.2		nC	V_{DS} = 400V, V_{GS} = 0V to 6.0V
Q_{GS}	Gate-to-Source charge		6.4		nC	V_{DS} = 400V, V_{GS} = 0V to 6.0V
Q_{GD}	Gate-to-Drain charge		9		nC	V_{DS} = 400V, V_{GS} = 6.0V
Q_{OSS}	Output charge		230		nC	V_{DS} = 400V, V_{GS} = 0V
$C_{O(er)}$ (Note 4)	Effective output capacitance, energy related		376		pF	V_{DS} = 400V, V_{GS} = 0V
$C_{O(tr)}$ (Note 5)	Effective output capacitance, time related		575		pF	V_{DS} = 400V, V_{GS} = 0V

(4) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(5) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

9. Electrical Curves (GaN FET, T_{CASE} = 25 °C unless otherwise specified)

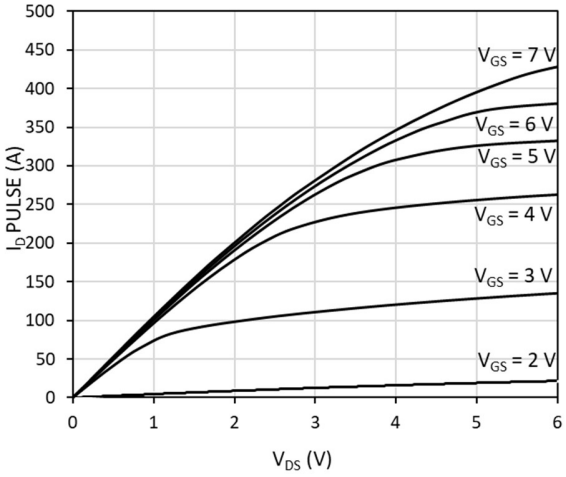


Fig. 1. I_{DS_PULSE} vs. V_{DS} , T_{JUNC} = 25 °C

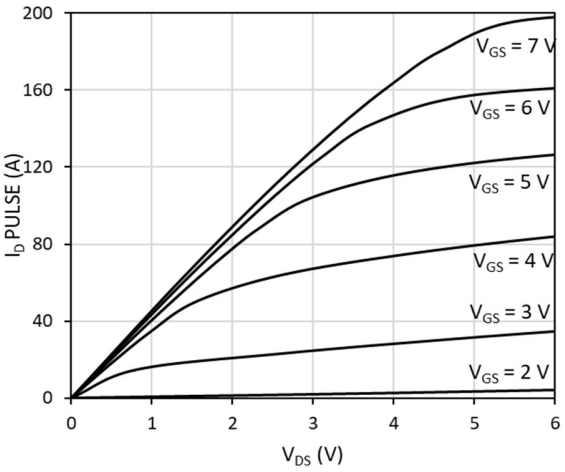


Fig. 2. I_{DS_PULSE} vs. V_{DS} , T_{JUNC} = 150 °C

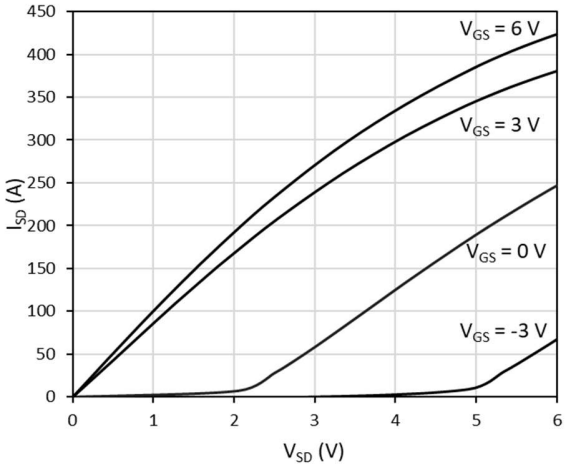


Fig. 3. V_{SD} (reverse conduction), T_{JUNC} = 25 °C

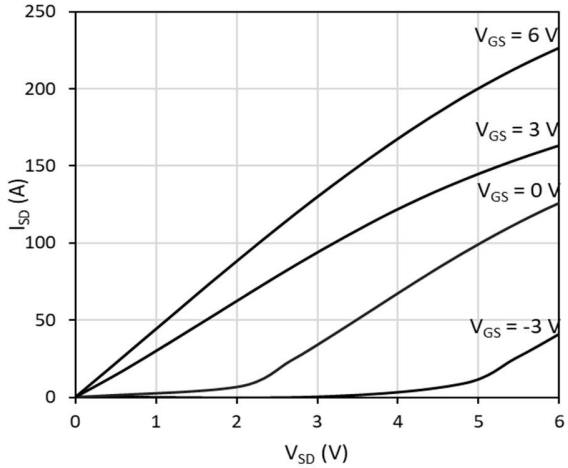


Fig. 4. V_{SD}, T_{JUNC} = 150 °C

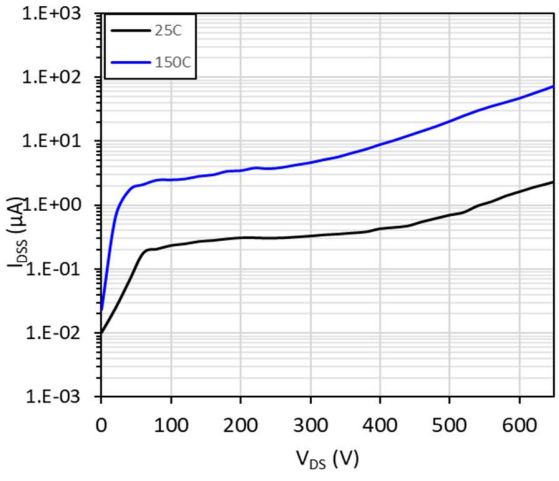


Fig. 5. I_{DSS} vs. V_{DS} (V_{GS} = 0V), T_{JUNC} = 25 ^{0}C, 150 ^{0}C

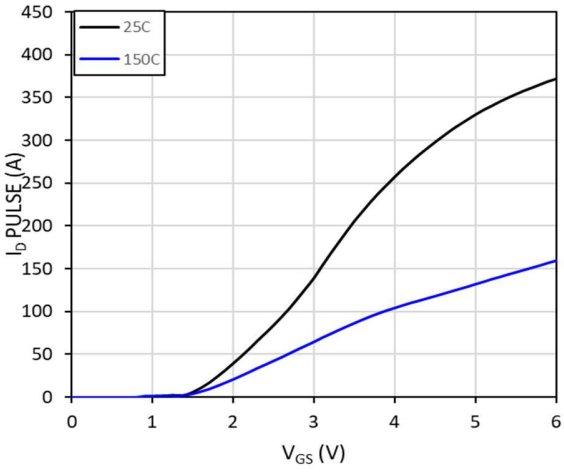


Fig. 6. I_{DS_PULSE} vs. V_{GS}

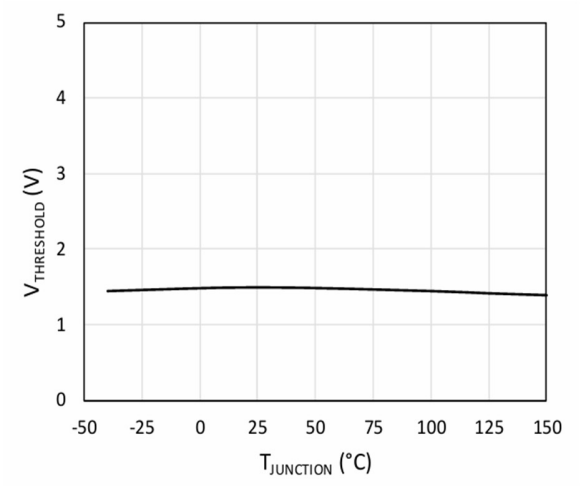


Fig. 7. $V_{GS(th)}$ vs. T_{JUNC}

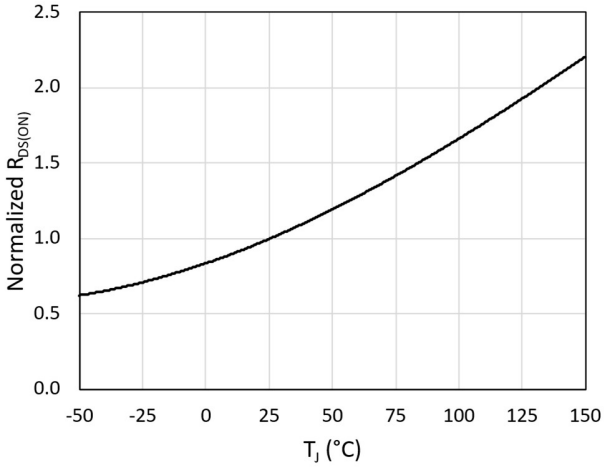


Fig. 8. Normalized $R_{DS(ON)}$ vs. T_{JUNC}

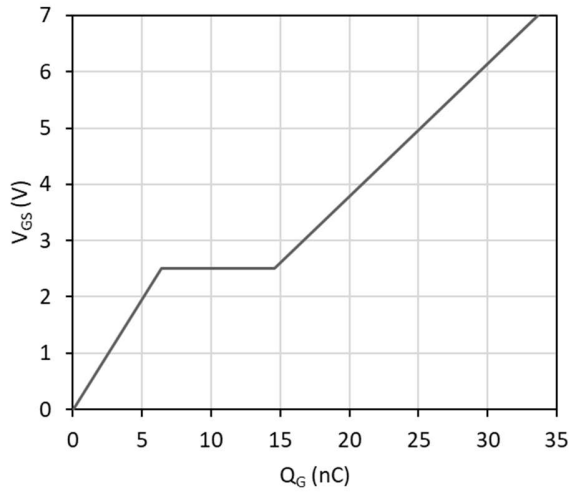


Fig. 9. V_{GS} vs. Q_{GATE}

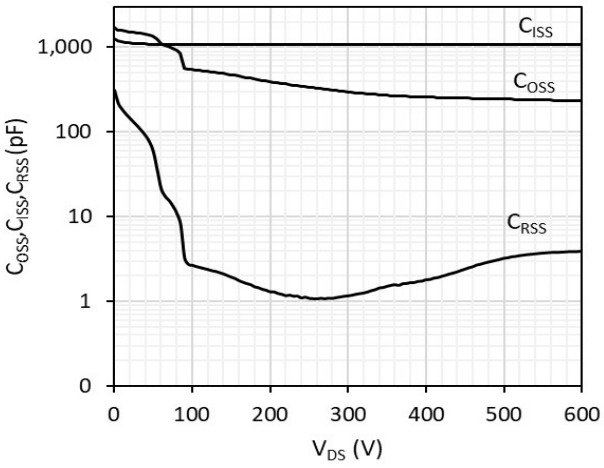


Fig. 10. C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

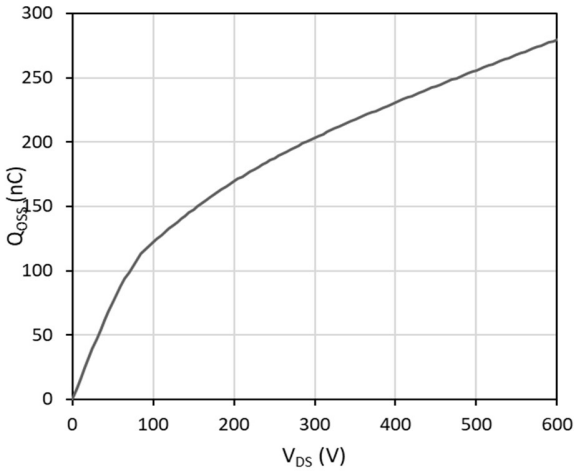


Fig. 11. Q_{OSS} vs. V_{DS}

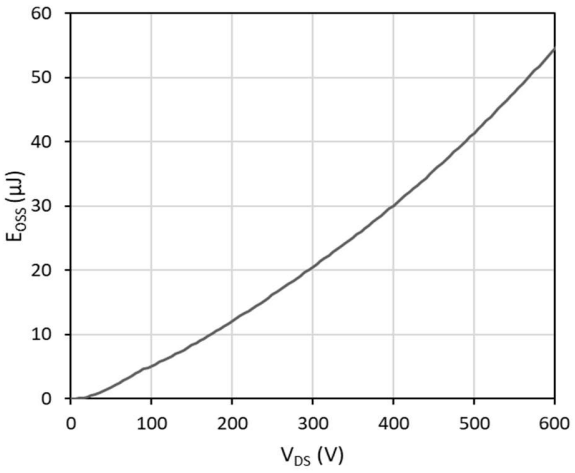


Fig. 12. E_{OSS} vs. V_{DS}

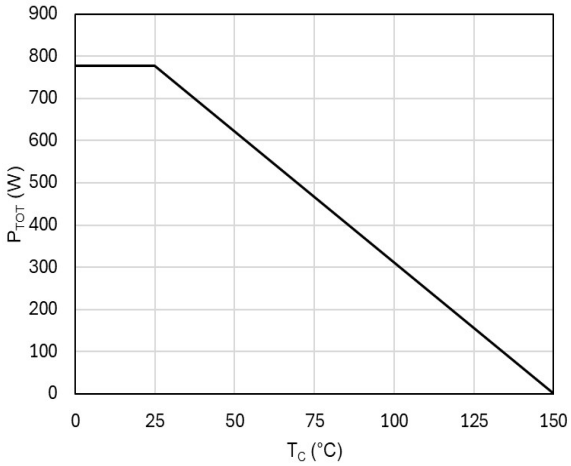


Fig 13. $P_{DISSIPATION}$ vs. T_{CASE}

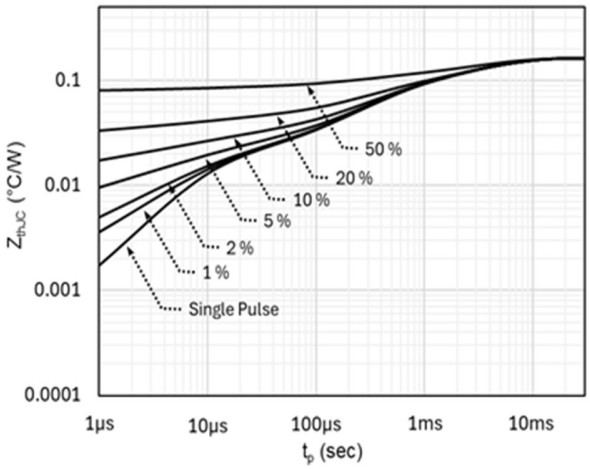


Fig. 14. Transient $R_{\Theta\_JUNC\text{-}CASE}$

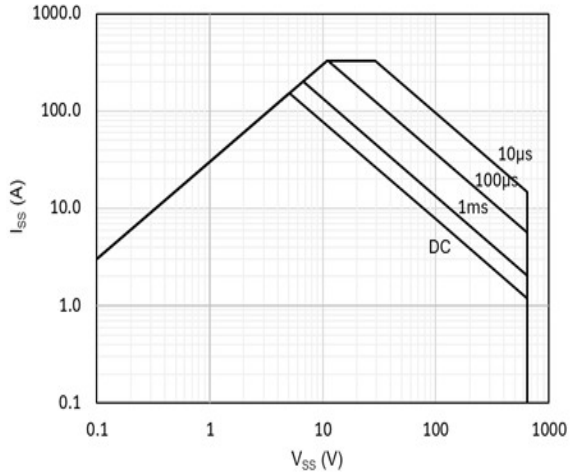
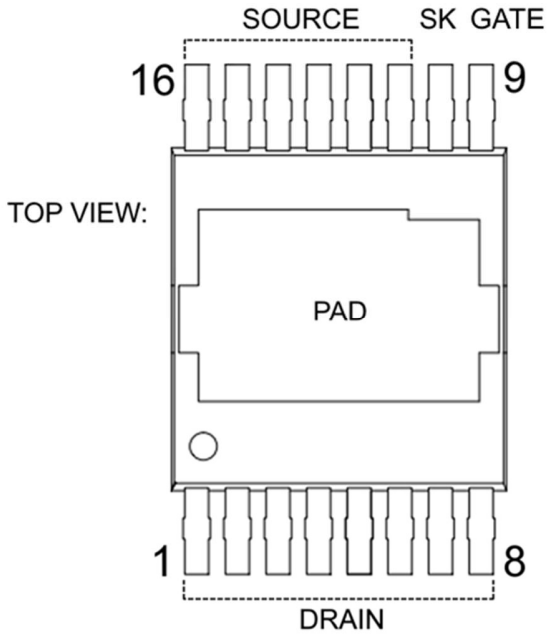


Fig. 15. Safe Operating Area, T_{CASE}= 25°C

10. Pinout Table and P/N Marking



PIN		I/O	Description
NUMBER	SYMBOL		
11 – 16	S	O	Source Terminal
10	SK	G	Kelvin Source
9	G	I	Gate of GaN FET
1 – 8	D	P	Drain of GaN FET
PAD	S	O, G	Source of GaN FET and Thermal Pad for Heatsink

Note: I = Input, O = Output, P = Power, G = GaN IC Ground

11. Drain-to-Source Voltage Considerations

GaN Power FETs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies such as quasi-resonant (QR) or flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 16. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE}. The clamp circuit should be designed to control the magnitude of V_{SPIKE}. It is recommended to apply an 80% derating from $V_{DS(TRAN)}$ rating (800V) to 650V max for repetitive V_{DS} spikes under the worst case steady-state operating conditions. After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 16 as $V_{PLATEAU}$. It is recommended to design the system such that $V_{PLATEAU}$ follows a typical derating of 80% (520V) from $V_{DS\ (CONT)}$ (650V). Finally, $V_{DS(TRAN)}$ (800V) rating is also provided for events that occur on a non-repetitive basis, such as line surge, lightning strikes, start-up, over-current, short-circuit, load transient, and output voltage transition. 800V $V_{DS(TRAN)}$ ensures excellent device robustness and no-derating is needed for these non-repetitive events, assuming the surge duration is < 100 µs.

For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the $V_{PLATEAU}$ derating guideline (520V).

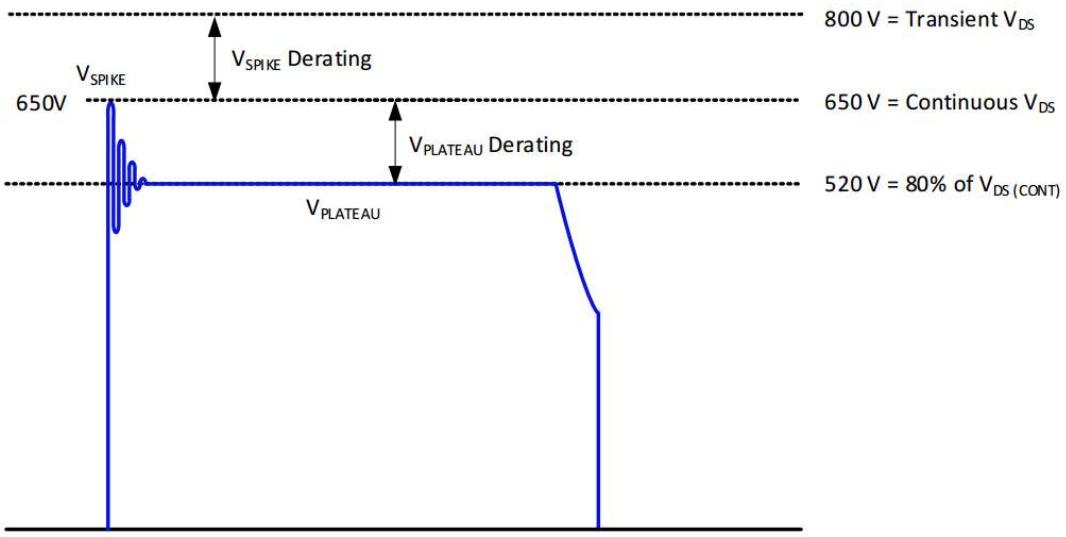
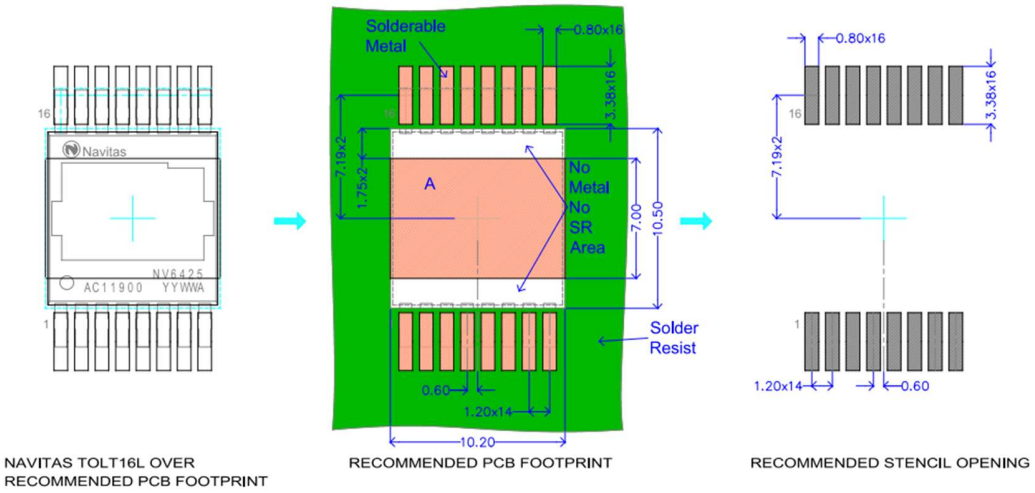


Fig. 16. Typical drain-to-source voltage stress diagram

12. PCB Layout Guidelines and PCBA SMT Solder Paste template

PCB layout is critical for thermal management, noise immunity, and proper operation of the device. The following rules should be followed carefully during the design of the PCB layout:

- Do not run power SOURCE current through SK pin!
- System-level thermal design for top-cooled packages must observe co-planarity and electrical isolation requirements when multiple power devices are cooled by the same heatsink (Cold Plate), however, TOLT employs negative offset gull-wing leads to help achieve thermal pad co-planarity across multiple devices. Also, while the majority of heat is transferred through the top-side thermal pad, placing a Cu Plane below the package (shown below) also transfers heat to the board.

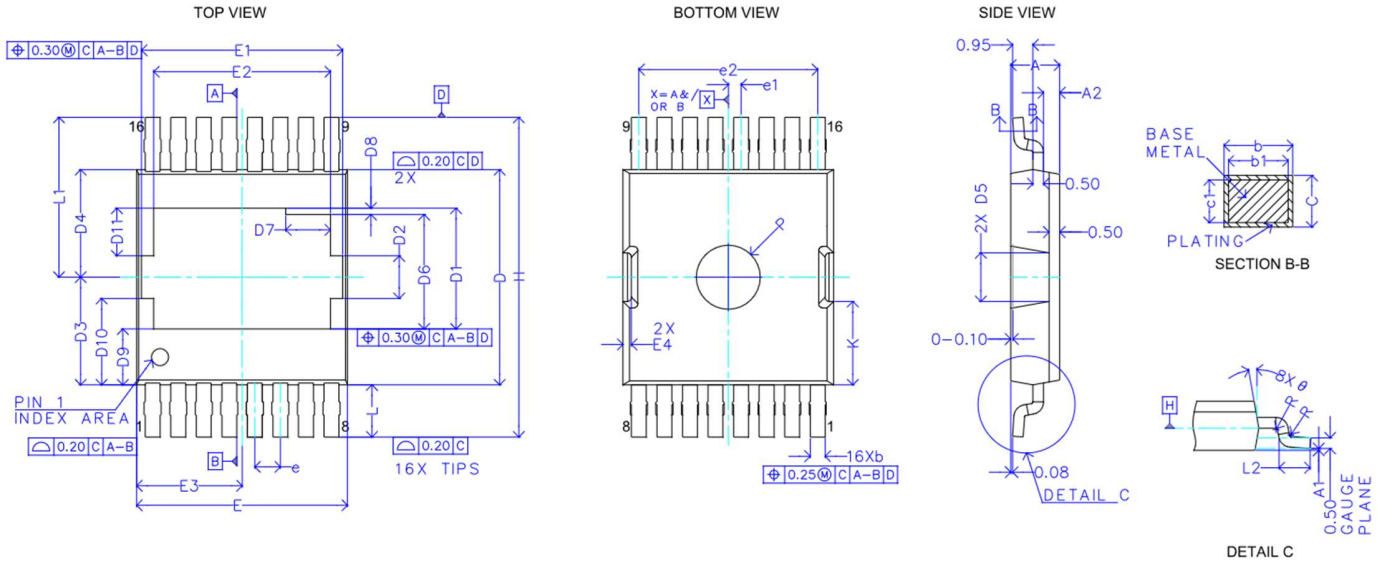


NAVITAS TOLT16L OVER RECOMMENDED PCB FOOTPRINT

RECOMMENDED PCB FOOTPRINT

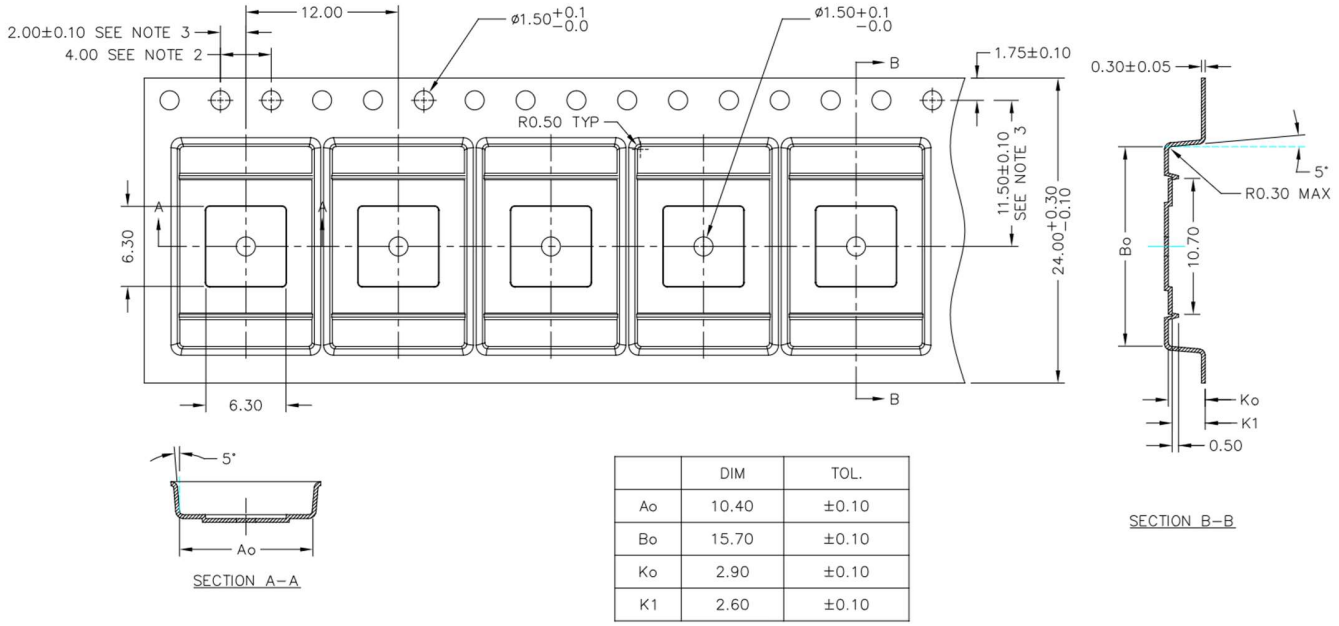
RECOMMENDED STENCIL OPENING

13. Package Outline Dimensions:

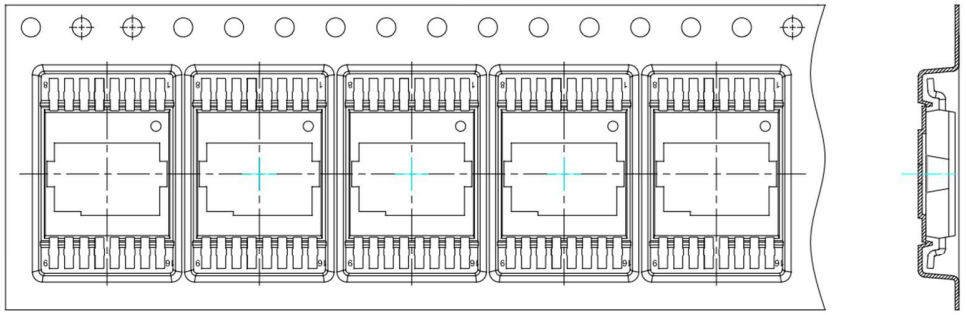


SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A	2.25	2.35	E	9.70	10.10
A1 (+)	0.01	0.11	E1	9.26	9.66
A2	0.56	0.96	E2	8.10	8.50
b	0.60	0.85	E3	4.75	5.15
b1	0.60	0.80	E4	0.20	0.60
c	0.45	0.65	e	1.20 BSC	
c1	0.45	0.60	e1	0.60 BSC	
D	10.00	10.30	e2	8.40 BSC	
D1	5.47	5.87	H	14.80	15.20
D2	1.80	2.20	K	3.71	4.11
D3	4.85	5.25	L	2.25	2.65
D4	5.00	5.13	L1	7.30	7.70
D5	2.08	2.48	L2	1.30	1.70
D6	5.17	5.57	R	0.07	-
D7	1.80	2.20	P	2.90	3.10
D8	0.10	0.50	θ	4°	10°
D9	2.42	2.82			
D10	3.85	4.25			
D11	2.04	2.44			

14. TnR Drawing



	DIM	TOL.
Ao	10.40	±0.10
Bo	15.70	±0.10
Ko	2.90	±0.10
K1	2.60	±0.10



Reel Quantity		Pin 1 Orientation
Reel Size	Unit qty in reel	2 1 Pin 1 on quadrant 1 3 4
7 "	450 units	
13 "	1500 units	

15. Ordering Information

Part Number	Qualification	Package	MSL Rating	TnR Sizes/Qtys
NV6066	JEDEC	TOLT-16L Top-cooled SMD	3	Standard (13” dia) Qty2,000
NV6066-RA				Mini-Reel (7” dia) Qty450

16. Revision History

Date	Status	Notes
Nov 24th, 2025	Initial Release	• Preliminary Datasheet
Dec 18th, 2025	Preliminary	• Data and graphs added
Jan 20th, 2026	Preliminary	• Data and graphs added

Additional Information

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