GaNSense™ HFQR Controller

1. Features

GaNSense™ Power FET
- Loss-less current sensing
- Low 520 mΩ power FET
- Zero reverse recovery charge
- Low output charge
- 800 V Transient Voltage Rating
- 700 V Continuous Voltage Rating

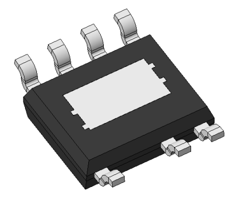
High Frequency QR Controller
- Wide VDD range up to 77V
- QR valley switching and optional CCM operating modes
- High frequency operation up to 225kHz
- High voltage start-up
- Frequency hopping for low EMI
- OVP, UVP, OTP, CSSP, SSSP protection functions
- LPS function
- Ultra-low standby current consumption (<20mW)

Small, low-profile SMT ESOP 7
- ESOP footprint, 1.27 mm profile
- Minimized package inductance
- Large cooling pad

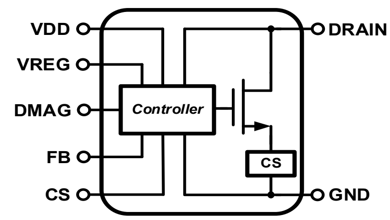
High Power Density
- > 1W/cc achievable power density
- Small transformer size
- Low component count

Sustainability
- RoHS, Pb-free, REACH-compliant
- Up to 40% energy savings vs Si solutions
- System level 4kg CO_2 Carbon Footprint reduction

Product Reliability
- 20-year limited product warranty (see Section 14 for details)



ESOP 7



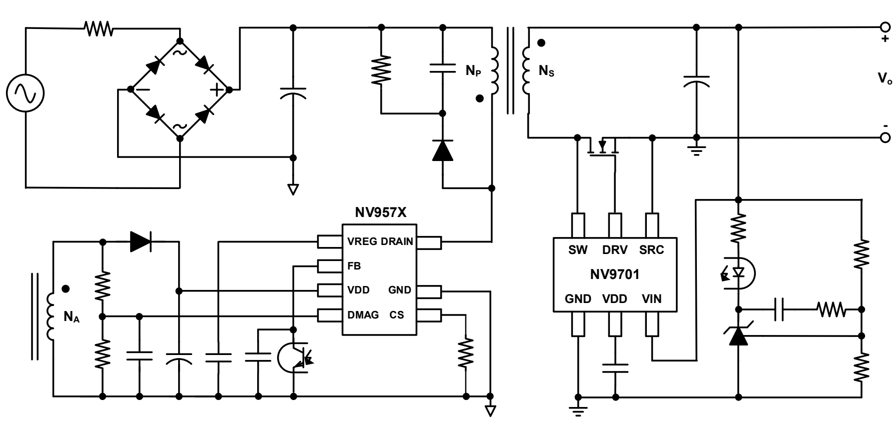
Simplified schematic

2. Topologies / Applications
- High efficiency AC-DC power adapters
- USB PD/QC battery charger
- Mobile chargers, adapters, aux power

3. Description

This GaNSense™ HFQR/CCM controller integrates a high performance eMode GaNSense Power FET together with an Flyback controller to achieve unprecedented high-frequency and high-efficiency operation for smallest size mobile charger and adapter solutions. The GaNSense Power FET includes loss-less current sensing, ultra-low gate charge, low output charge,700V continuous and 800V transient voltage ratings to provide excellent performance and robustness. The HFQR Flyback controller enables high frequency operation, wide VDD range, high-voltage start-up, and multi-mode operation. The Flyback controller also includes abnormal component short-circuit, over-temperature and LPS protection features to increase system robustness, while ultra-low standby current consumption increases light, tiny & no-load efficiency. Low-profile, low-inductance, and small footprint SMT ESOP 7 packaging enables designers to achieve simple, quick and reliable solutions. Navitas' GaN IC technology enables high frequencies, high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

4. Typical Application Circuit



HFQR Flyback

5.Table of Contents

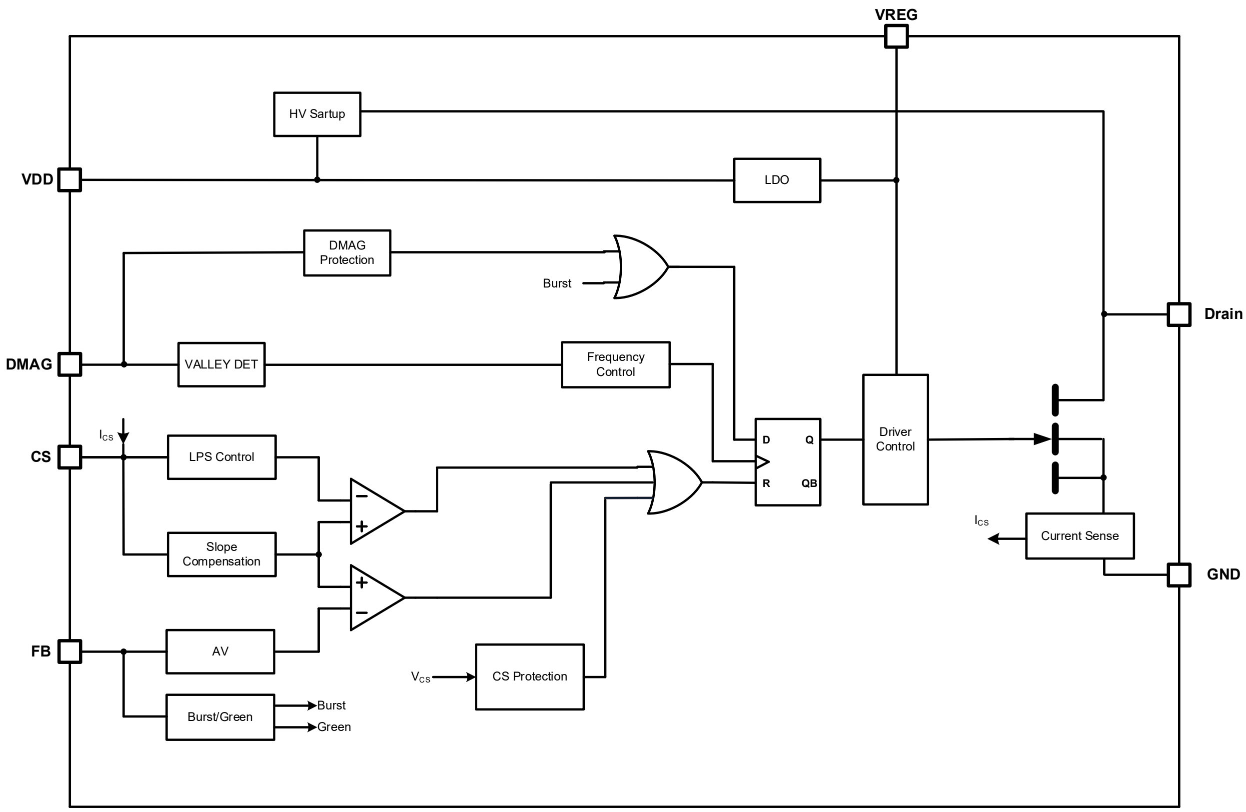
6.Ordering Information

Part Number	Maximum Frequency	Function	Protection Mode	$R_{DS(ON)}$	Operating Temperature Range	Package	Packing Method
NV9574S1P1	129kHz/100kHz	PL+CC OLP	AR	520mΩ	-40°C to +125°C	ESOP 7	4,000 13’’ Tape & Reel
NV9574S2P1	225kHz/164kHz	PL+CC OLP	AR				
NV9574S121	129kHz/100kHz	CCM PL+CC, OLP	AR				

*PL=Power Limit, CC=Constant Current

*Those protection functions not mentioned in **Protection Mode** column, they are all AR (auto restart) mode.

7. Internal Functional Block Diagram



8. Specifications

8.1. Absolute Maximum Ratings[1]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
$V_{DS(CONT)}$	GaN Power FET Continuous Drain-to-Source Voltage		-7	700	V
$V_{DS(TRAN)}$	GaN Power FET Transient Drain-to-Source Voltage[2]		-	800	V
V_{VDD}	VDD DC Supply Voltage		-0.3	80	V
V_{CS}	CS Pin Input Voltage		-0.3	6	V
V_{FB}	FB Pin Input Voltage		-0.3	6	V
V_{DMAG}	DMAG Pin Input Voltage		-0.3	6	V
V_{REG}	VREG Pin Output Voltage		-0.3	7.5	V
I_D	GaN Power FET Continuous Drain Current (@ T_C = 100ºC)		-	3	A
I_D PULSE	GaN Power FET Pulsed Drain Current (10 µs @ T_J = 25ºC)		-	6	A
θ_{JA}	Thermal Resistance (Junction-to-Ambient) [3]		-	48.29	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case) [3]		-	2.32	°C/W
T_J	Operating Junction Temperature		-40	150	°C
T_{STG}	Storage Temperature Range		-40	150	°C
T_L	Lead Temperature (Soldering) 10 Seconds		-	260	°C
ESD	Electrostatic Discharge Capability	Human Body Mode, ANSI/ESDA/JEDEC JS-001-2017	-	2.0	kV
		Charge Device Mode, ANSI/ESDA/JEDEC JS-001-2018	-	2.0	kV

Note (1): Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

Note (2): $V_{DS\,(TRAN)}$ rating allows for surge ratings during non-repetitive events that are <100us (for example start-up, line interruption). $V_{DS\,(TRAN)}$ rating allows for repetitive events that are <400ns, with 80% derating required (for example repetitive leakage inductance spikes). Refer to Section "GaN Power FET Drain-to-Source Voltage Considerations" for detailed recommended design guidelines.

Note (3): Measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

8.2. Recommended Operating Conditions[4]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Navitas does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{VDD}	VDD Pin Supply Voltage	-0.3		75	V
V_{CS}	CS Pin Supply Voltage	-0.3		5.5	V
V_{FB}	FB Pin Supply Voltage	-0.3		5.5	V
V_{DMAG}	DMAG Pin Supply Voltage	-0.3		5.5	V
V_{REG}	VREG Pin Output Voltage	-0.3		7	V

Note (4): Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied, exposure to absolute maximum rated conditions of extended periods may affect device reliability. All voltage values are with respect to the normal operation ambient temperature range is from -40°C to +125°C unless otherwise noted.

8.3. Electrical Specifications

V_{DD} (Typ.) = 12V, T_A = -40°C to 125°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
HV Startup Section						
I_{HV}	HV Startup Current Drawn from Drain Pin	V_{DRAIN}=50 V, V_{DD}=0 V	2		20	mA
I_{HV_LC}	HV Startup Leakage Current Drawn from Drain Pin	V_{DRAIN}=700 V, V_{DD}=V_{DD_UVLO}+1V			3	µA
VDD Section						
V_{DD_ON}	V_{DD} Turn-On Threshold Voltage	V_{DD} Rising	12.5	13.5	14.5	V
V_{DD_UVLO}	V_{DD} UVLO Threshold Voltage		6.2	6.5	6.8	V
V_{DD_DLCH} (5)	V_{DD} Threshold for Latch Release		1.2	1.8	2.2	V
I_{DD_ST}	Startup Current		0.5	2	5	µA
I_{DD_OP}	Operating Supply Current	No DRV Switching	0.60	0.75	0.90	mA
I_{DD_DPGN}	Operating Supply Current in Deep Green-Mode		300	375	450	µA
t_{D_DPGN}	Debounce Time to Enter Deep Green Mode		380	480	580	µs
V_{DD_OVP}	V_{DD} Over-Voltage-Protection Threshold		77	78.5		V
t_{D_UVLO} (5)	UVLO De-bounce Time			10		µs
$t_{D\_VDD\_OVP}$ (5)	V_{DD} Over-Voltage-Protection De-bounce Time			15		µs
t_{VDD_LAR}	Long Auto-Restart Mode Time	Trim Option	2.08	2.64	3.20	s
VREG Section						
V_{REG}	VREG output voltage		6.15	6.4	6.65	V
V_{REG_5mA}	VREG with 5mA Load Current	I_{OUT} = 5mA	6.05	6.4	6.65	V
Oscillator Section						
$f_{S\_BNK\_MAX\_LL}$	Maximum Blanking Frequency at Low Line Input Voltage	129kHz/100kHz	121	129	137	kHz
		225kHz/164kHz	202.5	225	247.5	kHz
$f_{S\_BNK\_MAX\_HL}$	Maximum Blanking Frequency at High Line Input Voltage	129kHz/100kHz	93	100	107	kHz
		225kHz/164kHz	147.2	164	180	kHz
$f_{S\_BNK\_MAX\_CCM}$	Maximum Blanking Frequency in CCM	129kHz/100kHz	93	100	107	kHz
f_{S_TMO}	Minimum Time-Out PWM Frequency		23	25	27	kHz
t_{ON_MAX}	Maximum PWM ON Time	129kHz/100kHz	16.6	18	19.4	µs
		225kHz/164kHz	9.5	10.5	11.5	µs
D_{MAX}	Maximum Duty Cycle		72	75	78	%
m_{slp} (5)	Slope Compensation			60		mv/µs
ΔV_{JIT} (5)	Current Sense Jitter Range			10		%
T_{JIT} (5)	Frequency Jitter Period			0.64		ms

Electrical Specifications (cont.)

V_{DD} (Typ.) = 12V, T_A = -40°C to 125°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
Feedback Section						
V_{FB_OPEN}	FB Open Voltage		4.7	5.2		V
Z_{FB}	FB Pull Up Resistor		36	42	48	kΩ
V_{FB_OLP}	FB Threshold for OLP		3.4	3.5	3.6	V
T_{D_OLP}(5)	OLP Protection De-bounce time			36		ms
A_{V_HV} (5)	FB Voltage Attenuation Factor at High Output Voltage	129kHz/100kHz (V_{DMAG} > 1.75V)		0.225		V/V
A_{V_LV} (5)	FB Voltage Attenuation Factor at Low Output Voltage	129kHz/100kHz (V_{DMAG}< 1.6V)		0.200		V/V
A_V (5)	FB Voltage Attenuation Factor	225kHz/164kHz		0.175		V/V
$V_{FB\_BST\_ENT}$	FB Threshold for Burst Mode Entry		0.50	0.55	0.60	V
$V_{FB\_BST\_EXT}$	FB Threshold for Burst Mode Exit		0.55	0.60	0.65	V
$V_{FB\_BNK\_STR}$	Frequency Foldback Start Point	129kHz/100kHz	2.240	2.300	2.380	V
$V_{FB\_BNK\_STR\_L}$	Frequency Foldback Start Point at Low Line Input Voltage	225kHz/164kHz	2.592	2.692	2.792	V
$V_{FB\_BNK\_STR\_H}$	Frequency Foldback Start Point at High Line Input Voltage	225kHz/164kHz	3.058	3.158	3.258	V
$V_{FB\_BNK\_END\_L}$	Frequency Foldback End Point at Low Line Input Voltage	129kHz/100kHz	1.340	1.394	1.480	V
		225kHz/164kHz	1.054	1.154	1.254	V
$V_{FB\_BNK\_END\_H}$	Frequency Foldback End Point at High Line Input Voltage	129kHz/100kHz	1.390	1.456	1.530	V
		225kHz/164kHz	1.051	1.151	1.251	V
$V_{FB\_CSMIN\_H}$(5)	V_{CS_MIN} Foldback High Threshold Voltage	225kHz/164kHz	1.450	1.500	1.550	V
$V_{FB\_CSMIN\_L}$(5)	V_{CS_MIN} Foldback Low Threshold Voltage	225kHz/164kHz	0.725	0.750	0.775	V

Electrical Specifications (cont.)

V_{DD} (Typ.) = 12V, T_A = -40°C to 125°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DMAG Section						
I_{DMAG_MAX}	Maximum Guaranteed Operating Current Flow Out of DMAG Pin		1.94			mA
I_{DMAG_BRI}	Current Threshold for Brown-In		0.432	0.480	0.528	mA
N_{BRI}	Debounce Cycle for Brown-In			4		Cycle
I_{DMAG_BRO}	Current Threshold for Brown-Out		0.324	0.360	0.396	mA
t_{D_BRO}	Debounce Cycle for Brown-Out		14.5	16.5	18.5	ms
I_{DMAG_HL}	Current Threshold for High Line		1.008	1.120	1.232	mA
N_{HL_ENT}	Debounce Cycle for High Line Entry			4		Cycle
I_{DMAG_LL}	Current Threshold for Low Line		0.936	1.040	1.144	mA
$t_{D\text{-}LL\_ENT}$	Debounce Cycle for Low Line Entry		14.5	16.5	18.5	ms
$t_{DMAG\_BNK\_L}$	DMAG Sampling Blanking Time	(V_{FB} < 1.5V)	0.85	1.00	1.15	µs
$t_{DMAG\_BNK\_M}$	DMAG Sampling Blanking Time	(V_{FB} > 1.6V)	1.28	1.50	1.73	µs
V_{DMAG_HV}	V_{DMAG} Threshold for High Output		1.65	1.75	1.85	V
$V_{DMAG\_LV\_HYS}$ (5)	V_{DMAG} Hysteresis Threshold for Low Output			0.15		V
V_{DMAG_UVP}	V_{DMAG} Under-Voltage-Protection Threshold		0.390	0.425	0.460	V
N_{DMAG_UVP} (5)	Debounce Cycle for V_{DMAG_UVP}			2		Cycle
$t_{VDMAG\_UVP\_BNK}$	V_{DMAG_UVP} Blanking Time during Start-up		25	32	36	ms
V_{DMAG_OVP}	V_{DMAG} Over-Voltage-Protection Threshold		3.45	3.55	3.65	V
N_{DMAG_OVP} (5)	Debounce Cycle for V_{DMAG_OVP}			2		Cycle

Electrical Specifications (cont.)

V_{DD} (Typ.) = 12V, T_A = -40°C to 125°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
Current Sense Section						
$Gain_{CS}$	Current Sense Ratio I_{DRAIN}/I_{CS}	T_A =25°C	1095	1180	1265	A/A
V_{CS_LIM}	Maximum Current Sense Limit		0.620	0.650	0.680	V
$V_{CS\_MIN\_H}$	Minimum Current Sense Limit at High Output Voltage		0.190	0.225	0.260	V
$V_{CS\_MIN\_L}$	Minimum Current Sense Limit at Low Output Voltage		0.140	0.175	0.210	V
$V_{CS\_MIN\_FB\_STR\_LL\_H}$	Feedback of V_{CS_MIN} Foldback Start Point at Low Line and High Output Voltage	225kHz/164kHz	0.380	0.425	0.470	V
$V_{CS\_MIN\_FB\_STR\_LL\_L}$	Feedback of V_{CS_MIN} Foldback Start Point at Low Line and Low Output Voltage	225kHz/164kHz	0.330	0.375	0.420	V
$V_{CS\_MIN\_FB\_STR\_HL\_H}$	Feedback of V_{CS_MIN} Foldback Start Point at High Line and High Output Voltage	225kHz/164kHz	0.480	0.525	0.570	V
$V_{CS\_MIN\_FB\_STR\_HL\_L}$	Feedback of V_{CS_MIN} Foldback Start Point at High Line and Low Output Voltage	225kHz/164kHz	0.430	0.475	0.510	V
t_{LEB}	Leading Edge Blanking Time		220	295	370	ns
t_{PD}	Propagation Delay			30	45	ns
V_{CSSP}	CS Threshold for CS Short Circuit Protection		0.095	0.125	0.155	V
N_{CS_CSSP} (5)	Debounce Cycle for CSSP Protection Trigger			2		Cycle
V_{CS_SSSP}	CS Threshold for SSSP		0.95	1.00	1.05	V
N_{CS_SSSP} (5)	Debounce Cycle for SSSP Protection Trigger			2		Cycle
t_{D_SSSP}	Debounce Time for SSSP Protection Trigger		90	125	200	ns

Electrical Specifications (cont.)

V_{DD} (Typ.) = 12V, T_A = -40°C to 125°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
Over-Temperature Protection Section						
T_{OTP} (5)	Over-Temperature-Protection Threshold		125	140		°C
ΔT_{OTP} (5)	Over-Temperature-Protection Hysteresis			20		°C
GaN Power FET Section						
Typical conditions: V_{DS} = 400V, F_{SW} = 1MHz, T_{AMB} = 25°C, I_D = 1.5 A, unless otherwise specified						
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 700V, PWM off		0.2	25	μA
$R_{DS(ON)}$	Drain-Source Resistance	PWM on, I_D = 1.5 A		520	728	mΩ
V_{SD}	Source-Drain Reverse Voltage	V_{PWM} = 0 V, I_{SD} = 1.5 A		3.5	5	V
Q_{OSS}	Output Charge			6		nC
Q_{RR}	Reverse Recovery Charge			0		nC
C_{OSS}	Output Capacitance	V_{DS} = 400 V, V_{PWM} = 0 V		8		pF
$C_{O(er)}$(6)	Effective Output Capacitance, Energy Related	V_{DS} = 400 V, V_{PWM} = 0 V		10		pF
$C_{O(tr)}$(6)	Effective Output Capacitance, Time Related	V_{DS} = 400 V, V_{PWM} = 0 V		14		pF

Note (5): Guaranteed by design

Note (6): $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

Note (6): $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

8.4. Characteristic Graphs

(T_C = -40 to 125 ºC unless otherwise specified)

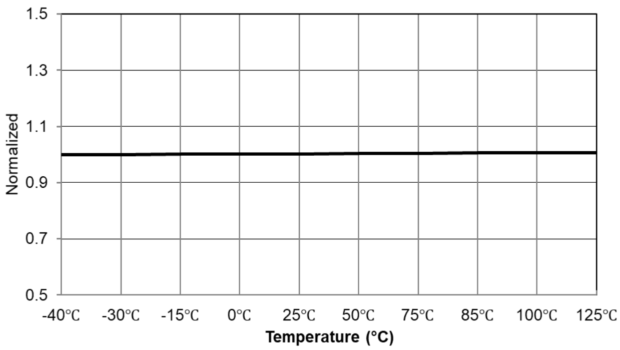


Fig. 1. V_{DD_ON}

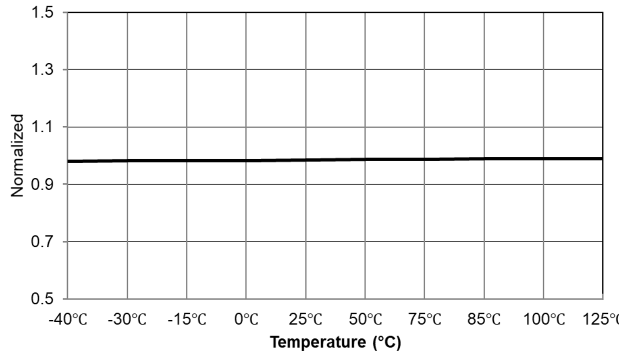


Fig. 2. V_{DD_UVLO}

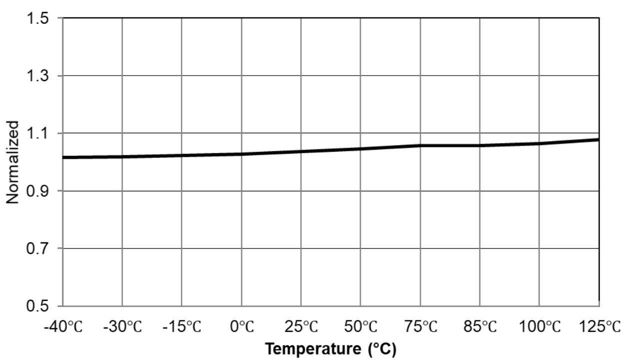


Fig. 3. V_{DD_OVP}

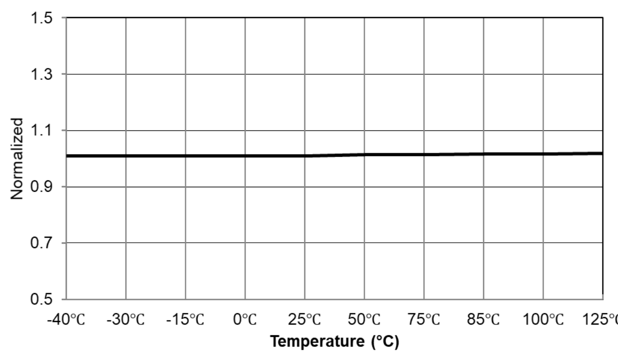


Fig. 4. f_{S_TMO}

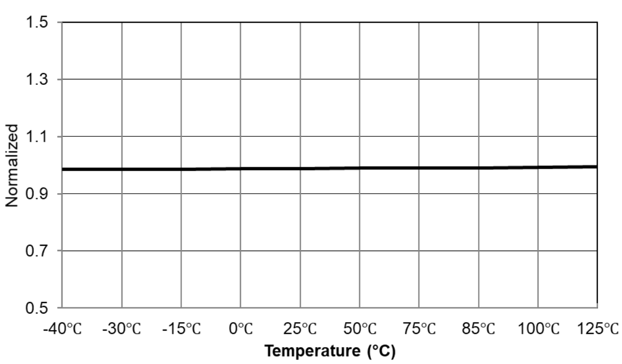


Fig. 5. $V_{FB\_BST\_ENT}$

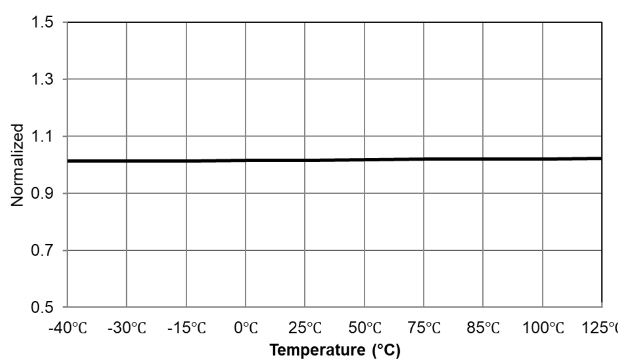


Fig. 6. $V_{FB\_BST\_EXT}$

Characteristic Graphs (cont.)

(T_C = -40 to 125 ºC unless otherwise specified)

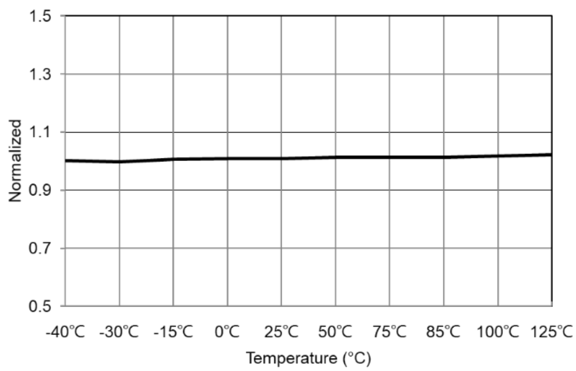


Fig. 7. I_{DMAG_BRI}

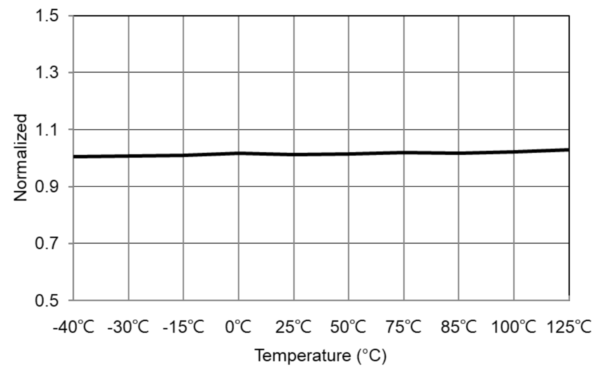


Fig. 8. I_{DMAG_BRO}

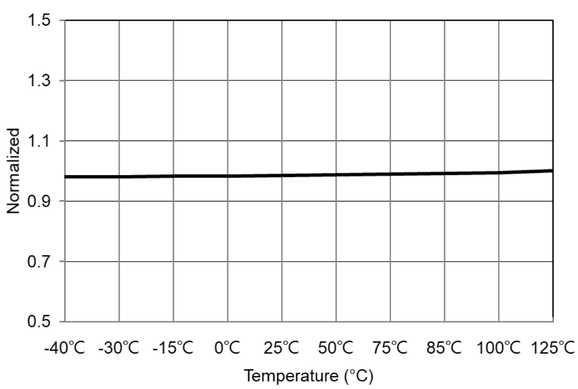


Fig. 9. V_{DMAG_UVP}

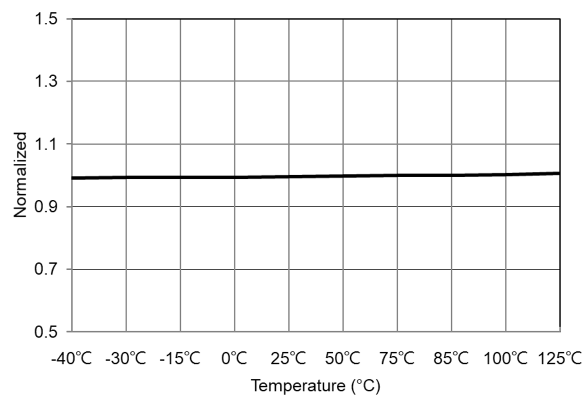


Fig. 10. V_{DMAG_OVP}

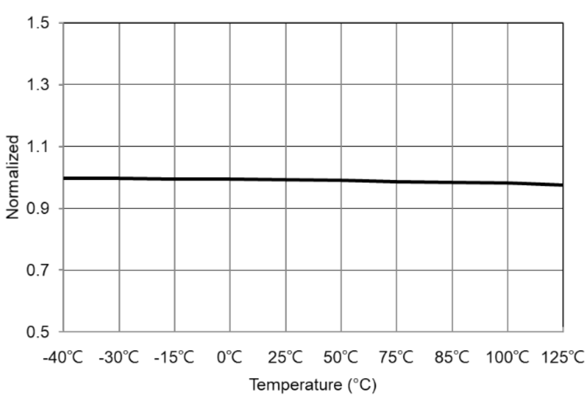


Fig. 11. $V_{CS\_LIM\_H}$

Characteristic Graphs (cont.)

(GaN Power FET, T_C = 25 ºC unless otherwise specified)

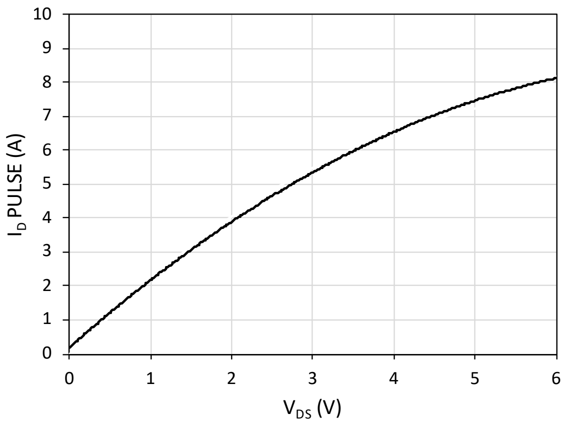


Fig. 12. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 25 °C

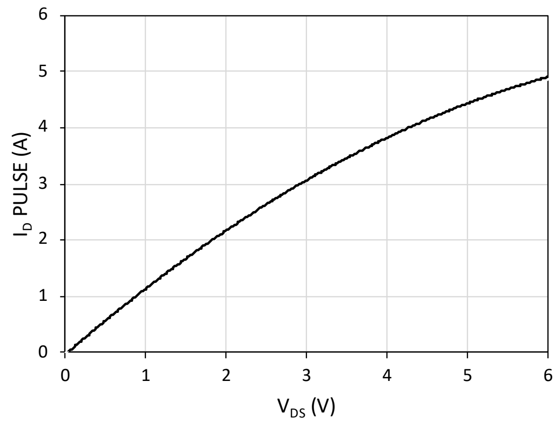


Fig. 13. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 125 °C

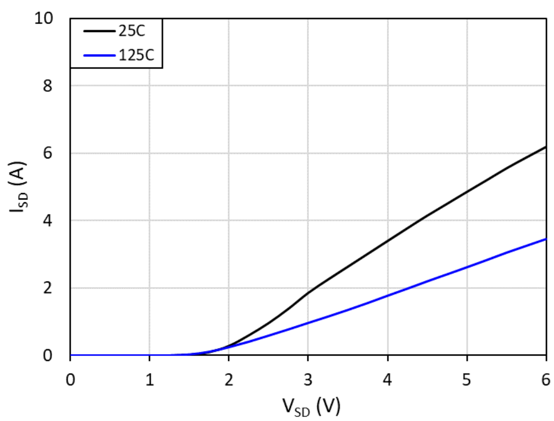


Fig.14. Source-to-drain reverse conduction voltage

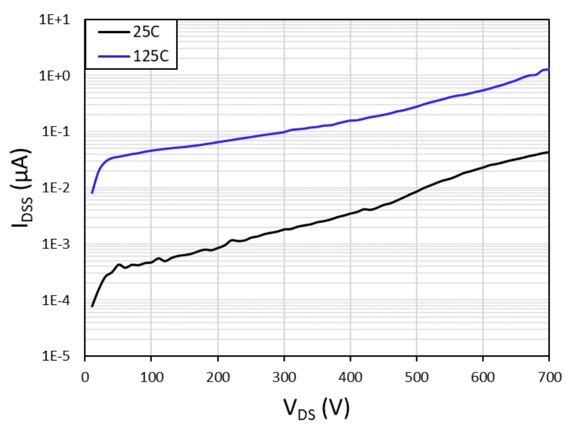


Fig.15. Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS})

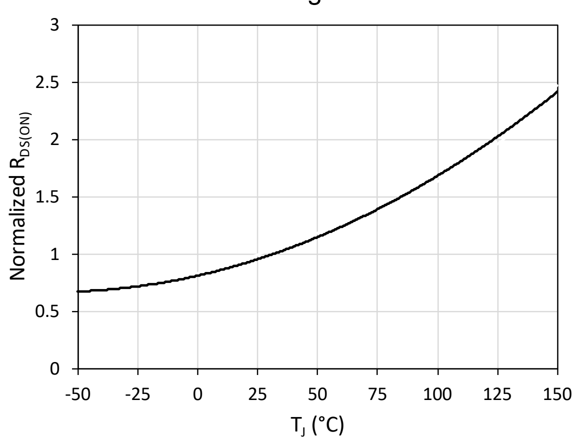


Fig.16. Normalized on-resistance ($R_{DS(ON)}$) vs. junction temperature (T_J)

Characteristic Graphs (Cont.)

(GaN Power FET, T_C = 25 ºC unless otherwise specified)

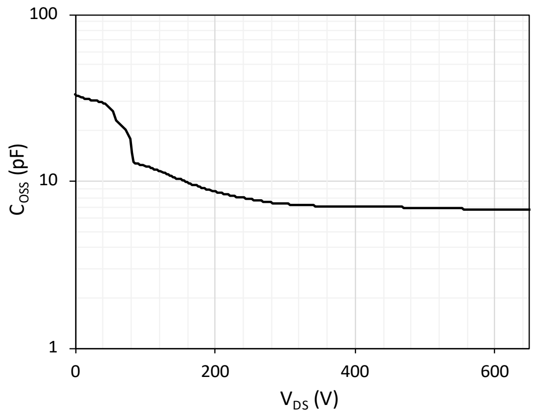


Fig.17. Output capacitance (C_{OSS}) vs. drain-to-source voltage (V_{DS})

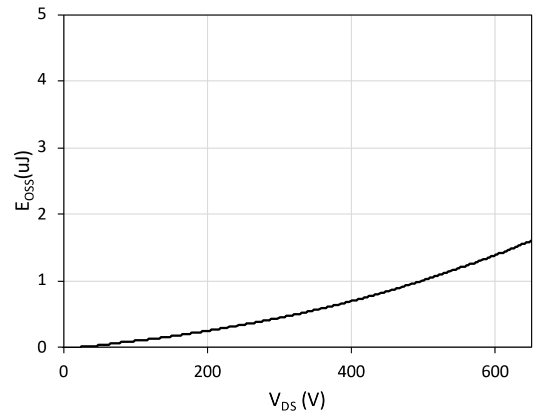


Fig.18. Energy stored in output capacitance (E_{OSS}) vs. drain-to-source voltage (V_{DS})

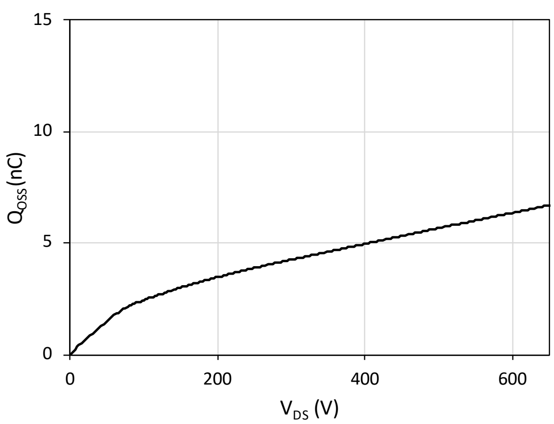


Fig.19. Charge stored in output capacitance (Q_{OSS}) vs. drain-to-source voltage (V_{DS})

9. Pin Configurations and Marking Diagram

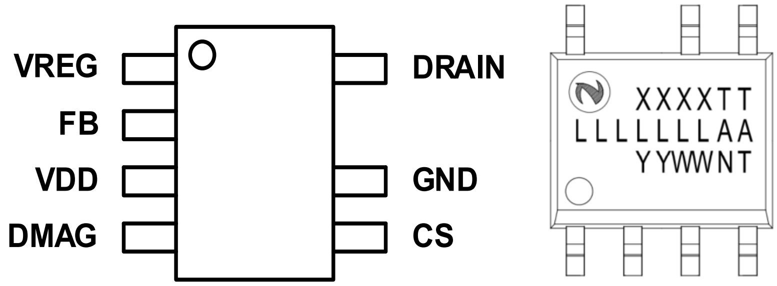


Fig. 20. Pin Configuration (Top View)

Symbol	Content
XXXX	Part Number
TT	Optional trim Code
LLLLLLL	Lot Number
AA	Die Run Code Number
YY	Year Code
WW	Week Code
N	Supplier Code
T	Optional Trim Code

Pin No.	Name	Description
1	VREG	**LDO Output**. Typically, this pin is connected to an external capacitor with recommended value = 100nF to 1uF.
2	FB	**Feedback.** Input for the internal PWM comparator.
3	VDD	**Power Supply**. IC operation current and GaN FET driving current are supplied through this pin. Typically, this pin is connected to external V_{DD} capacitor. The device starts to operate when V_{DD} exceeds V_{DD_ON}.
4	DMAG	**Demagnetization Sense**. This pin is used to detect resonant valleys for QR switching. It also detects the output voltage information, as well as the input voltage information for Brown-in & Brown-out protection.
5	CS	**Current Sense.** This pin detects the integrated GaN sense FET current cycle by cycle when connected to a current-sense resistor. There is a current ratio between Idrain and Ics
6	GND	**Ground.** Source of power FET and IC supply ground. Metal pad on bottom of package.
8	Drain	**Drain of GaN Power FET.** This pin is also connected internally to high-voltage startup circuit.

10. Functional Description

The following functional description contains additional information regarding the IC operating modes and pin functionality.

Basic Operation

NV957x family ICs are offline flyback regulator which operate in frequency limit quasi-resonant (QR) mode to reduce switching losses and EMI (electromagnetic interference). It regulates the output based on the load condition through feedback circuitry.

The QR resonant frequency is determined by the transformer primary inductance (L_P) and the primary side GaN FET effective output capacitance ($C_{oss\text{-}eff}$).

$$C_{oss-eff} = C_{oss-GaNFET} + C_{parasitic} + C_{transformer} \quad \text{(Equation 1)}$$

$$t_{resonance} = 2\pi\sqrt{L_p \times C_{oss-eff}} \quad \text{(Equation 2)}$$

In a general 957x family design, at no load or light load condition, the frequency limit f_{S_BNK} for the pulse to pulse operating frequency is f_{S_TMO}. So operating frequency is between f_{S_TMO} and $1/(1/f_{S\_TMO} + t_{resonance})$. At the medium load condition (e.g.25%~50% of full load), the frequency limit f_{S_BNK} is modulated as a function of load current such that it varies between f_{S_TMO} and $f_{S\_BNK\_MAX\_LL(HL)}$ as load varies. At the heavy load condition (e.g. 50%~100% of full load), f_{S_BNK} is fixed at $f_{S\_BNK\_MAX\_LL(HL)}$ such that the switching frequency is not higher than $f_{S\_BNK\_MAX\_LL(HL)}$ as shown in Figure 21.

NV957x family ICs also have option to operate in CCM at low line. When the device enters CCM, the maximum CCM frequency limit is $f_{S\_BNK\_MAX\_CCM}$.

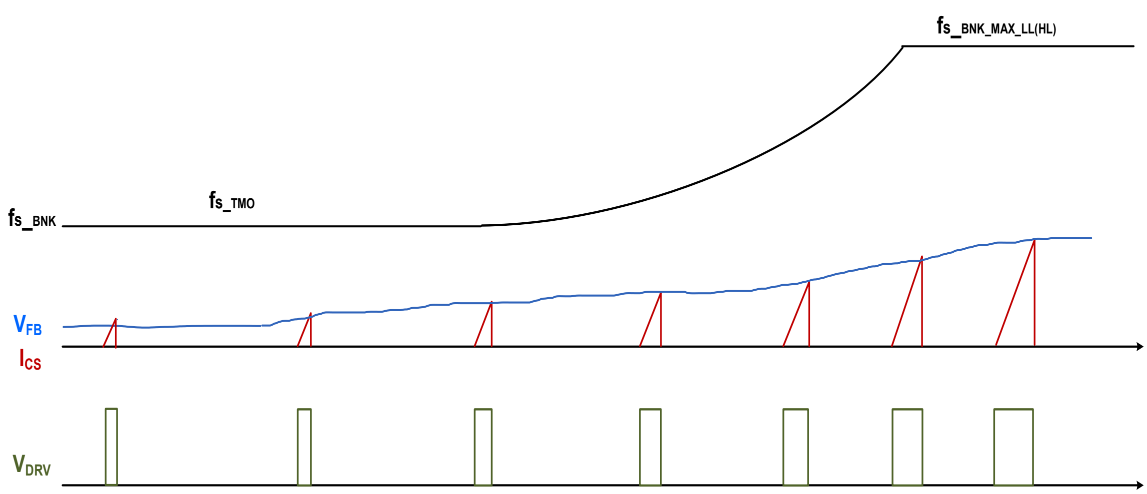


Figure 21 Frequency Fold-Back Operation

Burst Mode

As shown in Figure 22, when feedback voltage V_{FB} drops below $V_{FB\_BST\_ENT}$ at light load, the PWM output shuts off and the output voltage drops at a rate depending on the load current level. Thereafter, feedback voltage V_{FB} rises. Once V_{FB} exceeds $V_{FB\_BST\_EXT}$, NV957x family products resume switch, and the switch peak currents is limited by V_{CS_MIN}. If more power is delivered to the load than required, V_{FB} voltage will decrease. Once V_{FB} voltage is pulled below $V_{FB\_BST\_ENT}$, switching stops again. In this manner, the burst mode operation alternately enables and disables switching of the GaN FET to regulate the output and in the meanwhile reduce the switching losses.

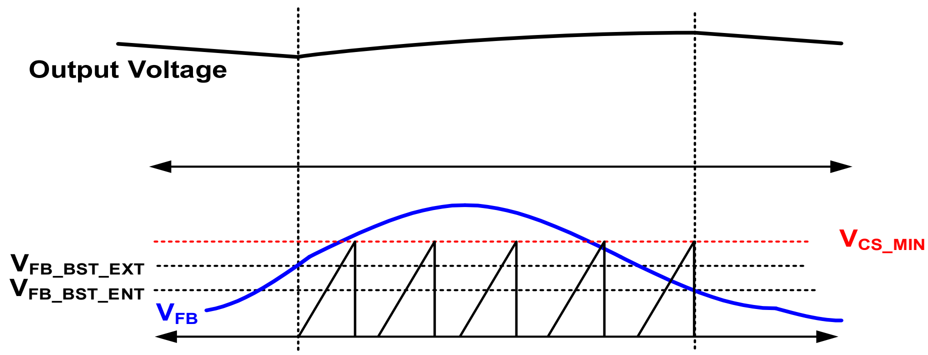


Figure 22 Burst Mode Operation

Deep Green Mode

NV957x family ICs enter the deep green mode if V_{FB} voltage stays below $V_{FB\_BST\_ENT}$ for more than t_{D_DPGN}. In the deep green mode, the IC operating current is reduced to I_{DD_DPGN} to minimize power consumption. IC resumes switching with normal operating current I_{DD_OP} once V_{FB} voltage rises above $V_{FB\_BST\_EXT}$.

Valley Detection

NV957x family valley detection is achieved by monitoring V_{DMAG} voltage, which is the divided auxiliary winding voltage by R_{DMAG1} and R_{DMAG2} as shown in Figure 23. One ceramic capacitor (C_{DMAG}) with typical value 10pF (and not bigger than 22pF) is recommended to filter out the noise if there is PCB noise coupling concern.

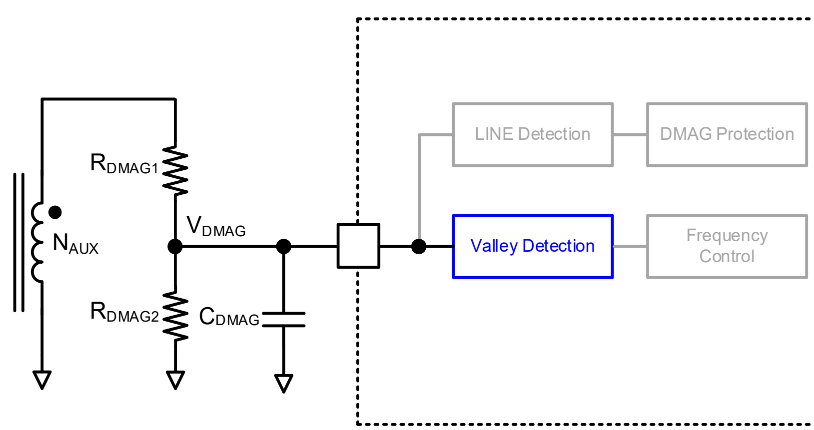


Figure 23 Valley Detection Circuit

Inherent Frequency Jitter

In flyback application, the DC ripple (ΔV_{DC}) of bulk capacitor at the low line application is larger than at the high line application as shown in Figure 24. This large DC ripple will result in switching frequency variation for a valley switched converter. The frequency variation scatters EMI noise over the nearby frequency band, allowing compliance with EMI requirement easily. Therefore, the EMI performance at the low line application is easy to comply with EMI limitation naturally. However, at the high line application, the DC ripple is relatively small and consequently the EMI performance may suffer. To maintain good EMI performance across over the universal input, a frequency jitter is implemented in the NV957x family products.

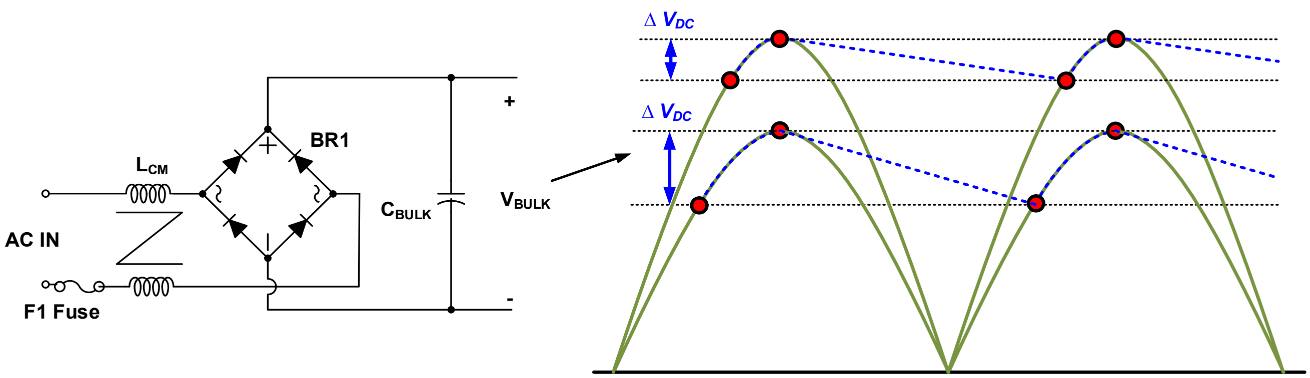


Figure 24 Inherent Frequency Jitter

Output Voltage Detection

NV957x family products detect output voltage through DMAG voltage. Figure 25 shows the DMAG voltage ($V_{DMAG-S/H}$) is sampled at the end of t_{DMAG_BNK} to avoid sampling error. The DMAG voltage is set based on the transformer turn ratio, the voltage divider resistors R_{DMAG1} & R_{DMAG2}. The ratio ($Ratio_{DMAG}$) between $V_{DMAG-S/H}$ and Vo can be defined as:

$$Ratio_{DMAG} = \frac{V_{DMAG-S/H}}{V_O} = \frac{N_A}{N_S} \times \frac{R_{DMAG2}}{R_{DMAG1} + R_{DMAG2}} \quad \text{(Equation 3)}$$

$Ratio_{DMAG}$ is required to be designed to guarantee Vo nominal operation will not hit protections, i.e., $V_{DMAG-S/H}$ will not hit either $V_{DMAG-OVP}$ or $V_{DMAG-UVP}$ described in protection section. For USB-PD/PPS application, a typical recommended $Ratio_{DMAG}$ design is 0.16.

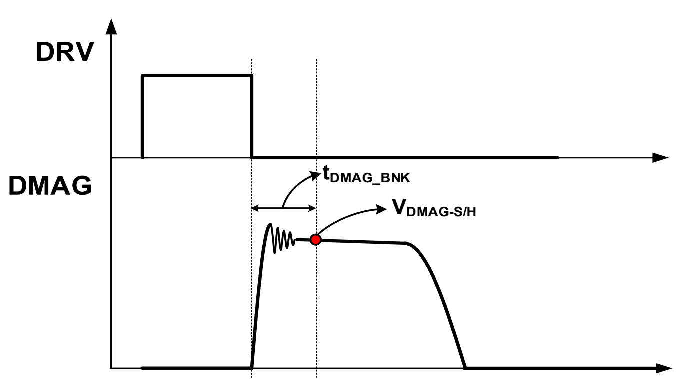


Figure 25 Output Voltage Detection

Line Voltage Detection

As illustrated in Figure 26, NV957x family products indirectly sense the line voltage through DMAG pin during GaN FET turn-on period. During the GaN FET conduction time, the line voltage detector clamps DMAG pin voltage at 0V. The auxiliary winding voltage, V_{AUX}, is proportional to the input bulk capacitor voltage, V_{BLK}. So current I_{DMAG} flowing out of DMAG pin is expressed as:

$$I_{DMAG} = \frac{V_{BLK}}{R_{DMAG1}} \times \frac{N_A}{N_P} \quad \text{(Equation 4)}$$

I_{DMAG} current, reflecting the line voltage information, is used for the brown-in and brown-out protection.

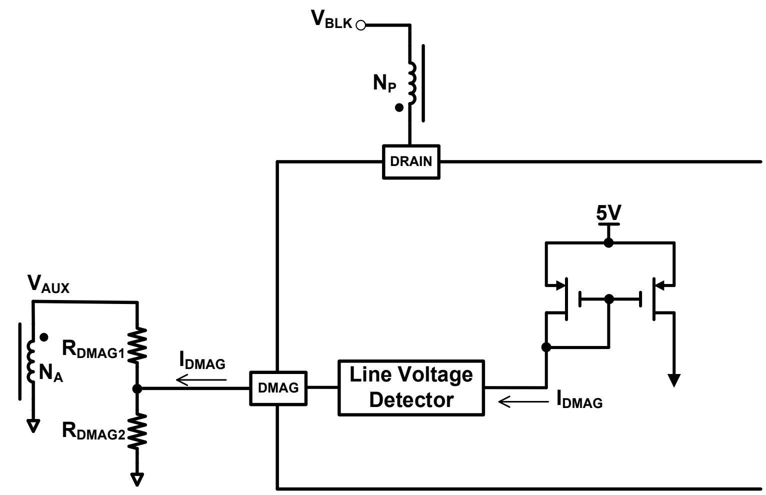


Figure 26 Line Voltage Detection Circuit

LPS Function

The NV957x family products incorporate built-in circuits to limit output power (PL) and limit output current (CC) in the event of the protocol IC becoming malfunction.

Cycle by Cycle Current Limit

Under certain operation condition, such as the startup or the overload condition, the feedback control loop can be saturated and is unable to control the primary peak current. To limit the current under such conditions, NV957x family products incorporate the cycle by cycle current limit function which forces the GaN switch turn off when CS pin voltage reaches the current limit threshold V_{CS_LIM}.

Start-up

During startup, the internal HV startup circuit is enabled, and the input voltage supplies the current, I_{HV}, to charge hold-up capacitor C_{VDD}. When V_{DD} voltage reaches V_{DD_ON}, the HV startup circuit is disabled. The IC starts PWM switching and senses DMAG signal to check the brown-in condition. If the brown-in is not detected, the IC enters the auto-restart mode. The internal startup circuit is connected to the Drain pin inside.

Protection Description

NV957x family products protection functions include VDD over-voltage protection (VDD-OVP), Brown-in/out protection, DMAG over-voltage protection (DMAG-OVP), DMAG under-voltage protection (DMAG-UVP), Overload protection (OLP), IC internal over-temperature protection (OTP) etc. All protections have auto-restart mode option. The DMAG-OVP can be configured with auto-restart or latch mode. The DMAG-UVP can be configured with auto-restart or long auto-restart mode. The protection function information is provided on page 3.

When the long auto-restart mode protection is triggered, the integrated GaN FET is turned off for a period of t_{VDD_LAR}. After t_{VDD_LAR}, if VDD rises above V_{DD_ON}, NV957x family products resume normal operation as shown in Figure 27.

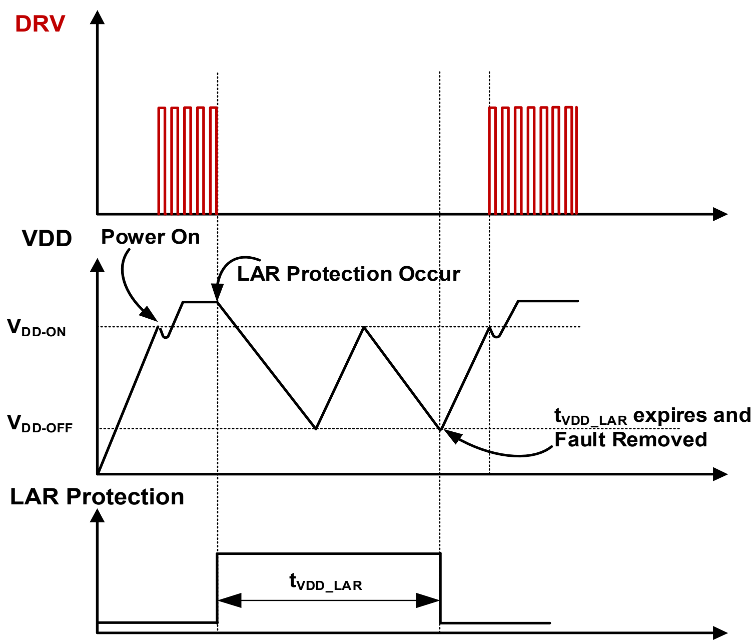


Figure 27 Auto-Restart Long AR Mode

VDD-OVP

VDD-OVP prevents IC damage from over voltage stress when abnormal system conditions occur. When VDD voltage exceeds V_{DD_OVP} for the debounce time $t_{D\_VDD\_OVP}$, the VDD-OVP protection is triggered, the device enters the auto-restart mode.

Brown-in & Brown-out

The sensed line voltage information is used for the brown-in and brown-out protection. During GaN FET conduction time, when the current, I_{DMAG}, flowing out of DMAG pin is higher than I_{DMAG_BRI} for N_{BRI} debounce cycles, the brown-in is enabled. The input bulk capacitor voltage level to enable the brown-in is given as

$$V_{BLK\_Brownin} = I_{DMAG\_BRI} \times \frac{R_{DMAG1}}{N_A/N_P} \quad \text{(Equation 5)}$$

When I_{DMAG} is lower than I_{DMAG_BRO} for longer than t_{D_BRO} , the brown-out is triggered. The input bulk capacitor voltage level to trigger the brown-out protection is given as

$$V_{BLK\_Brownout} = I_{DMAG\_BRO} \times \frac{R_{DMAG1}}{N_A/N_P} \quad \text{(Equation 6)}$$

IC Internal OTP

The internal temperature-sensing circuit disables the PWM output if the junction temperature exceeds T_{OTP}, and the IC enters protection mode.

DMAG-OVP

DMAG-OVP prevents server system damage when abnormal system conditions occur and cause DMAG voltage rising abnormally. Usually, DMAG over voltage protection is caused by not working properly feedback network (FB) or a fault condition of the DMAG voltage divider resistors. Figure 28 shows the internal circuit of DMAG-OVP. When abnormal system conditions occur and cause DMAG voltage to exceed V_{DMAG_OVP} for more than N_{DMAG_OVP} consecutive switching cycles, PWM pulses are disabled, and the IC enters the auto-restart mode or the latch mode.
For DMAG voltage divider design, R_{DMAG1} is obtained from Equation 5, and R_{DMAG2} is determined by Equation 3. The output over voltage protection level, V_{O_OVP}, can be determined by Equation 7.

$$V_{O\_OVP} = \frac{V_{DMAG_{OVP}}}{Ratio_{DMAG}} = \frac{N_S}{N_A} \times \left(1 + \frac{R_{DMAG1}}{R_{DMAG2}}\right) \times V_{DMAG_{OVP}} \qquad \text{(Equation 7)}$$

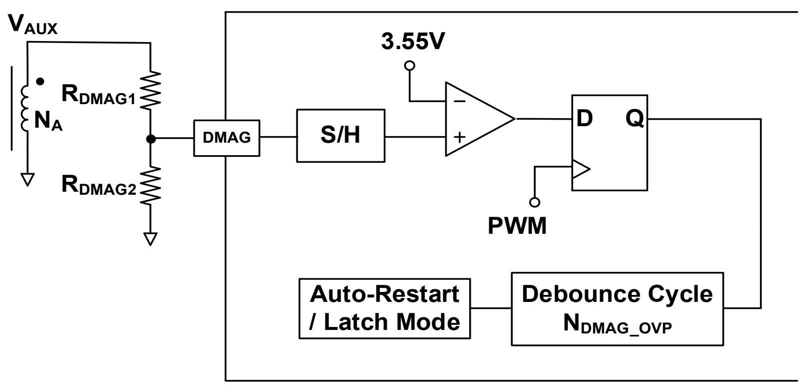


Figure 28 DMAG Over Voltage Protection Circuit

DMAG-UVP

In the event with shorted output, the output voltage will drop, and the primary peak current will increase. To prevent operation for a long time under this condition, NV957x family products incorporate the under voltage protection through DMAG pin (DMAG-UVP). Figure 29 shows the internal circuit for DMAG-UVP. When DMAG voltage is less than V_{DMAG_UVP} and longer than de-bounce cycles N_{DMAG_UVP}, DMAG UVP is triggered, and the IC enters the auto-restart mode or the long auto-restart mode.

The output under voltage protection level, V_{O_UVP}, can be determined by Equation 8.

$$V_{O\_UVP} = \frac{V_{DMAG_{UVP}}}{Ratio_{DMAG}} = \frac{N_S}{N_A} \times (1 + \frac{R_{DMAG1}}{R_{DMAG2}}) \times V_{DMAG\_UVP} \qquad \text{(Equation 8)}$$

To avoid DMAG-UVP triggering during the startup sequence, startup blanking time $t_{VDMAG\_UVP\_BNK}$ is incorporated for system power on.

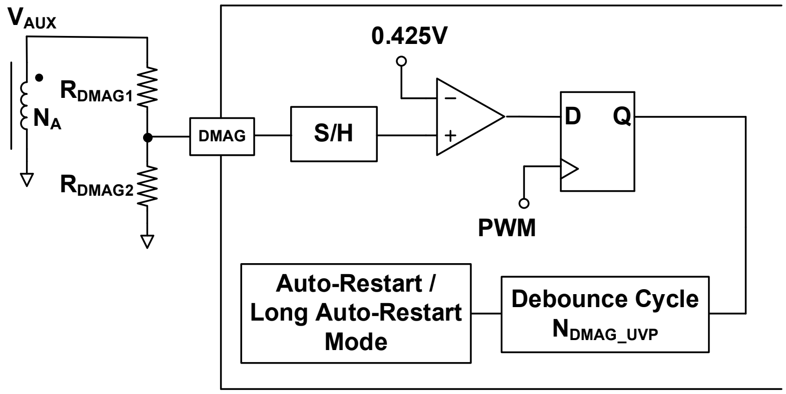


Figure 29 DMAG Under Voltage Protection Circuit

Current Sense Short Protection (CSSP)

NV957x family has CSSP function. When abnormal system conditions occur, in case after debounce time CS pin voltage is still lower than V_{CSSP}, the GaN switch turn on time will be limited to limit output power. If this status maintains consecutive N_{CS_CSSP} switching cycles, The IC enters auto-restart mode.

Secondary Side Short Protection (SSSP)

When the secondary-side rectifier is abnormally shorted, the primary-side switch current will increase dramatically within the leading-edge blanking time. To limit the switch current during such conditions, NV957x family products incorporate SSSP function which forces the GaN Switch to turn off when CS pin voltage reaches V_{CS_SSSP} after blanking time t_{D_SSSP}. If this status maintains consecutive N_{CS_SSSP} switching cycle, the IC enters auto-restart mode.

Over Load Protection (OLP)

NV957x family implements overload protection by limiting the maximum duration for operation of overload conditions. The overload timer starts counting when V_{FB} voltage reaches V_{FB_OLP}. If this time is over OLP debounce time T_{D_OLP}, OLP protection will be triggered, and device will shut down and turn to auto restart mode. If V_{FB} voltage drops to below V_{FB_OLP} before T_{D_OLP}, the overload timer will be reset.

GaN Power FET Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 30. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE}. The clamp circuit should be designed to control the magnitude of V_{SPIKE}. After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 30 as $V_{DS\text{-}OFF}$.

- For repetitive events, 80% derating should be applied from $V_{DS\ (TRAN)}$ rating (800V) to 640V max under the worst case operating conditions.
- It is recommended to design the system such that $V_{DS\text{-}OFF}$ is derated 80% from the $V_{DS(CONT)}$ (700V) max rating to 560V.
- For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the $V_{DS\text{-}OFF}$ derating guideline (560V).
- Non-repetitive events are infrequent, one-time conditions such as line surge, ESD, and lightning. No derating from the $V_{DS(TRAN)}$ rating (800V) is needed for non-repetitive V_{SPIKE} durations < 100 µs. The $V_{DS(TRAN)}$ rating (800V) allows for repetitive events that are <400ns, with 80% derating required (for example repetitive leakage inductance spikes).

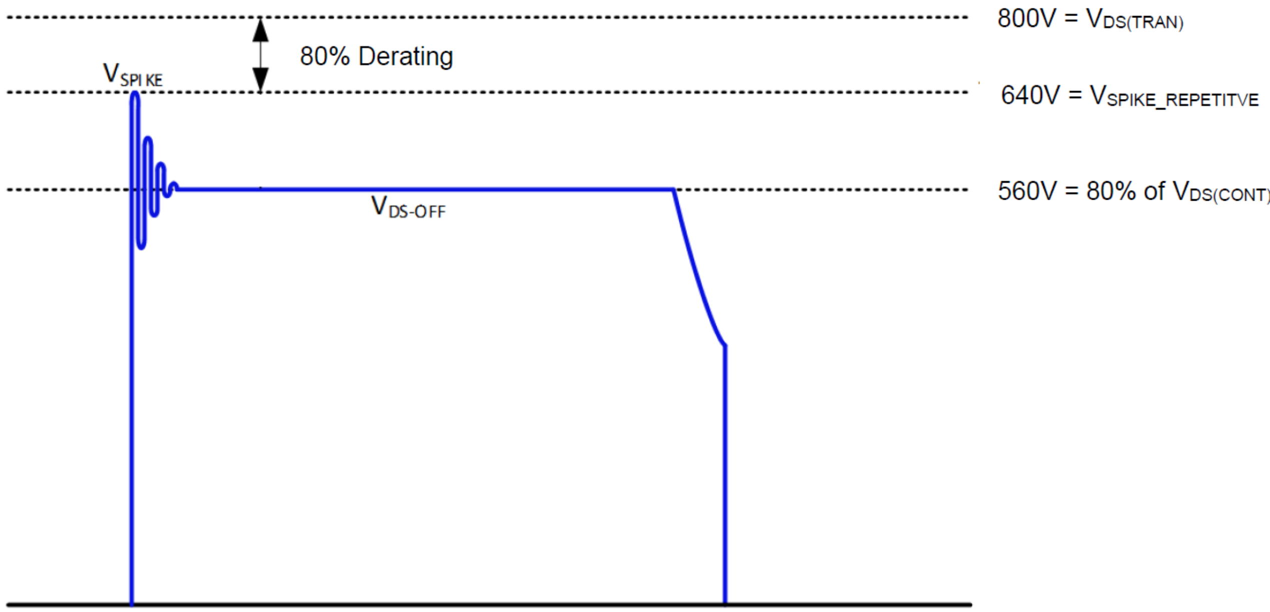
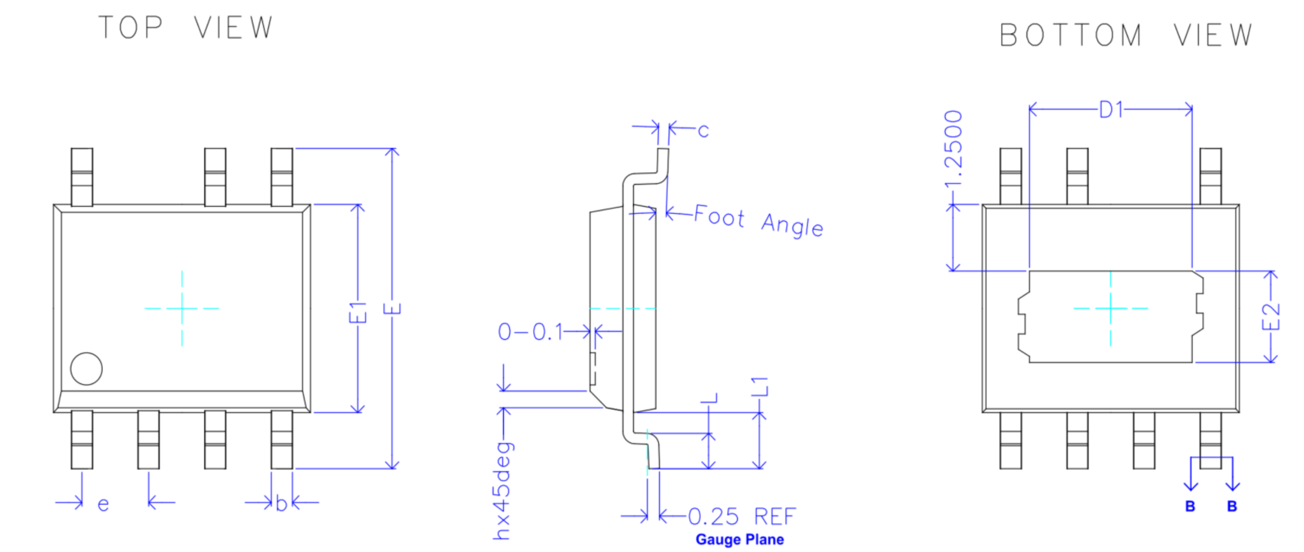
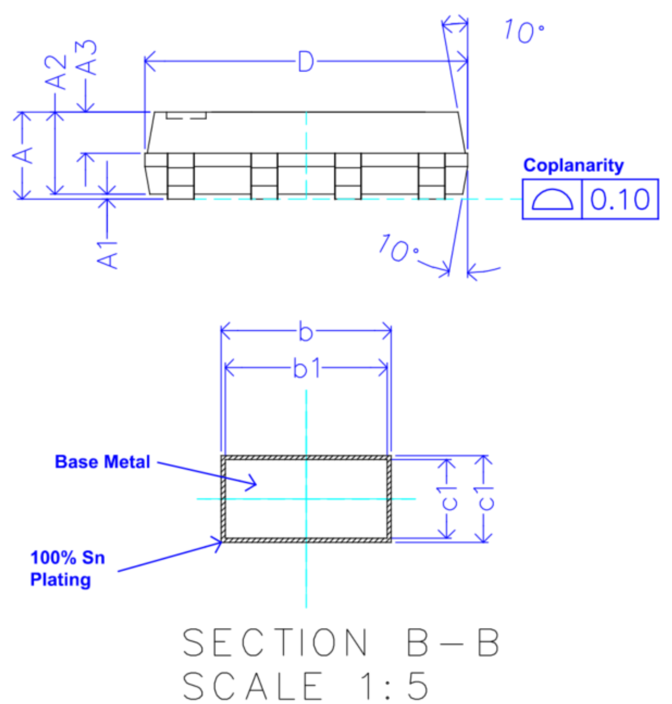


Figure 30 QR flyback drain-to-source voltage stress diagram

11. Package Outline (ESOP 7)

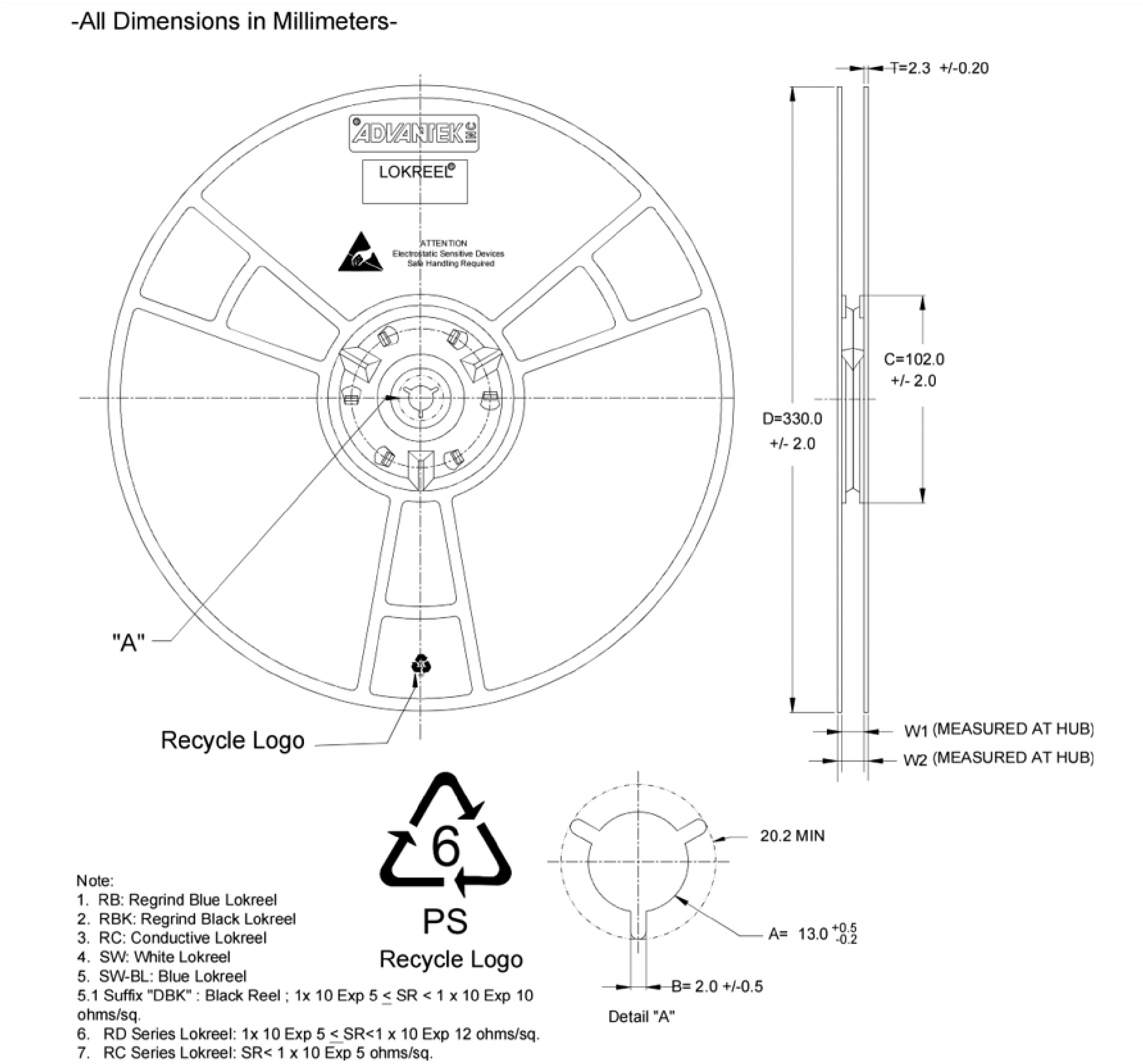




SYMBOL	MIN	NOM	MAX
A	-	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	__	0.47
b1	0.38	0.41	0.44
c	0.20	__	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25	-	0.50
L	0.50	0.60	0.80
L1		1.05 REF	
Foot angle : 0-8 degrees			
Expossed Pad Dimension: D1 : 3.10 REF E2 : 1.72 REF			

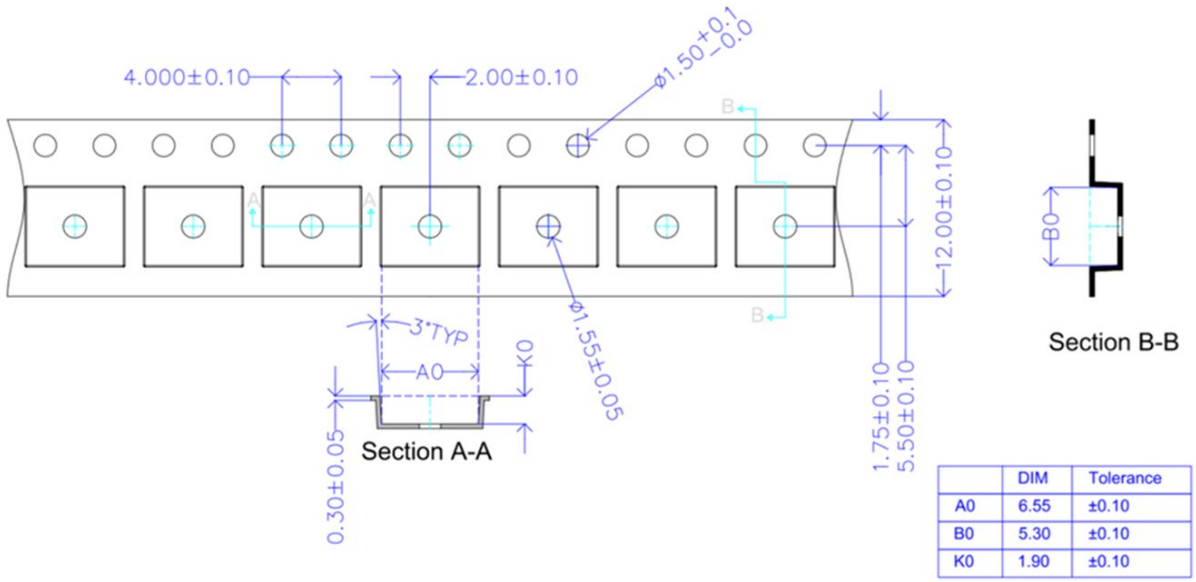
Note: Dimensions in mm

12. Tape and Reel Dimensions

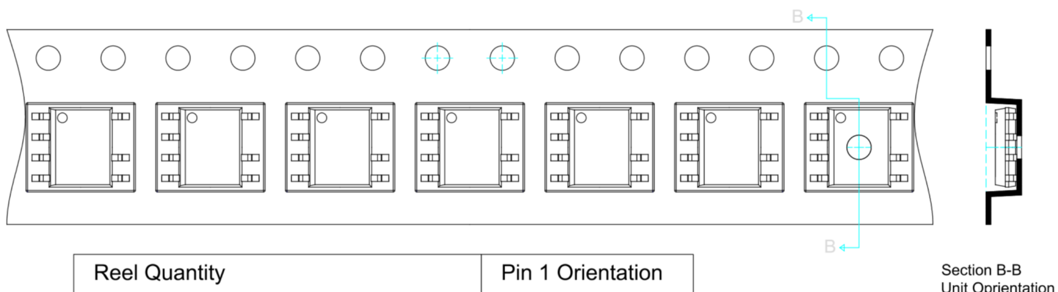


Nominal Hub Width	W1	W2 MAX
12mm	12.8mm +1.6 / -0.4	18.4mm

13. Tape and Reel Dimensions (Cont.)



	DIM	Tolerance
A0	6.55	±0.10
B0	5.30	±0.10
K0	1.90	±0.10



Reel Quantity		Pin 1 Orientation
Reel Size	Unit qty in reel	Pin 1 on quadrant 2 (2 1 / 3 4)
13 "	4000 units	

14. 20-Year Limited Product Warranty

The 20-year limited warranty applies to all packaged Navitas GaNFast Power ICs and GaNSense HFQR Controllers in mass production, subject to the terms and conditions of, Navitas' express limited product warranty, available at https://navitassemi.com/terms-conditions. The warranted specifications include only the MIN and MAX values only listed in Absolute Maximum Ratings and Electrical Characteristics sections of this datasheet. Typical (TYP) values or other specifications are not warranted.

15. Revision History

Date	Status	Notes
Sep. 20, 2024	Initial version	Included Sustainability description

Additional Information

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