IsoFast™ Half-Bridge GaN Digital Isolator

FEATURES

- **Extreme CMTI up to 200V/ns**
- **Switching Frequency up to 14MHz**
- **Minimum Pulse Width 36ns**
- **Low Pulse Width Distortion < 1.5ns**
- **Very Low Jitter <1ns**
- **Double Capacitive Isolation**
- **Peak Isolation Voltage V_{ISO} (60s) > 4kV_{RMS}**
- **DC Working Voltage V_{IORM} (40yrs) 975V**
- **2kV HBM ESD Protection**
- **Temperature Range -40°C to 125°C**
- **Output supplies Operation 5V±10%**
- **190mA pull-up / 300mA pull-down digital driver typical peak current**
- **TTL Digital Input Controls compatible with 3.3V±10%, 5V±10% and 12V±10%**
- **Input Supply Operation compatible with 8V…18V±10% (VCC) or 5V±10% (VDD)**
- **SOIC16 Narrow Body and SOIC14 Wide Body**
- **Carrier-Free Modulation**
- **Under Voltage Lockouts VDD, VDD1 and VDD2**
- **Low Quiescent-current Consumption (350µA on input supply and 300µA on each output supply)**
- **Low current consumption in disabled mode (230µA on input supply and 290µA on each output supply)**

APPLICATIONS

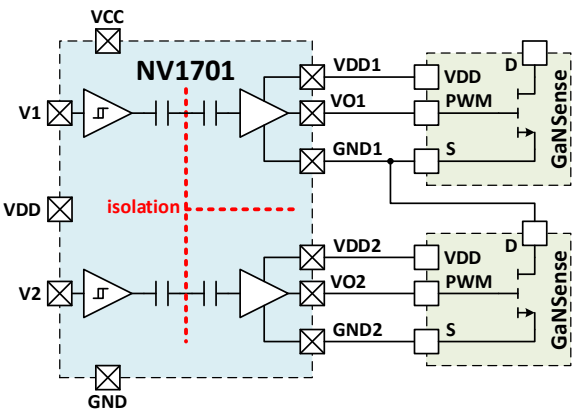
- **Single-Stage Converters**
- **DC-DC Switched Power Supplies**
- **High-Voltage Motor Control**
- **High-Voltage Inverters**

DESCRIPTION

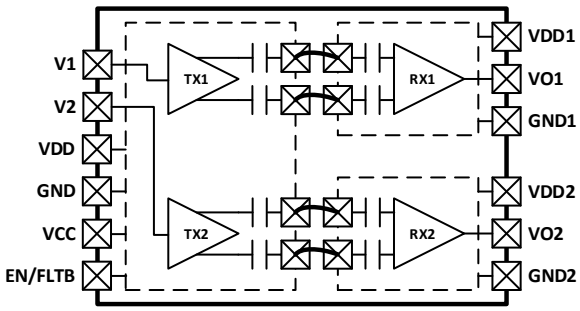
The NV1701 is a half-bridge digital isolator. This device has 2 fully isolated forward logic input and output buffers separated by Navitas' proprietary double capacitive Silicon isolation barrier. It provides galvanic isolation above 10 kV surge voltage between any input or output combination and can sustain common mode transients as large as 200V/ns. A digital signal is received through a 3-12V compatible Schmitt-triggered input buffer, translated to modulated balanced signals, transmitted across an integrated dual-layer capacitive isolation barrier before being demodulated and buffered to a digital output.

This Navitas' proprietary modulation technique is free of high frequency carrier for better EMC performances while providing a periodic refresh signal every $t_{REFRESH}$ < 340ns in case of steady state input signal. The NV1701 has been optimized for switching applications. In such cases, the power switches do not toggle while a fast transient event (dV/dt) is occurring. A "blank-and-refresh" feature is implemented in NV1701 making it robust against possible input noise induced by hard-switching events. The NV1701 is able to transmit short pulses as low as 36ns with low distortion and very low jitter, making it an ideal choice when, for example, extreme conversion ratio (i.e. very low duty cycles) are required as in DC-DC converter applications.

Isolated GaNSense Half Bridge

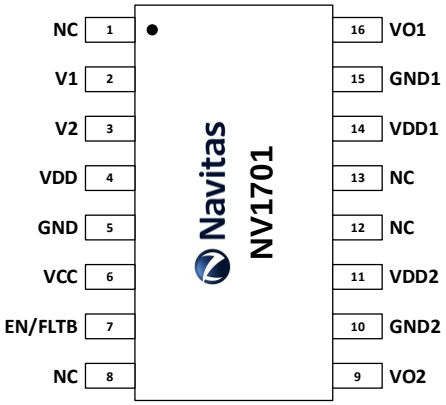


Simplified block diagram

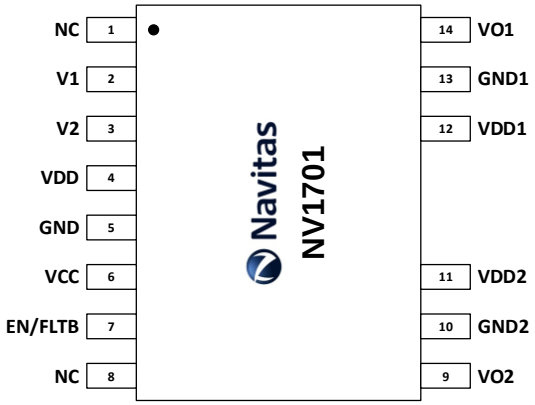


PIN DESCRIPTION

SOIC16N (Top View)



SOIC14W (Top View)



Pin Definition

PIN NUMBER		PIN NAME	FUNCTION	DESCRIPTION
NV1701N	NV1701W			
1	1	NC	NA	Do not connect.
2	2	V1	Digital Input	digital input for channel 1.
3	3	V2	Digital Input	digital input for channel 2.
4	4	VDD	Positive Supply	5V Input/Output power supply. When VCC is available, the VDD is internally generated and must be left floating (see also section “Supplies” further in this document). In this case VDD could be used for supplying external low noise circuits with maximum 1mA. If VCC is not available, VDD must be shorted to VCC and supplied with 5V voltage source.
5	5	GND	Ground	Input ground.
6	6	VCC	Positive Supply	Input power supply. Connect to 8V-18V voltage source. If not available, see pin 4.
7	7	EN/FLTB	Digital Input/Output	Enable input and Fault output. In normal operation, this pin must be driven high via pull-up resistor to VDD or VCC with R_{PU}>VCC/5mA. It has an internal pull-up to VDD with 100kΩ typical. When driven low, it unconditionally drives the VO1 and VO2 outputs low. In case of fault condition (UVLO on VDD), this pin is driven low for at least 2.5µs, with a typical 5mA current strength.
8	8	NC	NA	Do not connect.
9	9	VO2	Digital Output	Channel 2 digital output.
10	10	GND2	Ground	Output channel 2 ground.
11	11	VDD2	Positive Supply	Output channel 2 power supply. Connect to 5V voltage source.
12	NA	NC	NA	Left floating or removed for isolation between output channels.
13				
14	12	VDD1	Positive Supply	Output channel 1 power supply. Connect to 5V voltage source.
15	13	GND1	Ground	Output channel 1 ground.
16	14	VO1	Digital Output	Channel 1 digital output.

SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
VCC vs. GND	DC Supply vs. ground	-0.5	26.4	V
VDDx vs. GNDx	DC Supply vs. ground (same side)	-0.5	6	
GND vs. GND1 GND vs. GND2 GND1 vs. GND2	DC Isolation SOIC16N	-750	750	
GND vs. GND1 GND vs. GND2 GND1 vs. GND2	DC Isolation SOIC16W	-1500	1500	
Inputs vs GND	Input voltage on V1, V2 versus GND	-0.5	14	
EN/FLTB vs GND	Input voltage on EN/FLTB versus GND	-0.5	26.4	
Outputs vs GNDx	Output voltage on VOx versus GNDx (same side)	-0.5	VDDx+0.5	
Tj	Junction temperature	-40	150	°C

ESD Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{HBM}	Human Body Model robustness	-2000	2000	V
V_{CDM}	Charged Device Model robustness	-500	500	V
$I_{LATCHUP}$	Latch-up immunity	-200	200	mA

Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
VCC vs. GND	High Voltage DC Supply vs. ground	7.2	19.8	V
VDD vs. GND	DC Supply vs. ground (primary side)	4.5	5.5	V
I(VDD)	External use (output sourcing current)	0	1	mA
VDDx vs. GNDx	DC Supply vs. ground (secondary side)	4.5	5.5	V
Inputs vs. GND	Input voltage on V1, V2 versus GND	-0.3	13.2	V
EN/FLTB vs. GND	Enable input versus GND	-0.3	19.8	V
I_{OUT}	DC Output current on VOx for VDDx = 5V	-50	50	mA
f_{SW}	Switching Frequency	0	14	MHz
T_A	Ambient Temperature	-40	125	°C

Insulation Characteristics

PARAMETER	DESCRIPTION	SOIC16N	SOIC14W	UNIT
CLR External clearance	Shortest distance through air	>4	>8	mm
CRP External creepage	Shortest distance through the package	>4	>8	
DTI Isolation distance	Minimum internal isolation gap	>20	>20	µm
C_{IB}	Isolation barrier capacitance (per channel)	200	200	fF
V_{ISO}	Withstanding isolation voltage (60s)	1.5	4	kV_{RMS}
V_{IOWM}	Maximum working isolation voltage	480	690	V_{RMS}
V_{IOTM}	Maximum transient isolation voltage (60s)	2.1	5.65	kV
V_{IORM}	Maximum repetitive peak isolation voltage	678	975	V
CMTI	Common-Mode Transient Immunity	200	200	V/ns
CMT_{BLANK}	Common mode transient threshold for blanking V1 & V2	>5	>5	V/ns
t_{BLANK_DLY}	Output refresh delay after blanking	<55	<55	ns

Electrical Characteristics at 5V Supply

VDD/VCC, VDD1, VDD2 over recommended operating conditions. Typical values are given at 25°C ambient temperature and VDD=VCC=VDD1=VDD2=5V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} output high level	VO1, VO2, I_{OUT} = -50mA	3.66	4.62	5.26	V
V_{OL} output low level	VO1, VO2, I_{OUT} = 50mA	0.08	0.14	0.32	V
I_{PU_PK} peak pull-up current on VO1, VO2	C_{LOAD} = 1nF		190		mA
I_{PD_PK} peak pull-down current on VO1, VO2	C_{LOAD} = 1nF		300		mA
V_{IH} input high level	V1, V2, EN/FLTB	2.08	2.47	2.8	V
V_{IL} input low level	V1, V2, EN/FLTB	0.82	1.11	1.7	V
V_{IHYST} input hysteresis	V1, V2, EN/FLTB	0.9	1.36	1.62	V
V_{FLTB} EN/FLTB voltage in fault mode	I_{SINK}=5mA			0.8	V
I_{IH} high-level input leakage at V1	V1 = 5.5V			50	µA
I_{IH} high-level input leakage at V2	V2 = 5.5V			10	µA
I_{IL} low-level input leakage at V_{FLTB}	V_{FLTB} = 0V, VCC=VDD=5.5V	-90			µA
$V_{TH\_UVLO\_UV\_VDDx}$ rising edge UVLO threshold	VDDx rising edge	4.230	4.350	4.480	V
$V_{TH\_UVLO\_DN\_VDDx}$ falling edge UVLO threshold	VDDx falling edge	4.120	4.240	4.360	V
$V_{UVLO\_HYST\_VDDx}$ UVLO threshold hysteresis	VDDx	82.5	107	115	mV

Switching Characteristics

VDD/VCC, VDD1, VDD2 over recommended operating conditions. Typical values are given at 25°C ambient temperature and VDD=VCC=VDD1=VDD2=5V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDLH}, t_{PDHL} Propagation Delay	V1,V2,EN/FLTB to VO1,VO2	30	50	65	ns
$\lvert t_{PDLH}-t_{PDHL} \rvert$ Pulse Width Distortion	V1,V2 to VO1,VO2			3.5	
Channel to channel skew VDD1=VDD2=5V	V1 to VO1 vs. V2 to VO2			1.5	
Channel to channel skew VDD1/2=4.5V VDD2/1=5.5V	V1 to VO1 vs. V2 to VO2			5	
t_R Output rise time	C_{OUT} = 15pF, 10% to 90%		1	2.3	
t_F Output fall time	C_{OUT} = 15pF, 90% to 10%		1	2.3	
t_{DT} Dead time		14.4	18	24	
t_{START} Startup time (secondary sides)	During fast supply rising edge		1	2	µs

Supply Current Characteristics

VDD=VCC, VDD1, VDD2 over recommended operating conditions. Typical values are given at 25°C ambient temperature and VDD=VCC=VDD1=VDD2=5V.

PARAMETER	CONDITIONS	CURRENT	MIN	TYP	MAX	UNIT
Supply current in disabled mode	EN/FLTB = 0V	IVDD		200		µA
		IVDD1		275		
		IVDD2		275		
Supply current in DC mode	V1 = 0V & V2 = 0V	IVDD		350	450	µA
		IVDD1		300	385	
		IVDD2		300	385	
	V1 = 5V & V2 = 5V	IVDD		350	450	
		IVDD1		300	385	
		IVDD2		300	385	
Supply current at 1MHz	50% Duty Cycle, VO1 & VO2 load 15pF[1]	IVDD		560	715	µA
		IVDD1		395	485	
		IVDD2		395	485	
Supply current at 10MHz	50% Duty Cycle, VO1 & VO2 load 15pF[1]	IVDD		2.4	3.15	mA
		IVDD1		1.09	1.37	
		IVDD2		1.09	1.37	

[1] Dynamic current in C_{load} is removed from the supply current

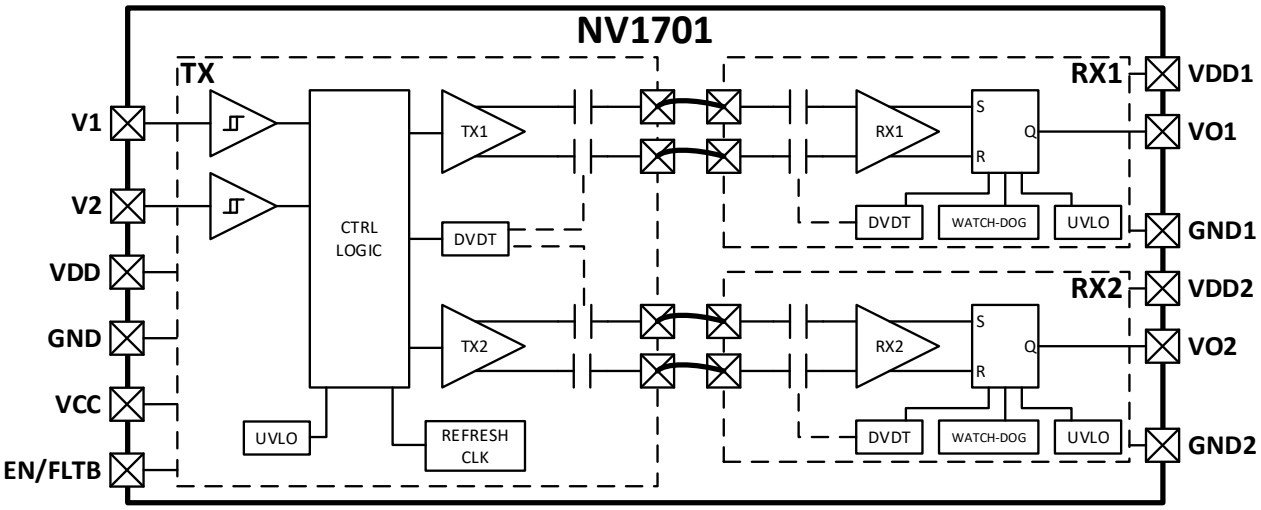
VCC (VDD generated by internal LDO), VDD1, VDD2 over recommended operating conditions. Typical values are given at 25°C ambient temperature and VCC=12V, VDD1=VDD2=5V.

PARAMETER	CONDITIONS	CURRENT	MIN	TYP	MAX	UNIT
Supply current in disabled mode	EN/FLTB = 0V	IVCC		250		µA
		IVDD1		275		
		IVDD2		275		
Supply current in DC mode	V1 = 0V & V2 = 0V	IVCC		360	385	µA
		IVDD1		300	325	
		IVDD2		300	325	
	V1 = 5V & V2 = 5V	IVCC		360	385	
		IVDD1		300	325	
		IVDD2		300	325	
Supply current at 1MHz	50% Duty Cycle, VO1 & VO2 load 15pF[2]	IVCC		570	625	µA
		IVDD1		390	430	
		IVDD2		390	430	
Supply current at 10MHz	50% Duty Cycle, VO1 & VO2 load 15pF[2]	IVCC		2.15	2.4	mA
		IVDD1		1.09	1.28	
		IVDD2		1.09	1.28	

[2] Dynamic current in C_{load} is removed from the supply current

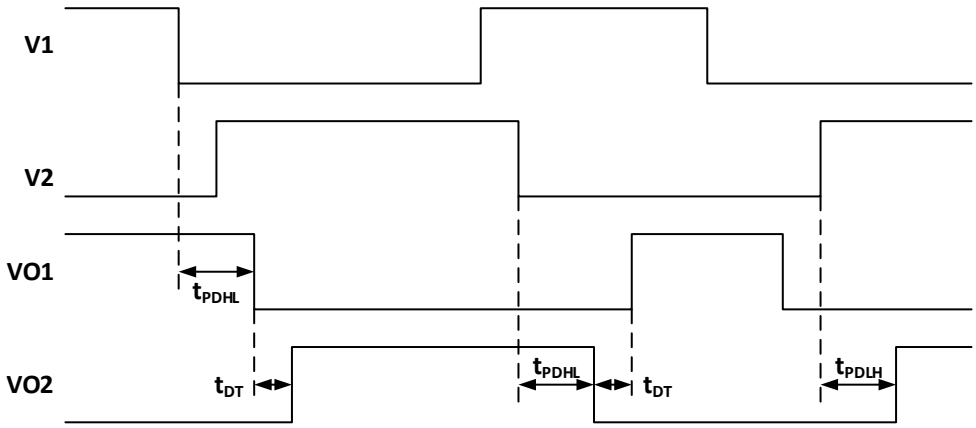
DETAILED DESCRIPTION

Block Diagram



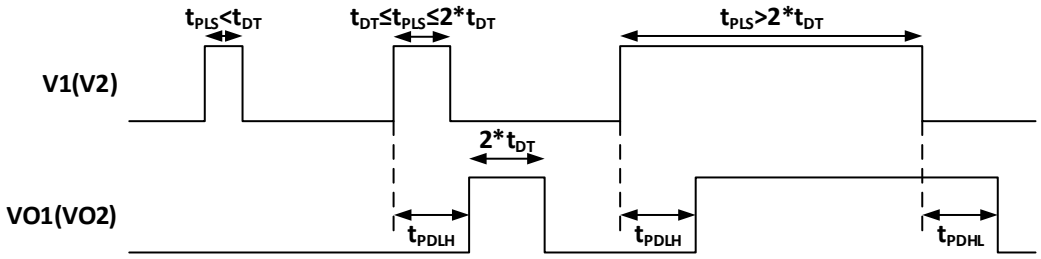
Input logic (AST)

The NV1701 is composed of a transmitter die and two identical receiver dies. The distance between each die is such that it can sustain the HV rating of the product. An anti-shoot-through (AST) logic is integrated, with a dead time t_{DT} of 18ns typical. The logic is such that if both V1 and V2 inputs are high, none or only one of the outputs will be active. One output will be active only if its corresponding input is high for at least t_{DT} delay prior the rising of the other input. If both inputs go up within t_{DT} delay, then both outputs will remain low.

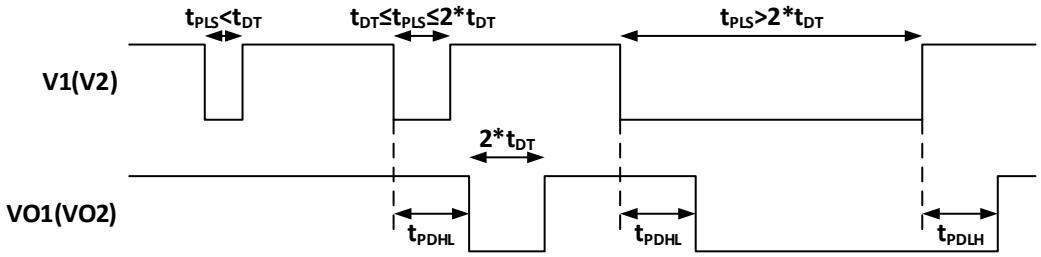


Before passing by the internal AST logic, each input passes through a deglitch circuit, also with the same deglitch time t_{DT}. Any toggling at the deglitch circuit input resets its timing. Only pulses with at least t_{DT} duration without any digital noise can pass the internal deglitch circuit and go to the AST logic.

In practice, the minimum recommended input pulse width is $2*t_{DT}$. If the inputs are driven by a shorter pulse ($t_{DT}<tpulse<2t_{DT}$), it will be internally extended to the minimum pulse duration of $2*t_{DT}$. For $tpulse<t_{DT}$, the input is filtered-out by the internal deglitch circuit.



Positive Input Pulse



Negative Input Pulse

It is not recommended to rely on the internal AST logic as the 18ns typical internal dead time is small and might not be sufficient in some applications. It can be considered as an internal protection that will limit shoot-through duration in case of error on external controls during the development of a new board.
All inputs (V1, V2, EN/FLTB) have TTL compatible levels. It is not recommended to exceed 14V on these digital inputs (note that these are high-voltage pads so that there is no risk of self-supply of the chip if V1, V2 or EN/FLTB is high while VDD or VCC are not supplied).

EN/FLTB

This pin is internally pulled up to VDD across a HV pass transistor. This pin can have an optional external pull-up up to 18V (+10%). Any capacitor on this pin can slow down the turn-on of the circuit. This pin is internally pulled down (with at least 5mA pull-down current) if VDD is below UVLO threshold. EN/FLTB can never be directly connected to a positive supply with a low impedance. The minimum external pull-up resistor, if used, should be at least equal to the external pull-up voltage divided by 5mA. If a smaller pull-up resistor is used, the circuit could detect an over-current in the EN/FLTB pin and protect it by implementing a hiccup current limitation on this pin (typical 600ns active and 12µs off).
The EN/FLTB input is blocking the signals V1 / V2 using two internal AND gates. The outputs of these two internal AND gates go to the internal deglitch and AST logic of previous section. It also means that any digital noise on EN/FLTB can directly affect the internal V1 and V2 signals. In noisy environment, it might be required to add a local decoupling capacitance on the EN/FLTB pin to avoid unexpected disturbances (this extra capacitor slows down the circuit startup).
When an internal fault is activated, this fault is internally forced to a minimum duration of 2.5µs typical. When such a fault occurs, it immediately sends a reset pulse to the two output channels of the chip (VO1 and VO2). Note that no internal refresh is sent during a fault as the outputs are automatically reset thanks to their integrated watchdog feature.

VO1 / VO2 outputs

These outputs can drive typical 190mA source and 300mA sink peak currents with the VDD1 / VDD2 level (5V typical). These outputs have a short-circuit protection to GND and VDD. For a short-circuit to GND (resp. VDD), if the output does not exceed 40% of VDD level (resp. does not pass below 30% of VDD) within 600ns when the input is high (resp. low), the circuit will consider that there is a short-circuit condition. In this case, the output is immediately set to high impedance for 10µs. After this, if the input is still “1” (resp. “0”), the driver will try again for 600ns to pull-up (resp. pull-down) the output. This Hiccup protection limits the average output current in case of short-circuit to GND or VDD.

Watchdog & Refresh

The isolator uses a proprietary modulation technique with a periodic data refresh, so that in case of unexpected corrupted data, it would not last for more than 340ns. Also, if the isolator receiver’s part does not detect any signal from a data change or refresh pulse during 1.5µs, the internal watchdog is triggered. In this case, the output is immediately forced to zero, as long as there is no detected input signal. Note that in case of a slow decrease of the primary side supply (<1V/µs), the transmitter is able to send a last RESET pulse to the receiver when the transmitter UVLO threshold is reached. The VO1 and VO2 outputs are then reset to GND1 and GND2 respectively. The watchdog feature is a security in case of prompt accidental loss of the primary supply, in which case the primary would not have time to send a last reset pulse.

Supplies

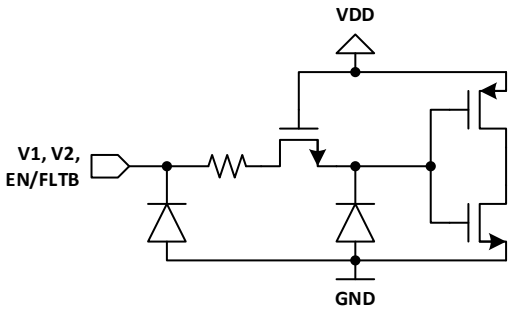
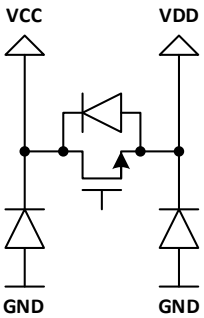
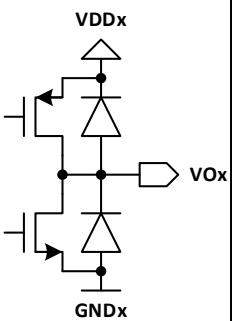
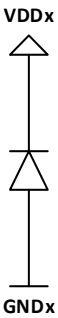
A decoupling capacitor of at least 10nF is recommended on VDD1 and VDD2.
On the primary side of the NV1701, the circuit can be supplied either by VCC (>7.2V) or by VDD (5V) directly.
If supplied by VCC, it is recommended to add at least 3nF on VDD (and 10nF if the circuit can see dv/dt events larger than 20V/ns). If a larger capacitor is used, it will appear as a temporary short-circuit for the LDO so that the EN/FLTB

would remain low till the capacitor is charged (with a pull-up current of about 1mA once the short-circuit protection is activated). It is not recommended to exceed 100V/µs on VCC vs. GND as it might generate a slight overshoot at the LDO output. When using VCC, the VDD pin should not be used to bias any noisy external circuit. VDD could be used for sourcing external low noise circuits with maximum 1mA.
If supplied directly by an external 5V supply on VDD, then VCC must be connected to VDD. A 10nF decoupling capacitor is recommended.
On the primary side, the startup time can be as low as 3µs for fast rising supply. On the secondary side, the startup time can be as low as 1µs for fast rising VDD1/VDD2 supply.

High voltage dv/dt & Blanking

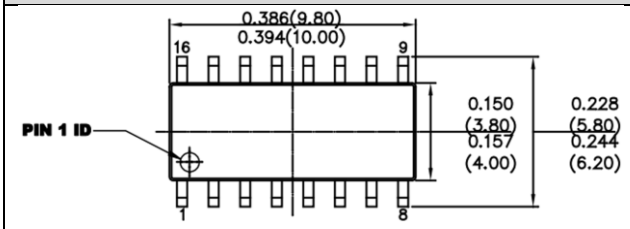
The NV1701 is optimized for switching applications. For dv/dt events (between GND and any GND1/GND2) up to 5V/ns, VO1/VO2 will remain a delayed copy of V1/V2 with low distortion and low jitter.
Above 5V/ns (between 5V/ns and 10V/ns), a blanking feature is implemented independently for each channel. The blanking is operating as follows. As soon as the primary side of the NV1701 detects a dv/dt event above 5V/ns (one detector for each channel 1 and 2), it samples and holds the corresponding input state. During this time, no refreshing SET or RESET pulse is sent across the capacitive insulation. When dv/dt event goes below 5V/ns plus an internal delay of typically 16ns, the primary side stops its sample/hold status and reconsiders the input state at that moment. Based on this, it immediately sends the relevant SET or RESET pulse to refresh the secondary side state that was in hold state during the dv/dt. During the primary side blanking period, any input change (after the internal deglitch circuitry) is not considered. It will be considered only when the dv/dt is finished (<5V/ns).

ESD I/O Schematics

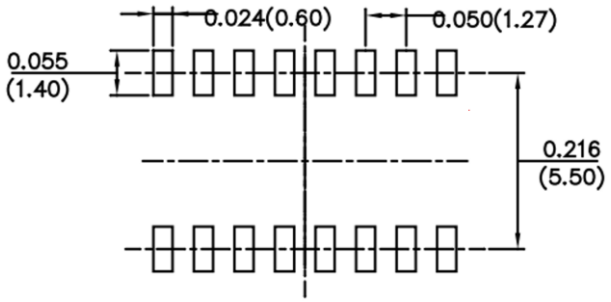
Inputs	Input supplies	Outputs	Output supplies
			

PACKAGE INFORMATION

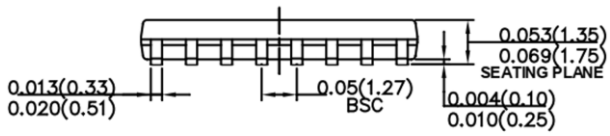
Narrow Body SOIC16N

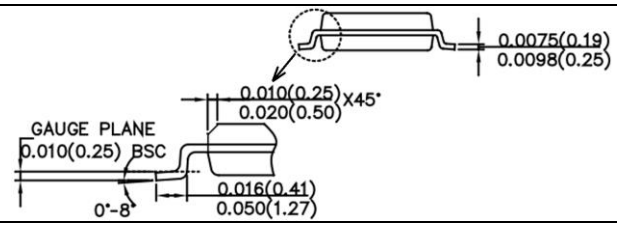


Top View



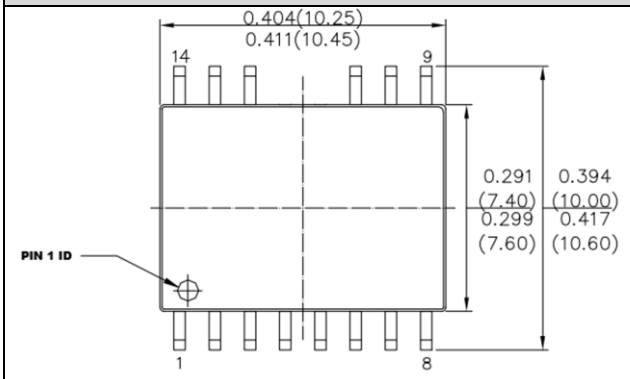
Recommended Land Pattern



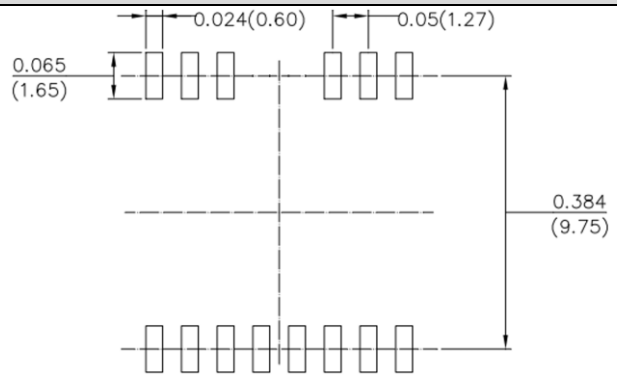


Side Views

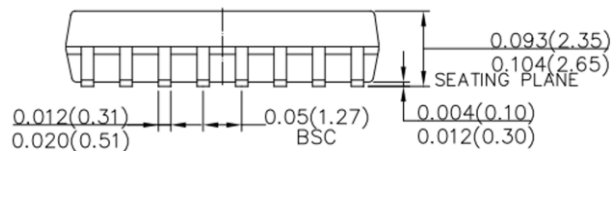
Wide Body SOIC14N

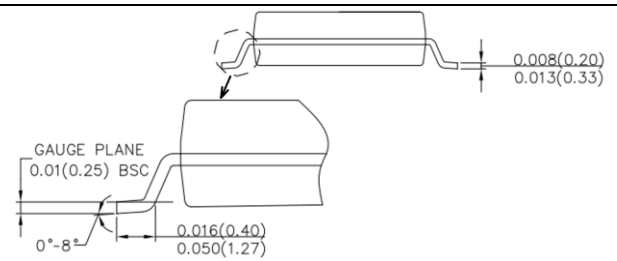


Top View



Recommended Land Pattern





Side Views

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