IsoFast™ Dual Independent Channel Digital Isolated Bi-Directional GaN Gate Driver

FEATURES

- **Extreme CMTI up to 200V/ns**
- **Switching Frequency up to 7MHz**
- **Minimum Pulse Width 36ns**
- **Low Pulse Width Distortion < 10ns**
- **Very Low Jitter < 1ns**
- **Double Capacitive Isolation**
- **Peak Isolation Voltage V_{ISO} (60s) > 4kV_{RMS}**
- **DC Working Voltage V_{IORM} (40yrs) 975V**
- **2kV HBM ESD Protection**
- **Temperature Range -40°C to 125°C**
- **Output Supply Range 10V…18V±10% (VCC1, VCC2)**
- **TTL Digital Input Controls compatible with 3.3V±10%, 5V±10% and 12V±10%**
- **80mA pull-up / 300mA pull-down GaN driver typical peak current**
- **Input Supply Operation compatible with 8V…18V±10% (VCC) or 5V±10% (VDD)**
- **SOIC16 Narrow Body and SOIC14 Wide Body**
- **Carrier-Free Modulation**
- **Under Voltage Lockouts on all VDD and VCCx**
- **Regulated gate voltage for GaN power switch**
- **Low Quiescent-current Consumption (350µA on input supply and 390µA on each output supply)**
- **Low current consumption in disabled mode (230µA on input supply and 290µA on each output supply)**

APPLICATIONS

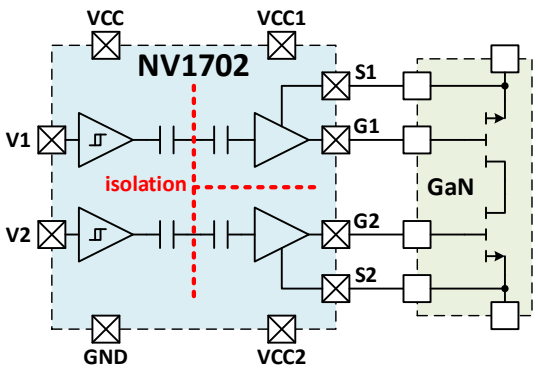
- **Single-Stage Converters**
- **DC-DC Switched Power Supplies**
- **High-Voltage Motor Control**
- **High-Voltage Inverters**

DESCRIPTION

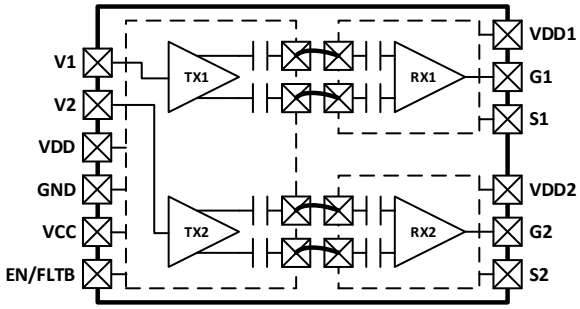
The NV1702 is a dual-independent-channel digital isolated bi-directional GaN driver. This device has two fully isolated drivers specifically designed to drive GaN power switches with medium on-resistance range and low dV/dt applications (10V/ns to 20V/ns). The digital input controls are galvanically isolated from the drivers' sides via Navitas's proprietary double capacitive Silicon isolation barrier. It provides isolation above 10 kV surge voltage between any input or output combination and can sustain common mode transients as large as 200V/ns.

A digital signal is received through a 3-12V compatible Schmitt-triggered input buffer, translated to a proprietary modulated balanced signal, transmitted across an integrated dual-layer capacitive isolation barrier before being demodulated and buffered to the GaN driver output. Navitas's proprietary modulation technique is free of high frequency carrier for better EMC performances while providing a periodic refresh signal every $t_{REFRESH}$ < 340ns in case of steady state input signal. The NV1702 has been optimized for switching applications. In such cases, the power switches do not toggle while a fast transient event (dV/dt) is occurring. A blanking feature is implemented in NV1702 making it robust against possible input noise induced by hard-switching events. The NV1702 is able to transmit short pulses as low as 36ns with low distortion and very low jitter, making it an ideal choice when, for example, extreme conversion ratio (i.e. very low duty cycles) is required as in DC-DC converter applications.

Isolated Bi-directional Switch

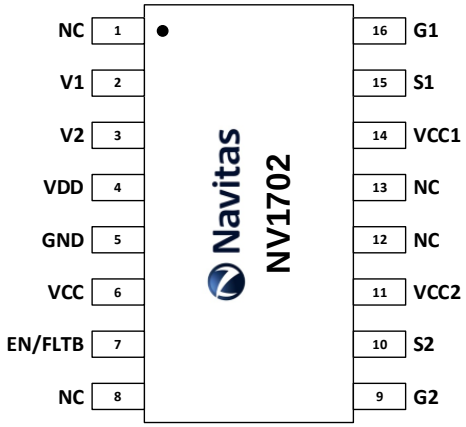


Simplified block diagram

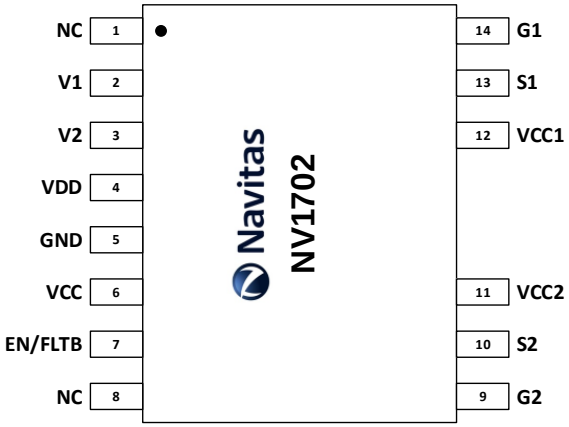


PIN DESCRIPTION

SOIC16N (Top View)



SOIC14W (Top View)



Pin Definition

PIN NUMBER		PIN NAME	FUNCTION	DESCRIPTION
SOIC16N	SOIC14W			
1	1	NC	NA	Do not connect.
2	2	V1	Digital Input	digital input for channel 1.
3	3	V2	Digital Input	digital input for channel 2.
4	4	VDD	Positive Supply	5V Input/Output power supply. When VCC is available, the VDD is internally generated and must be left floating (see "Supplies" section further in this document). In this case VDD could be used for sourcing external low noise circuits with maximum 1mA. If VCC is not available, VDD must be shorted to VCC and supplied with 5V voltage source.
5	5	GND	Ground	Input ground.
6	6	VCC	Positive Supply	Input power supply. Connect to 8V…18V voltage source. If not available, see pin 4.
7	7	EN/FLTB	Digital Input/Output	Enable input and Fault output. In normal operation, this pin must be driven high via pull-up resistor to VDD or VCC with R_{PU}=VCC/5mA. It has an internal pull-up to VDD with 100kΩ typical. When driven low, it unconditionally drives the G1 and G2 outputs low. In case of fault condition (UVLO on VDD), this pin is driven low for at least 2.5µs, with a typical 5mA current strength.
8	8	NC	NA	Do not connect.
9	9	G2	Gate 2	Output channel 2 gate.
10	10	S2	Source 2	Output channel 2 source.
11	11	VCC2	Positive Supply	Output channel 2 power supply. Connect to 10V…18V voltage source.
12	NA	NC	NA	Left floating or removed for isolation between output channels.
13				
14	12	VCC1	Positive Supply	Output channel 1 power supply. Connect to 10V…18V voltage source.
15	13	S1	Source 1	Output channel 1 source.
16	14	G1	Gate 1	Output channel 1 gate.

SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
VCC vs. GND	DC Supply vs. ground	-0.5	26.4	V
VCCx vs. Sx	DC Supply vs. ground (same side)	-0.5	26.4	
GND vs. S1 GND vs. S2 S1 vs. S2	DC Isolation SOIC16N	-750	750	
GND vs. S1 GND vs. S2 S1 vs. S2	DC Isolation SOIC16W	-1500	1500	
Inputs vs GND	Input voltage on V1, V2 versus GND	-0.5	14	
EN/FLTB vs GND	Input voltage on EN/FLTB versus GND	-0.5	26.4	
Outputs vs GNDx	Output voltage on Gx versus Sx (same side)	-0.5	12	
Tj	Junction temperature	-40	150	°C

ESD Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{HBM}	Human Body Model robustness	-2000	2000	V
V_{CDM}	Charged Device Model robustness	-500	500	V
$I_{LATCHUP}$	Latch-up immunity	-200	200	mA

Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
VCC vs. GND	High Voltage DC Supply vs. ground	7.2	19.8	V
VDD vs. GND	DC Supply vs. ground (primary side)	4.5	5.5	V
I(VDD)	External use (output sourcing current)	0	1	mA
VCCx vs. Sx	DC Supply vs. ground (secondary side)	9	19.8	V
Inputs vs GND	Input voltage on V1, V2, versus GND	-0.3	13.2	V
EN/FLTB vs. GND	Enable input versus GND	-0.3	19.8	
FREQ	Input Data Frequency	0	7	MHz
T_A	Ambient Temperature	-40	125	°C

Insulation Characteristics

PARAMETER	DESCRIPTION	SOIC16N	SOIC14W	UNIT
CLR External clearance	Shortest distance through air	>4	>8	mm
CRP External creepage	Shortest distance through the package	>4	>8	
DTI Isolation distance	Minimum internal isolation gap	>20	>20	µm
C_{IB}	Isolation barrier capacitance (per channel)	200	200	fF
V_{ISO}	Withstanding isolation voltage (60s)	1.5	4	kV_{RMS}
V_{IOWM}	Maximum working isolation voltage	480	690	V_{RMS}
V_{IOTM}	Maximum transient isolation voltage	2.1	5.65	kV
V_{IORM}	Maximum repetitive peak isolation voltage	678	975	V
CMTI	Common-Mode Transient Immunity	200	200	V/ns
CMT_{BLANK}	Common mode transient threshold for blanking V1 & V2	>5	>5	V/ns
t_{BLANK_DLY}	Output refresh delay after blanking	<55	<55	ns

Electrical Characteristics at 5V Supply

VDD/VCC, VCC1, VCC2 over recommended operating conditions. Typical values are given at 25°C ambient temperature and VDD=VCC=5V and VCC1=VCC2=12V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{Gx} steady state gate high level on G1, G2			6.2	6.9	V
R_{PD_GX} pull-down resistance on G1, G2	IG1 = IG2 = 50mA	0.698	1.118	2.148	Ω
I_{PU_PK} peak pull-up current on G1, G2	C_{LOAD} = 1nF		82		mA
I_{PD_PK} peak pull-down current on G1, G2	C_{LOAD} = 1nF		326		mA
V_{IH} input high level	V1, V2, EN/FLTB	2.08	2.47	2.8	V
V_{IL} input low level	V1, V2, EN/FLTB	0.82	1.11	1.7	V
V_{IHYST} input hysteresis	V1, V2, EN/FLTB	1.08	1.36	1.62	V
V_{FLTB} EN/FLTB voltage in fault mode	I_{SINK}=5mA			0.8	V
I_{IH} high-level input leakage at V1	V1 = 5.5V			30	µA
I_{IH} high-level input leakage at V2	V2 = 5.5V			10	µA
I_{IL} low-level input leakage at V_{FLTB}	V_{FLTB} = 0V, VCC=VDD=5.5V	-90			µA
$V_{TH\_UVLO\_UP\_VCC}$ rising edge UVLO threshold	VCCx rising edge	8	8.4	8.8	V
$V_{TH\_UVLO\_DN\_VCC}$ falling edge UVLO threshold	VCCx falling edge	7	7.3	7.6	V
$V_{UVLO\_HYST\_VCC}$ UVLO threshold hysteresis	VCCx	1	1.1	1.15	V
$V_{TH\_UVLO\_UP\_VDD}$ rising edge UVLO threshold	VDDx rising edge	4.230	4.350	4.480	V
$V_{TH\_UVLO\_DN\_VDD}$ falling edge UVLO threshold	VDDx falling edge	4.120	4.240	4.360	V
$V_{UVLO\_HYST\_VDD}$ UVLO threshold hysteresis	VDDx	103	107	112	mV

Switching Characteristics

VDD/VCC, VCC1, VCC2 over recommended operating conditions. C_{LOAD}=0pF unless otherwise specified. Typical values are given at 25°C ambient temperature and VCC=VCC1=VCC2=12V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDLH}, t_{PDHL} Propagation Delay	V1 to G1, V2 to G2, C_{LOAD}=0pF	31	49	70	ns
$\lvert t_{PDLH}-t_{PDHL} \rvert$ Pulse Width Distortion	input 50% to output 10%/90%	0.5	1	8.8	
Channel to channel skew low to high	V1 to S1 vs. V2 to S2,	0.13	0.34	2.6	
Channel to channel skew high to low	VCC1=VCC2=12V	0.19	0.22	0.71	
t_R Output rise time	C_{LOAD} = 1nF, VCC1=VCC2=12V, 10%		70.6	114	
t_F Output fall time	to 90% (t_R), 90% to 10% (t_F)		17.7	27.6	
t_{DT} Deglitch time		14.4	18	21.6	
t_{START} Startup time (secondary sides)	During fast supply rising edge		1	2	µs

Supply Current Characteristics

VDD=VCC=5V, VCC1=VCC2=12V. Typical values are given at 25°C ambient temperature.

PARAMETER	CONDITIONS	CURRENT	MIN	TYP	MAX	UNIT
Supply current in disabled mode	EN/FLTB = 0V	IVDD		200		µA
		IVCC1		360		
		IVCC2		360		
Supply current in DC mode	V1 = 0V & V2 = 0V	IVDD		350	450	µA
		IVCC1		390	470	
		IVCC2		390	470	
	V1 = 5V & V2 = 5V	IVDD		350	450	
		IVCC1		440	485	
		IVCC2		440	485	
Supply current at 1MHz	50% Duty Cycle, G1 & G2 load 1nF[1]	IVDD		555	715	µA
		IVCC1		560	670	
		IVCC2		560	670	

[1] Dynamic current in C_{LOAD} is removed from the supply current.

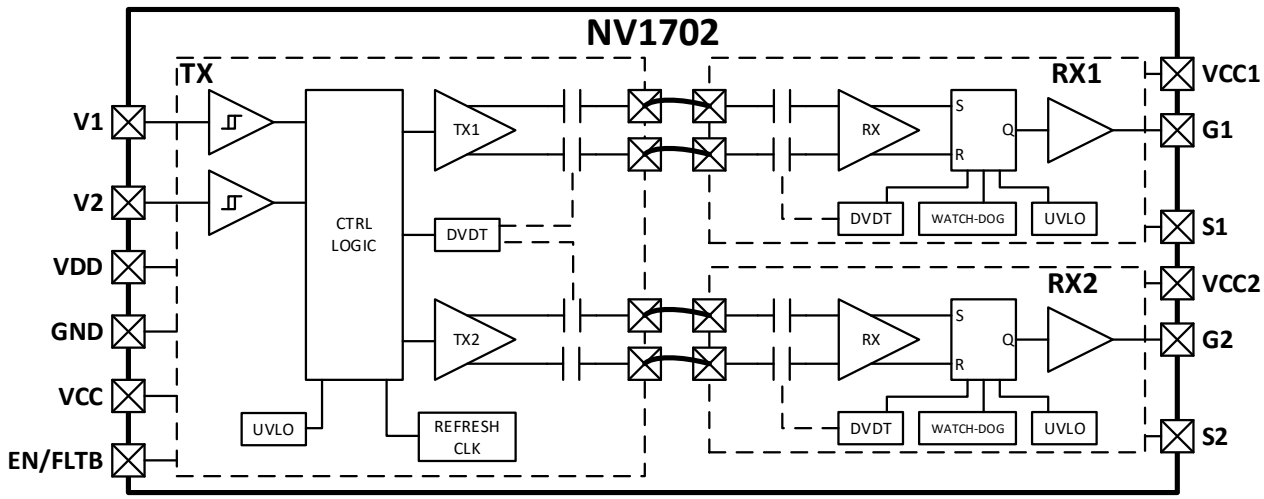
VCC=12V (VDD generated by internal LDO), VCC1=VCC2=12V. Typical values are given at 25°C ambient temperature.

PARAMETER	CONDITIONS	CURRENT	MIN	TYP	MAX	UNIT
Supply current in disabled mode	EN/FLTB = 0V	IVCC		250		µA
		IVCC1		360		
		IVCC2		360		
Supply current in DC mode	V1 = 0V & V2 = 0V	IVCC		360	440	µA
		IVCC1		390	470	
		IVCC2		390	470	
	V1 = 5V & V2 = 5V	IVCC		360	440	
		IVCC1		440	485	
		IVCC2		440	485	
Supply current at 1MHz	50% Duty Cycle, G1 & G2 load 1nF[2]	IVCC		575	685	µA
		IVCC1		560	670	
		IVCC2		560	670	

[2] Dynamic current in C_{LOAD} is removed from the supply current.

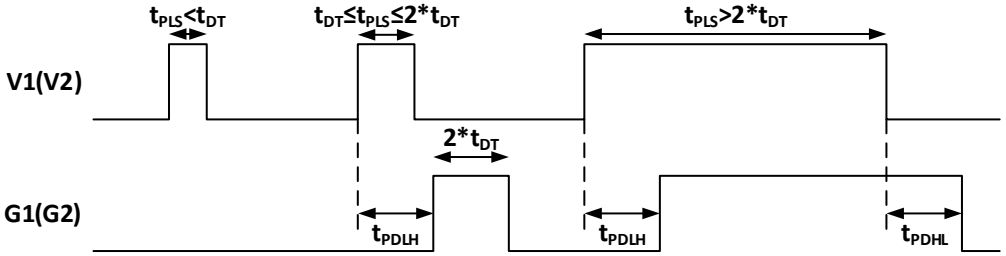
DETAILED DESCRIPTION

Block Diagram

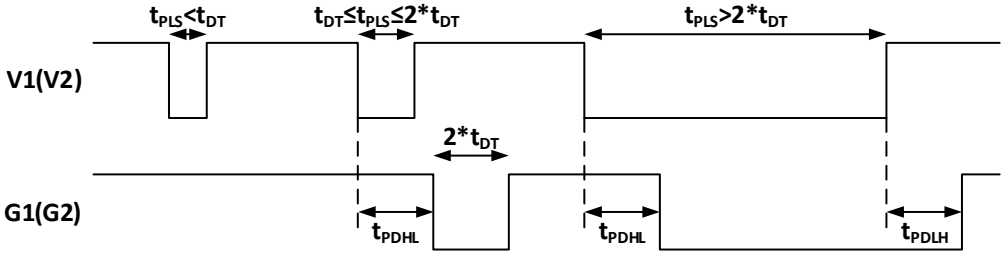


Input logic

The NV1702 is composed of a transmitter die and two identical receiver dies. The distance between each die is such that it can sustain the HV rating of the product. The inputs V1 & V2 levels are transferred to the G1 & G2 gate drivers' outputs after the propagation delays t_{PDLH} and t_{PDHL}. Each input passes through a deglitch circuit, with the same deglitch time t_{DT}. Any toggling at the deglitch circuit input resets its timing. Only pulses with at least t_{DT} duration without any digital noise can pass the internal deglitch circuit.



Positive Input Pulse



Negative Input Pulse

In practice, the minimum recommended input pulse width is $2*t_{DT}$. If the inputs are driven by a shorter pulse ($t_{DT}<t_{PLS}<2t_{DT}$), it will be internally extended to the minimum pulse duration of $2*t_{DT}$. For $t_{PLS}<t_{DT}$, the input is filtered-out by the internal deglitch circuit.

All inputs (V1, V2, EN/FLTB) have TTL compatible levels. It is not recommended to exceed 14V on these digital inputs (note that these are high-voltage pads so that there is no risk of self-supply of the chip if V1, V2 or EN/FLTB is high while VDD or VCC are not supplied).

It should be noted that NV1702 input logic has purposely no integrated anti-shoot through (AST) feature between channel 1 and channel 2. The user must carefully design AST feature with sufficient dead-time at system level for safe operation in classical half-bridge topology.

EN/FLTB

This pin is internally pulled up to VDD across a HV pass transistor. This pin can have an optional external pull-up up to 18V (+10%). Any capacitor on this pin can slow down the turn-on of the circuit. This pin is internally pulled down (with at least 5mA pull-down current) if VDD is below UVLO threshold. EN/FLTB can never be directly connected to a positive supply with a low impedance. The minimum external pull-up resistor, if used, should be at least equal to the external pull-up voltage divided by 5mA. If a smaller pull-up resistor is used, the circuit could detect an over-current in the EN/FLTB pin and protect it by implementing a hiccup current limitation on this pin (typical 600ns active and 12µs off).
The EN/FLTB input is blocking the signals V1 / V2 using two internal AND gates. The outputs of these two internal AND gates go to the internal deglitch logic of previous section. It also means that any digital noise on EN/FLTB can directly affect the internal V1 and V2 signals. In noisy environment, it might be required to add a local decoupling capacitance on the EN/FLTB pin to avoid unexpected disturbances (this extra capacitor slows down the circuit startup).
When an internal fault is activated, this fault is internally forced to a minimum duration of 2.5µs typical. When such a fault occurs, it immediately sends a reset pulse to the two output channels of the chip (G1 and G2). Note that no internal refresh is sent during a fault as the outputs are automatically reset thanks to their integrated watchdog feature.

G1 / G2 outputs

These outputs can drive typical 80mA source and 300mA sink peak currents. These outputs have a short-circuit protection to Sx and VCCx. For a short-circuit to Sx (resp. VCCx), if the output does not exceed 40% of the Gx steady-state level (resp. does not pass below 30% of the Gx steady-state level) within 600ns when the input is high (resp. low), the circuit will consider that there is a short-circuit condition. In this case, the output is immediately set to high impedance. To get out from this fault state, a VCCx supply power-down below UVLO level is necessary.

Watchdog & Refresh

The isolator uses a proprietary modulation technique with a periodic data refresh, so that in case of unexpected corrupted data, it would not last for more than 340ns.
Also, if the isolator receiver's part doesn't detect any signal from a data change or refresh pulse during 1.5µs, the internal watchdog is triggered. In this case, the output is immediately forced to zero, as long as there is no detected input signal. Note that in case of a slow decrease of the primary side supply (<1V/µs), the transmitter is able to send a last RESET pulse to the receiver when the transmitter UVLO threshold is reached. G1 and G2 are then forced to zero. The watchdog feature is a security in case of prompt accidental loss of the primary supply, in which case the primary would not have time to send a last reset pulse.

Supplies

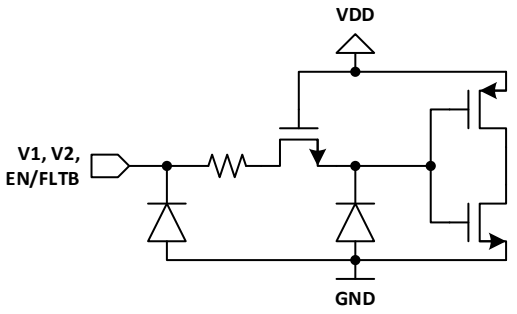
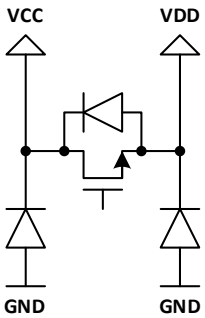
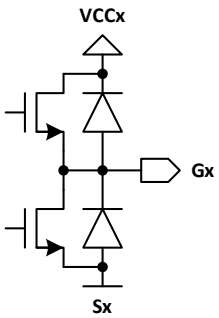
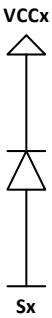
A decoupling capacitor of at least 10nF is recommended on VCC1 and VCC2. On the primary side of the NV1702, the circuit can be supplied either by VCC (>8V) or by VDD (5V) directly.
If supplied by VCC, it is recommended to add at least 3.3nF on VDD (and 10nF if the circuit can see dv/dt events larger than 20V/ns). If a larger capacitor is used, it will appear as a temporary short-circuit for the internal LDO so that the EN/FLTB would remain low till the capacitor is charged (with a pull-up current of about 1mA once the short-circuit protection is activated). It is not recommended to exceed 100V/µs on VCC vs. GND as it might generate a slight overshoot at the LDO output. When using VCC, the VDD pin should not be used to bias any noisy external circuit. VDD could be used for sourcing external low noise circuits with maximum 1mA.
If supplied directly by an external 5V supply on VDD, then VCC must be connected to VDD. A 10nF decoupling capacitor is recommended.
On the primary side, the startup time can be as low as 3µs for fast rising supply. On the secondary side, the startup time can be as low as 1µs for fast rising VCC1/VCC2 supply.

High voltage dv/dt & Blanking

The NV1702 is optimized for switching applications. For dv/dt events (between GND and any S1/S2 grounds) up to 5V/ns, G1/G2 will remain a delayed copy of V1/V2 with low distortion and low jitter.
Above 5V/ns (between 5V/ns and 10V/ns), a blanking feature is implemented independently for each channel. The blanking is operating as follows. As soon as the primary side of the NV1702 detects a dv/dt event above 5V/ns (one detector for each channel 1 and 2), it samples and holds the corresponding input state. During this time, no refreshing SET or RESET pulse is sent across the capacitive isolation. When dv/dt event goes below 5V/ns plus an internal delay of typically 16ns, the primary side stops its sample/hold status and reconsiders the input state at that moment. Based on this, it immediately sends the relevant SET or RESET pulse to refresh the secondary side state that was in hold state

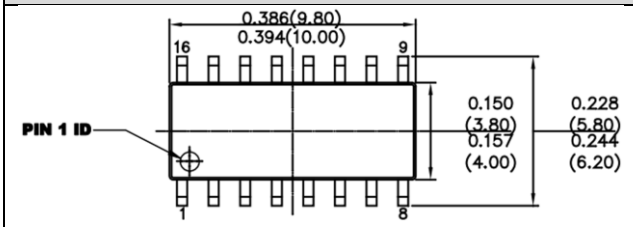
during the dv/dt. During the primary side blanking period, any input change (after the internal deglitch circuitry) is not considered. It will be considered only when the dv/dt is finished (<5V/ns).

ESD I/O Schematics

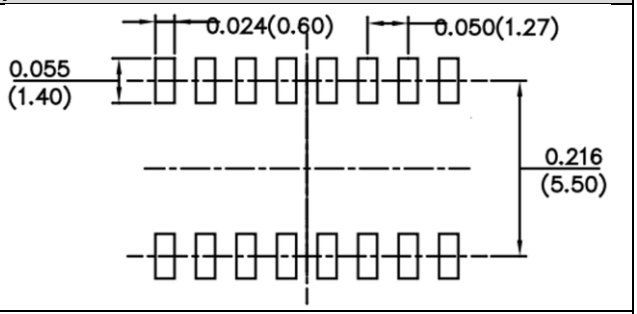
Inputs	Input supplies	Outputs	Output supplies
			

PACKAGE INFORMATION

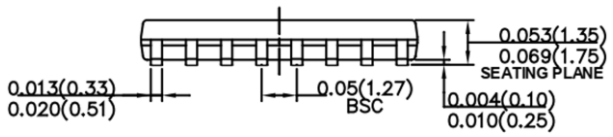
Narrow Body SOIC16N

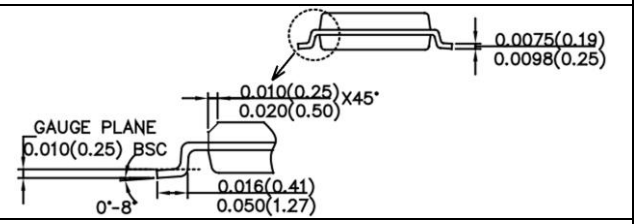


Top View



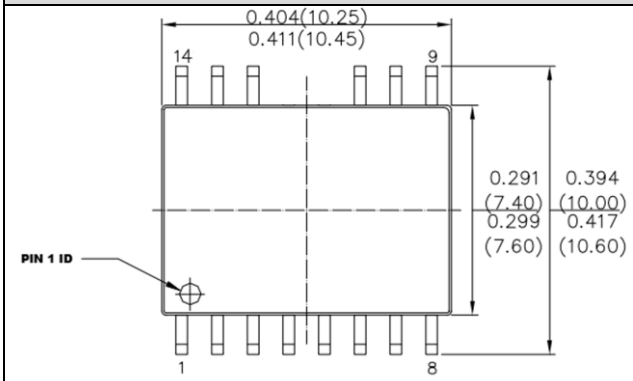
Recommended Land Pattern



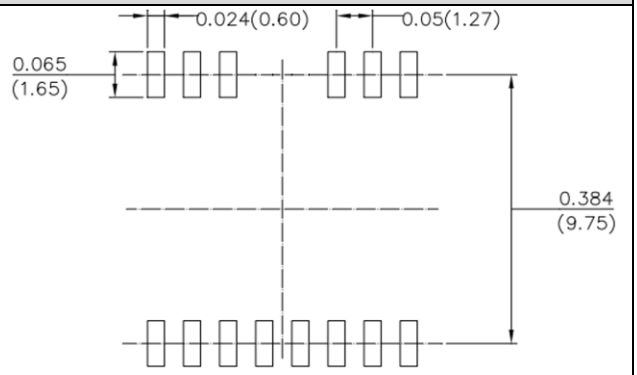


Side Views

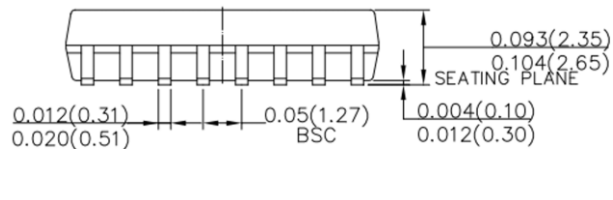
Wide Body SOIC14N

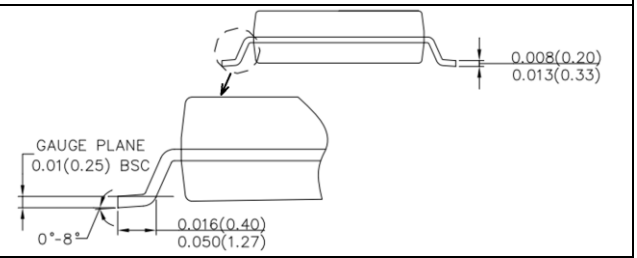


Top View



Recommended Land Pattern





Side Views

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