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# Application Notes for Surface Mount Assembly of Amkor's *MicroLeadFrame*<sup>®</sup> (MLF<sup>®</sup>) Packages



July 2013

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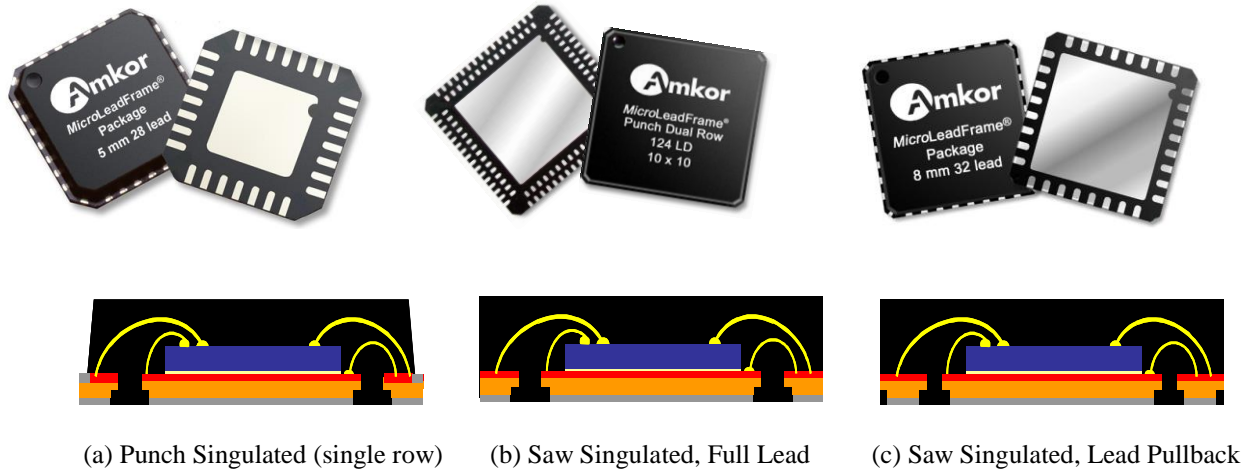
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## 1.0 Introduction

The *MicroLeadFrame*® package (MLF®) is a near CSP plastic encapsulated package with a copper leadframe substrate. This is a leadless package where electrical contact to the PCB is made by soldering the lands on the bottom surface of the package to the PCB, instead of the conventional formed perimeter leads. Amkor's ePad technology enhances the thermal and electrical properties of the package. The exposed die attach paddle on the bottom efficiently conducts heat to the PCB and provides a stable ground through down bonds and electrical connections through conductive die attach material. The design of the *MicroLeadFrame*® package also allows for flexibility. Its enhanced electrical performance enables the standard 2 GHz operating frequency to be increased up to 10 GHz with some design considerations.



**Figure 1. MLF® Package Photo and Cross Section Drawings**

The package comes in two formats: punch singulated, and saw singulated. While punch singulated packages are individually punched from molded strip during final assembly, the saw singulated package are assembled in array format and separated into individual components during the final sawing operation. The punch package family includes both single row and dual row configurations. The saw singulated package is divided into two options: Full Lead package, and Lead Pullback package. While full lead package has the whole thickness of the lead exposed on the package sides, the lead pullback package has a bottom half etch leadframe, resulting in only the top half of the lead thickness exposed to the sides of the package. Figure 1 depicts the different configurations of these packages. Dual Row designs are covered by a separate applications note and are not discussed within the context of this document. This application note addresses SMT considerations for single row designs of both punch and saw package configurations.

## 2.0 Surface Mount Considerations for MLF® Package

In order to perform at peak, special considerations are needed to properly design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, the exposed pad on the package needs to be soldered to the board using a corresponding thermal pad on the board. Furthermore, for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region. The PCB footprint design needs to be considered from dimensional tolerances due to package, PCB, and assembly.

A number of factors may have a significant effect on mounting MLF® package on the board and the quality of solder joints. Some of these factors include: amount of solder paste coverage in thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow profile. This applications note provides the guidelines for this purpose. It should be emphasized that this is just a guideline to help the user in developing the proper motherboard design and surface mount process. Actual studies as well as development effort maybe needed to optimize the process as per user's surface mount practices and requirements.

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### 3.0 PCB Design Guidelines

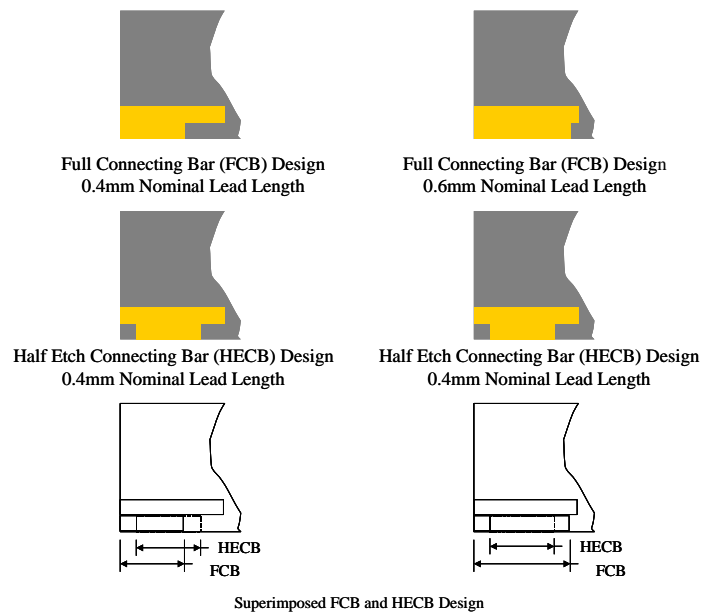
As shown in Figure 1, the lands on the package bottom side are rectangular in shape with rounded edge on the inside. Since the package does not have any solder balls, the electrical connection between the package and the motherboard is made by printing the solder paste on the motherboard and reflowing it after component placement. In order to form reliable solder joints, special attention is needed in designing the motherboard pad pattern and solder paste printing.

#### 3.1 Perimeter Pads Design

Typically the PCB pad pattern for an existing package is designed based on guidelines developed within a company or by following industry standards such as IPC-SM-782. However, since MLF® is a new package and the industry guidelines have not been developed yet for PCB pad pattern design, the development of proper design may require some experimental trials. For the purpose of this document, IPC's methodology is used here for designing PCB pad pattern. However, because of exposed die paddle and the package lands on the bottom side of the package, certain constraints are added to IPC's methodology. The pad pattern discussed in this application note includes considerations for lead and package tolerances and is considered appropriate for both standard leads and plated end lead (punch dimple) configurations.

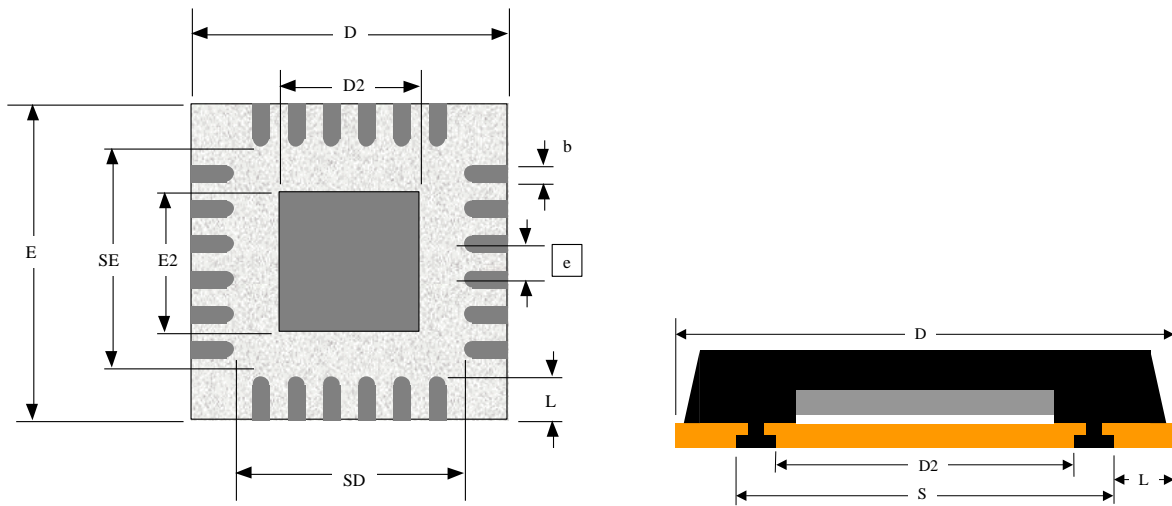
##### 3.1.1 Full Lead and Lead Pullback Options

Figure 2 shows the cross-sectional views of full lead and lead pullback package options for saw singulated packages. These options are also commonly referred to as Full Connecting Bar (FCB) and Half Etch Connecting Bar (HECB) designs. Notice that in full lead option the peripheral leads are extended all the way to package edges on the bottom side of the package. In case of lead pullback, the end of the leads are etched resulting in lands that are embedded in the mold compound except for the bottom side. To increase the length of the exposed leads on bottom, the leads are also pulled back by 0.1mm nominal. The cross-sectional view is shown in Figure 2, comparing the two options.



**Figure 2: Full vs. Half Etch Connecting Bar Design**

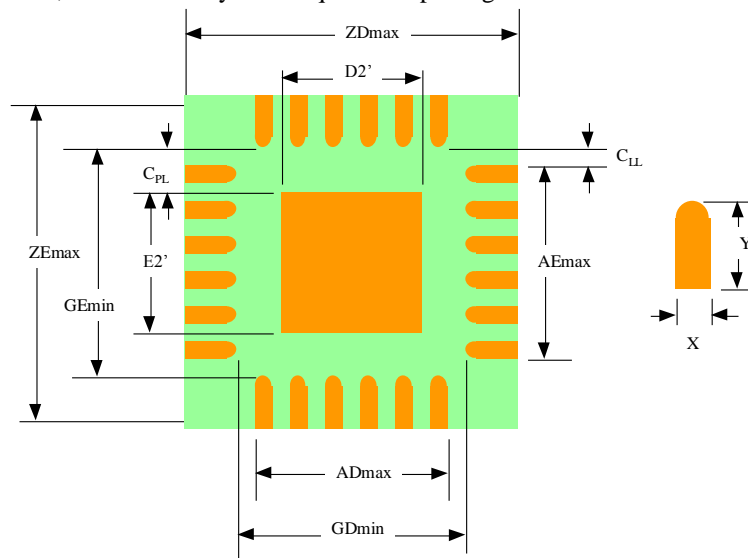
Figure 3 shows the bottom and side views of full lead option, indicating the dimensions needed to design the pad pattern for PCB. Although, the leads are pulled back in the HECB design, the PCB pad pattern does not need to change for these options. Since most packages are square with dimension D equal to dimension E and the leads are along the E direction for dual packages, the side view dimensions (D, S, D2, & L) are used to determine the land length on the PCB.



**Figure 3. MLF® (full lead design) component dimensions needed for PCB land pattern design.**

### 3.1.2 PCB Pad Pattern

The PCB pad pattern dimensions to be determined are shown in Figure 4. In the figure, the dimensions  $ZD_{max}$  and  $GD_{min}$  (and  $ZE_{max}$  and  $GE_{min}$ ) are the outside to outside and inside to inside dimensions, respectively. The dimension X and Y indicate the width and the length of the pad, respectively. Two additional clearances  $C_{LL}$  and  $C_{PL}$  are also defined to avoid solder bridging. While  $C_{LL}$  defines the minimum distance between land to land for the corner joints on adjacent sides,  $C_{PL}$  defines the minimum distance between the inner tip of the peripheral lands and the outer edge of the thermal pad. In order to design a proper pad pattern, tolerance analysis is required on package and motherboard dimensions.



**Figure 4. PCB Land Pattern Dimensions to be Determined.**

The tolerance analysis requires the consideration of a) component tolerances, b) the PCB tolerances, and c) the accuracy of the equipment used for placing the component. In addition, minimum values of toe, heel, and side fillets are considered for the formation of reliable solder joints.

For component tolerances, the profile tolerances usually given in the package outline drawing are converted into Maximum Material Condition (MMC) and Least Material Condition (LMC) based tolerances. The minimum and maximum

values thus obtained are listed in Table 1 for various MLF® type packages. In order to determine the pad pattern dimensions, three sets of tolerances are involved; one set for the overall component tolerances, and the other two sets for the leads on each end. Since it is unrealistic to assume that all three tolerances will be at their worst case, a more realistic RMS (root-mean-square) system is used here as described in IPC-SM-782.

The dimension S, shown in Figure 3, is not normally shown in package outline drawings. Since this dimension is required to determine the pad length, it is calculated as follows:

$$\begin{aligned}SD_{\min} &= D_{\min} - 2L_{\max} \\SD_{\max} &= SD_{\min} + SD_{\text{tol}} \text{ (rms)}\end{aligned}$$

Where,

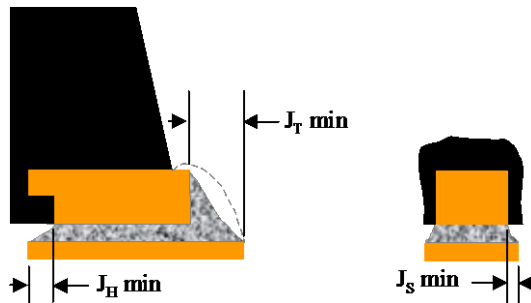
$$SD_{\text{tol}} \text{ (rms)} = \sqrt{(D_{\max} - D_{\min})^2 + 2(L_{\max} - L_{\min})^2}$$

The board tolerance defines the difference between the MMC and LMC of each pad pattern dimension and is assumed as 0.05mm here. The placement tolerance is also assumed as 0.05mm, given that most placement machines have placement accuracy between 20 and 70 microns.

The minimum values for solder joint fillets, defined in Figure 5, used to calculate the land pattern dimensions are:

Minimum Toe Fillet	= $J_T \text{ min}$	= 0.1mm
Minimum Heel Fillet	= $J_H \text{ min}$	= 0.05mm
Minimum Side Fillet	= $J_S \text{ min}$	= 0.0mm

The values are selected recognizing that both sides and one end of the leads are embedded in the mold compound and solder fillets cannot be formed on these sides. The fourth side, however, has either full or half the thickness of the lead exposed on the side of the package, depending on the full lead or lead pull back options. Since the pad pattern dimension is most likely to be larger than the nominal lead dimension, solder joints may assume some angular shape or fillets as shown in Figure 5 for full lead option. It should be realized that the formation of the toe fillet is not guaranteed as the sides of the leads are not plated. It is generally observed, however, that the toe fillets are formed depending on the type of solder paste used and length of exposure of package to environment. The toe fillet, if formed, will improve the solder joint reliability and allocation must be made for its formation. Although the toe fillet is not expected to form for the lead pullback option, the same pad pattern as the one for full lead option can be used for this design.



**Figure 5: Definition of toe, heel, and side fillets.**

#### Pad Pattern Design Calculations

With these assumptions and tolerances, the land pattern dimensions are determined by using the following relations:

$$\begin{aligned}ZD_{\max} &= D_{\min} + 2J_T + T_T \\X_{\max} &= b_{\min} + 2J_S + T_S \\GD_{\min} &= SD_{\max} - 2J_H - T_H\end{aligned}$$

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Where  $T_T$ ,  $T_S$ , and  $T_H$  are the RMS values of toe, heel, and side tolerances accounting for component, board, and placement tolerances. The calculations for these values are defined in more detail in IPC-SM-782 document.

The above calculation for  $GD_{min}$  does not account for the leads on all four sides of the package. In order to include this and to avoid any solder bridging between the two perpendicular leads on each corner, a minimum clearance,  $C_{LL}$ , is needed. This clearance, shown in Figure 3, is assumed as 0.1 mm and the final value of  $GD_{min}$  is determined by using the following constraint:

$$GD_{min} \geq AD_{max} + 2C_{LL}$$

Where

$$AD_{max} = (\text{Lead Pitch}) \times (\# \text{ of leads on one side} - 1) + \text{Pad Width}$$

Finally, the pad length is determined as:

$$Y = (ZD_{max} - GD_{min})/2$$

The pads may also be rounded on the inner edge.

**Using the above methodology, the perimeter pad pattern dimensions for various MLF® packages with Full lead option are listed in Table 1. It should be noted that the calculated  $X_{max}$  dimension (pad width) from the above equations is reduced for 0.4 and 0.5mm pitch devices to avoid any solder bridging issues. Also, because of rectangular dimension of the package in most case, the suffix D and E from dimension notations in Figure 3 (e.g. ZD and ZE) are dropped in the table and it is implied that  $Z_{max} = ZD_{max} = ZE_{max}$ .**

### 3.2 Thermal Pad and Via Design

The MLF® package is designed to provide a superior thermal performance. This is partly achieved by incorporating an exposed die paddle on the bottom surface of the package. However, in order to take full advantage of this feature, the PCB must have features to effectively conduct heat away from the package. This can be achieved by incorporating thermal pad and thermal vias on the PCB. While thermal pad provides a solderable surface on the top surface of the PCB (to solder the package die paddle on the board), thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat.

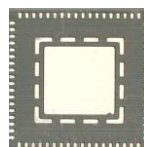
Normally, the size of the thermal pad should at least match the exposed die paddle size. However, depending upon the die paddle size, this size needs to be modified in some cases to avoid solder bridging between thermal pad and the perimeter pads. This is done by defining a clearance between the outer edges of the thermal pad and the inner edges of perimeter pads. This clearance is defined as  $C_{PL}$  in Figure 3 and is fixed as 0.15mm here. With this constraint, the maximum size of the thermal pad is calculated by the following relationship and is listed in Table 1 & 2 for various package sizes.

$$D2'_{TH} = G_{min} - 2C_{PL}$$

It should be noted that the  $D2'_{TH}$  dimension gives the theoretical maximum value. Since the size of the exposed die paddle on the component may actually be much smaller than this value, the actual  $D2'$  dimension should be modified by

$$\text{Component } D2 \leq D2' \leq D2'_{TH \text{ max}}$$

Note: MLF® with downbond ring design does not require the ring to be soldered to the board. The thermal pad design on the board should be based on the exposed paddle area, excluding the ring area.



In order to effectively transfer heat from the top metal layer of the PCB to the inner or bottom layers, thermal vias need to be incorporated into the thermal pad design. The number of thermal vias will depend on the application and power dissipation and electrical requirements. Although more thermal vias improve the package thermal performance, there is a point of diminishing returns as additional thermal vias may not significantly improve the performance. This is shown in Figure 6 where the effect of number of vias on  $\Theta_{ja}$  is plotted for 7mm, 48 lead package. A via diameter of 0.3mm was used for this simulation. As the via pitch decreases more vias can be incorporated for the same thermal pad size but the incremental performance improvement goes down.

**Table 1: Component and PCB Land Pattern Dimensions for Full Lead and Lead Pullback Options**

Package				Package Dimensions with Tolerance								Board Land Pattern Dimensions					
Size	I/O	Leads / Side	Lead Pitch	D(min)	D(max)	E(min)	E(max)	b(min)	b(max)	L(min)	L(max)	Xmax	Yref	Amax	Gmin	Zmax	D2'th max
6x5	8 (dual)	4	1.27	5.90	6.10	4.90	5.10	0.35	0.47	0.5	0.7	0.50	0.96	NA	4.39	6.31	4.09
3x3	12	3	0.8	2.90	3.10	2.90	3.10	0.28	0.40	0.5	0.7	0.42	0.57	2.02	2.17	3.31	1.87
4x4	12	3	0.8	3.90	4.10	3.90	4.10	0.28	0.40	0.5	0.7	0.42	0.96	2.02	2.39	4.31	2.09
5x5	16	4	0.8	4.90	5.10	4.90	5.10	0.28	0.40	0.5	0.7	0.42	0.96	2.82	3.39	5.31	3.09
6x6	20	5	0.8	5.90	6.10	5.90	6.10	0.28	0.40	0.5	0.7	0.42	0.96	3.62	4.39	6.31	4.09
7x7	28	7	0.8	6.90	7.10	6.90	7.10	0.28	0.40	0.5	0.7	0.42	0.96	5.22	5.39	7.31	5.09
8x8	32	8	0.8	7.90	8.10	7.90	8.10	0.28	0.40	0.5	0.7	0.42	0.96	6.02	6.39	8.31	6.09
9x9	36	9	0.8	8.90	9.10	8.90	9.10	0.28	0.40	0.5	0.7	0.42	0.96	6.82	7.39	9.31	7.09
10x10	44	11	0.8	9.90	10.10	9.90	10.10	0.28	0.40	0.5	0.7	0.42	0.87	8.42	8.57	10.31	8.27
2x3	8 (dual)	4	0.65	1.90	2.10	2.90	3.10	0.23	0.35	0.3	0.5	0.37	0.76	NA	0.79	2.31	0.49
3x3	8 (dual)	4	0.65	2.90	3.10	2.90	3.10	0.23	0.35	0.5	0.7	0.37	0.96	NA	1.39	3.31	1.09
4x4	16	4	0.65	3.90	4.10	3.90	4.10	0.23	0.35	0.5	0.7	0.37	0.92	2.32	2.47	4.31	2.17
5x5	20	5	0.65	4.90	5.10	4.90	5.10	0.23	0.35	0.5	0.7	0.37	0.96	2.97	3.39	5.31	3.09
6x6	28	7	0.65	5.90	6.10	5.90	6.10	0.23	0.35	0.5	0.7	0.37	0.96	4.27	4.42	6.31	4.12
7x7	32	8	0.65	6.90	7.10	6.90	7.10	0.23	0.35	0.5	0.7	0.37	0.96	4.92	5.39	7.31	5.09
8x8	40	10	0.65	7.90	8.10	7.90	8.10	0.23	0.35	0.5	0.7	0.37	0.96	6.22	6.39	8.31	6.09
9x9	44	11	0.65	8.90	9.10	8.90	9.10	0.23	0.35	0.5	0.7	0.37	0.96	6.87	7.39	9.31	7.09
10x10	52	13	0.65	9.90	10.10	9.90	10.10	0.23	0.35	0.5	0.7	0.37	0.96	8.17	8.39	10.31	8.09
3x3	8	2	0.50	2.90	3.10	2.90	3.10	0.18	0.30	0.5	0.7	0.28	0.96	0.78	1.39	3.31	1.09
3x3	12	3	0.50	2.90	3.10	2.90	3.10	0.18	0.30	0.5	0.7	0.28	0.94	1.28	1.43	3.31	1.13
3x3	16	4	0.50	2.90	3.10	2.90	3.10	0.18	0.30	0.3	0.5	0.28	0.69	1.78	1.93	3.31	1.63
4x4	20	5	0.50	3.90	4.10	3.90	4.10	0.18	0.30	0.5	0.7	0.28	0.94	2.28	2.43	4.31	2.13
4x4	24	6	0.50	3.90	4.10	3.90	4.10	0.18	0.30	0.3	0.5	0.28	0.69	2.78	2.93	4.31	2.63
5x5	28	7	0.50	4.90	5.10	4.90	5.10	0.18	0.30	0.5	0.7	0.28	0.94	3.28	3.43	5.31	3.13
5x5	32	8	0.50	4.90	5.10	4.90	5.10	0.18	0.30	0.3	0.5	0.28	0.69	3.78	3.93	5.31	3.63
6x6	36	9	0.50	5.90	6.10	5.90	6.10	0.18	0.30	0.5	0.7	0.28	0.94	4.28	4.43	6.31	4.13
6x6	40	10	0.50	5.90	6.10	5.90	6.10	0.18	0.30	0.3	0.5	0.28	0.69	4.78	4.93	6.31	4.63
7x7	44	11	0.50	6.90	7.10	6.90	7.10	0.18	0.30	0.5	0.7	0.28	0.94	5.28	5.43	7.31	5.13
7x7	48	12	0.50	6.90	7.10	6.90	7.10	0.18	0.30	0.3	0.5	0.28	0.69	5.78	5.93	7.31	5.63
8x8	52	13	0.50	7.90	8.10	7.90	8.10	0.18	0.30	0.5	0.7	0.28	0.94	6.28	6.43	8.31	6.13
8x8	56	14	0.50	7.90	8.10	7.90	8.10	0.18	0.30	0.3	0.5	0.28	0.69	6.78	6.93	8.31	6.63
9x9	60	15	0.50	8.90	9.10	8.90	9.10	0.18	0.30	0.5	0.7	0.28	0.94	7.28	7.43	9.31	7.13
9x9	64	16	0.50	8.90	9.10	8.90	9.10	0.18	0.30	0.3	0.5	0.28	0.69	7.78	7.93	9.31	7.63
10x10	68	17	0.50	9.90	10.10	9.90	10.10	0.18	0.30	0.5	0.7	0.28	0.94	8.28	8.43	10.31	8.13
10x10	72	18	0.50	9.90	10.10	9.90	10.10	0.18	0.30	0.3	0.5	0.28	0.69	8.78	8.93	10.31	8.63
8x8	68	17	0.4	7.90	8.10	7.90	8.10	0.15	0.25	0.3	0.5	0.25	0.76	6.65	6.80	8.31	6.50
10x10	84	21	0.4	9.90	10.10	9.90	10.10	0.15	0.25	0.3	0.5	0.25	0.76	8.25	8.79	10.31	8.49
12x12	100	25	0.4	11.90	12.10	11.90	12.10	0.15	0.25	0.5	0.7	0.25	0.96	9.85	10.39	12.31	10.09

All Dimensions in mm

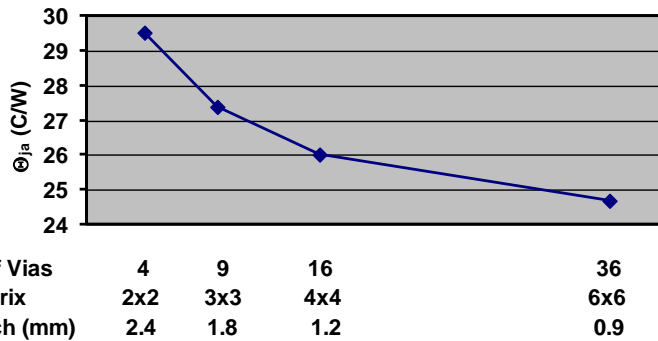
**Notes:**

**Xmax dimension reduced for 0.4 and 0.5mm pitch devices to avoid solder bridging.**

Refer to "Exposed Pad Variations" in the Package Outline Drawing for specific D2 and E2 dimensions.

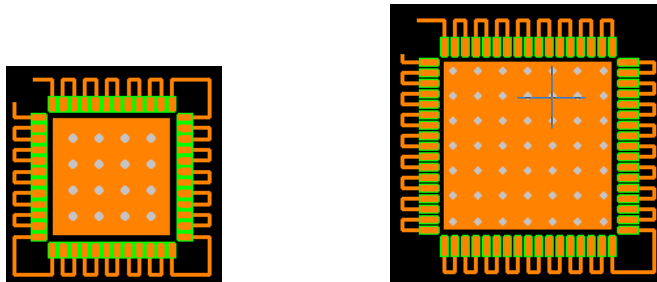
D2' should be equal to Component D2 or D2'<sub>TH</sub> max above, whichever is minimum.





**Figure 6: Effect of Number of Thermal Via on Package Thermal Performance.**

Based on this and similar thermal simulations, it is recommended that an array of thermal vias should be incorporated at 1.0 to 1.2mm pitch with via diameter of 0.3 to 0.33 mm. Representative of these arrays are shown in Figure 7 for 7x7mm, 48 lead and 10x10mm, 68 lead packages.



**Figure 7: PCB Thermal Pad and Via Array for 7x7mm, 48 Lead and 10x10mm, 68 lead Packages.**

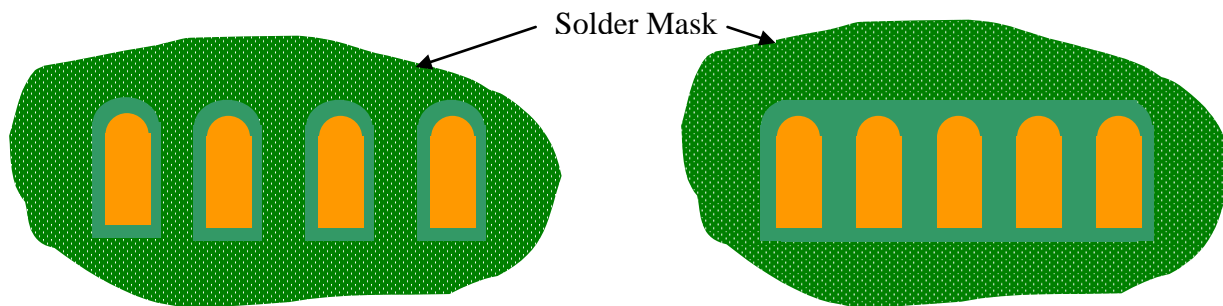
### 3.3 Solder Masking Considerations

The pads on the printed circuit board are either solder mask defined (SMD) or non solder mask defined (NSMD). Since copper etching process has tighter control than solder masking process, NSMD pads are preferred over SMD pads. Also, NSMD pads with solder mask opening larger than the metal pad size also improves the reliability of solder joints as solder is allowed to wrap around the sides of metal pads. Because of these reasons, NSMD pad is recommended for perimeter lands.

The solder mask opening should be 120 to 150 microns larger than the pad size resulting in 60 to 75 micron clearance between the copper pad and solder mask. This allows for solder mask registration tolerances, which are typically between 50 to 65 microns, depending upon the board fabricators' capabilities. Typically each pad on the PCB should have its own solder mask opening with a web of solder mask between two adjacent pads. Since the web has to be at least 75 microns in width for solder mask to stick to the PCB surface, each pad can have its own solder mask opening for lead pitch of 0.5mm or higher, based on the pad width dimensions given in Table 1. However, for 0.4mm pitch parts with PCB pad width of 0.25mm, not enough space is available for solder mask web in between the pads. In such cases, it is recommended to use "Trench" type solder mask opening where a big opening is designed around all pads on each side of the package with

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no solder mask in between the pads, as shown in Figure 8. It should also be noted that the inner edge of the solder mask should be rounded, especially for corner leads to allow for enough solder mask web in the corner area.



**Figure 8: Solder Mask Definition for Perimeter Lands; a) for 0.5mm and higher pitch parts, and b) for 0.4mm pitch parts.**

For the cases where thermal land dimension is close to the theoretical maximum discussed above, it is recommended that the thermal pad area should be solder mask defined in order to avoid any solder bridging between the thermal pad and the perimeter pads. The mask opening should be 100 microns smaller than the thermal land size on all four sides. This will guarantee a 25 microns solder mask overlap even for the worse case misregistration.

#### **4.0 Board Mounting Guidelines**

Because of the small lead surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for MLF® packages. This is further complicated by the large thermal pad underneath the package and its proximity to the inner edges of the leads. Although the pad pattern design suggested above might help in eliminating some of the surface mounting problems, special considerations are needed in stencil design and paste printing for both perimeter and thermal pads. Since surface mount process varies from company to company, careful process development is recommended. The following provides some guidelines for stencil design based on Amkor's experience in surface mounting MLF® packages.

#### **4.1 Stencil Design for Perimeter Pads**

The optimum and reliable solder joints on the perimeter pads should have about 50 to 75 microns (2 to 3 mils) standoff height and good side fillet on the outside. A joint with good standoff height but no or low fillet will have reduced life but may meet application requirement. The first step in achieving good standoff is the solder paste stencil design for perimeter pads. The stencil aperture opening should be so designed that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

$$\begin{aligned} \text{Area Ratio} &= \text{Area of Aperture Opening} / \text{Aperture Wall Area, and} \\ \text{Aspect Ratio} &= \text{Aperture width} / \text{Stencil Thickness} \end{aligned}$$

For rectangular aperture openings, as required for this package, these ratios are given as

$$\begin{aligned} \text{Area Ratio} &= LW / 2T(L+W), \text{ and} \\ \text{Aspect Ratio} &= W/T \end{aligned}$$

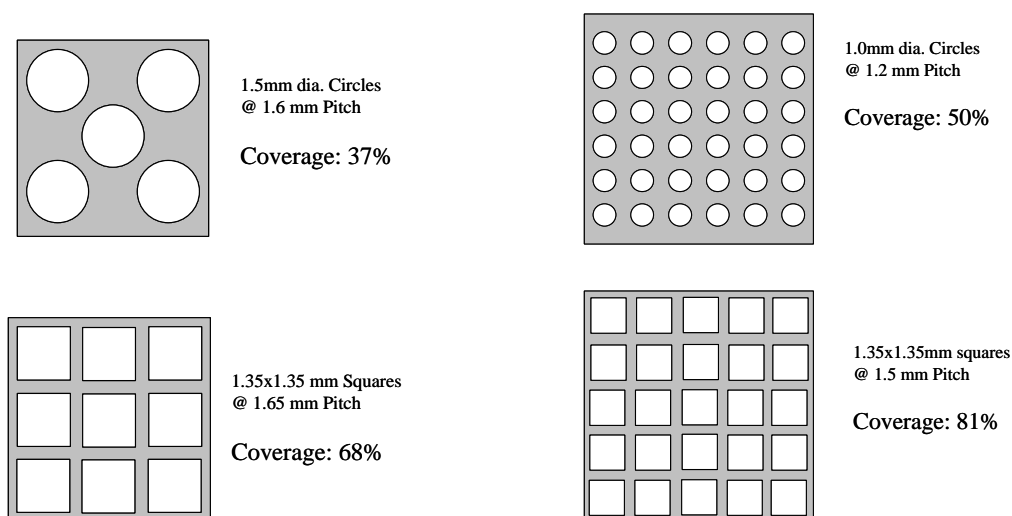
Where L and W are the aperture length and width, and T is stencil thickness. For optimum paste release the area and aspect ratios should be greater than 0.66 and 1.5 respectively.

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It is recommended that the stencil aperture should be 1:1 to PCB pad sizes as both area and aspect ratio targets are easily achieved by this aperture. The opening can be reduced for lead pullback option because of reduction of solderable area on the package. The stencil should be laser cut and electro polished. The polishing helps in smoothing the stencil walls which results in better paste release. It is also recommended that the stencil aperture tolerances should be tightly controlled, especially for 0.4 and 0.5mm pitch devices, as these tolerances can effectively reduce the aperture size.

## 4.2 Stencil Design for Thermal Pad

In order to effectively remove the heat from the package and to enhance electrical performance the die paddle needs to be soldered to the PCB thermal pad, preferably with minimum voids. However, eliminating voids may not be possible because of presence of thermal vias and the large size of the thermal pad for larger size packages. Also, out gassing occurs during reflow process which may cause defects (splatter, solder balling) if the solder paste coverage is too big. It is, therefore, recommended that smaller multiple openings in stencil should be used instead of one big opening for printing solder paste on the thermal pad region. This will typically result in 50 to 80% solder paste coverage. Shown in Figure 9 are some of the ways to achieve these levels of coverage.



**Figure 9: Thermal Pad Stencil Designs for 7x7 and 10x10mm MLF® Packages.**

## 4.3 Via types and solder voiding

Voids within solder joints under the exposed pad can have an adverse effect on high speed and RF applications as well as on thermal performance. As the MLF® package incorporates a large center pad, controlling solder voiding within this region can be difficult. Voids within this ground plane can increase the current path of the circuit. The maximum size for a void should be less than the via pitch within the plane. This recommendation would assure that any one via would not be rendered ineffectual based on any one void increasing the current path beyond the distance to the next available via.

With regards to voids in the thermal pad region, it should be emphasized that the presence of these voids is not expected to result in degradation of thermal and electrical performance. This is shown in Figure 10 where no loss in thermal performance is predicted from thermal simulation for smaller multiple voids covering up to 50% of thermal pad area. It should also be noted that the voids in thermal pad region do not impact the reliability of perimeter solder joints.

Although the percentage of voids may not be a big concern, large voids in thermal pad area should be avoided. In order to control these voids, solder masking may be required for thermal vias to prevent solder wicking inside the via during reflow, thus displacing the solder away from the interface between the package die paddle and thermal pad on the PCB. There are different methods employed within the industry for this purpose, such as “via tenting” (from top or bottom side) using dry film solder mask, “via plugging” with liquid photo-imagable (LPI) solder mask from the bottom side, or “via

encroaching”. These options are depicted in Figure 11. In case of via tenting, the solder mask diameter should be 100 microns larger than via diameter.

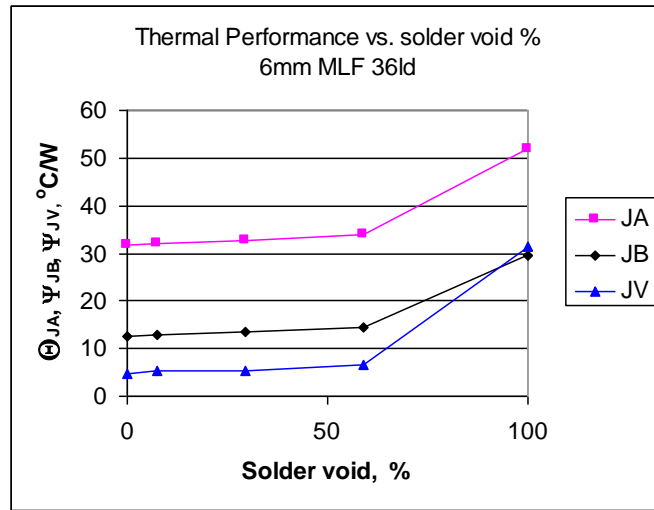


Figure 10: Effect of Voids on Thermal Performance.

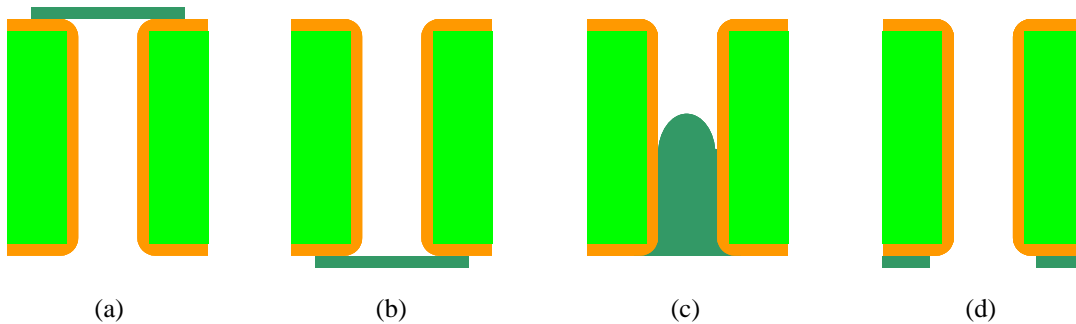


Figure 11: Solder mask options for thermal vias: (a) via tenting from top, (b) via tenting from bottom, (c) via plugging from bottom, and (d) via encroached from bottom.

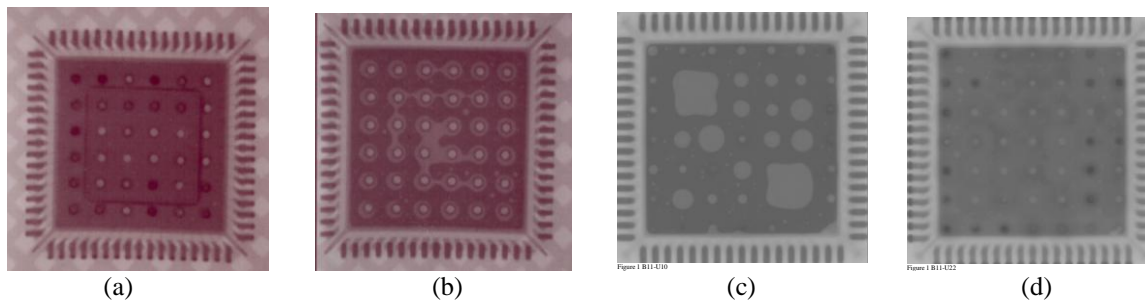


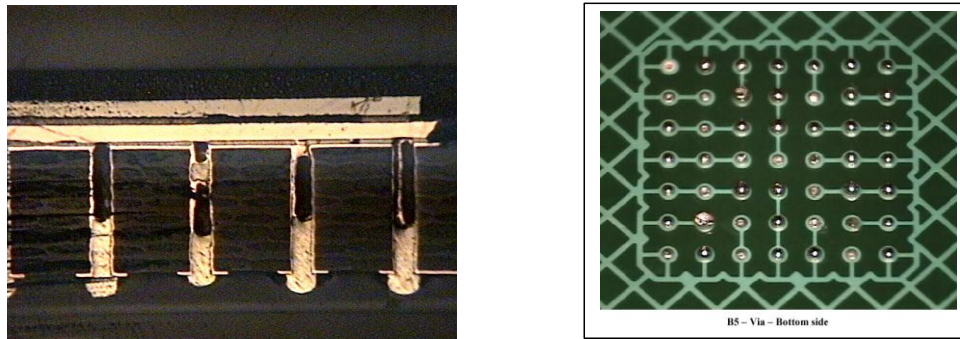
Figure 12: Voids in Thermal Pad Solder Joint for (a) vias tented from top, (b) vias tented from bottom, (c) via plugged from bottom, and (d) via encroached from bottom surface of the PCB.

All of these options have pros and cons when mounting MLF® package on the board. While via tenting from top side may result in smaller voids, the presence of solder mask on the top side of the board may hinder proper paste printing. On the other hand, both via tenting from bottom or via plugging from bottom may result in larger voids due to out-gassing,

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covering more than two vias. Finally, encroached vias allow the solder to wick inside the vias and reduce the size of the voids. However, it also results in lower standoff of the package, which is controlled by the solder underneath the exposed pad. Figure 12 shows representative x-ray pictures of MLF® packages mounted on boards with different via treatments.

Encroached via, depending on the board thickness and amount of solder printed underneath the exposed pad, may also result in solder protruding from the other side of the board, as shown in Figure 13. Note that the vias are not completely filled with solder, suggesting that solder wets down the via walls until the ends are plugged. This protrusion is a function of PCB thickness, amount of paste coverage in the thermal pad region, and the surface finish of the PCB. Amkor's experience is that this protrusion can be avoided by using lower volume of solder paste and reflow peak temperature of less than 215°C. If solder protrusion cannot be avoided, the MLF® components may have to be assembled on the top side (or final pass) assembly, as the protruded solder will impede acceptable solder paste printing on the other side of the PCB.



**Figure 13: Solder protrusion from the bottom side of PCB for encroached vias.**

#### **4.4 Stencil thickness and Solder Paste**

The stencil thickness of 0.125mm is recommended for 0.4 and 0.5mm pitch parts and can be increased to 0.15 – 0.2mm for coarser pitch parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

Since not enough space is available underneath the part after reflow, it is recommended that “No Clean”, Type 3 paste be used for mounting MLF® packages. Nitrogen purge is also recommended during reflow.

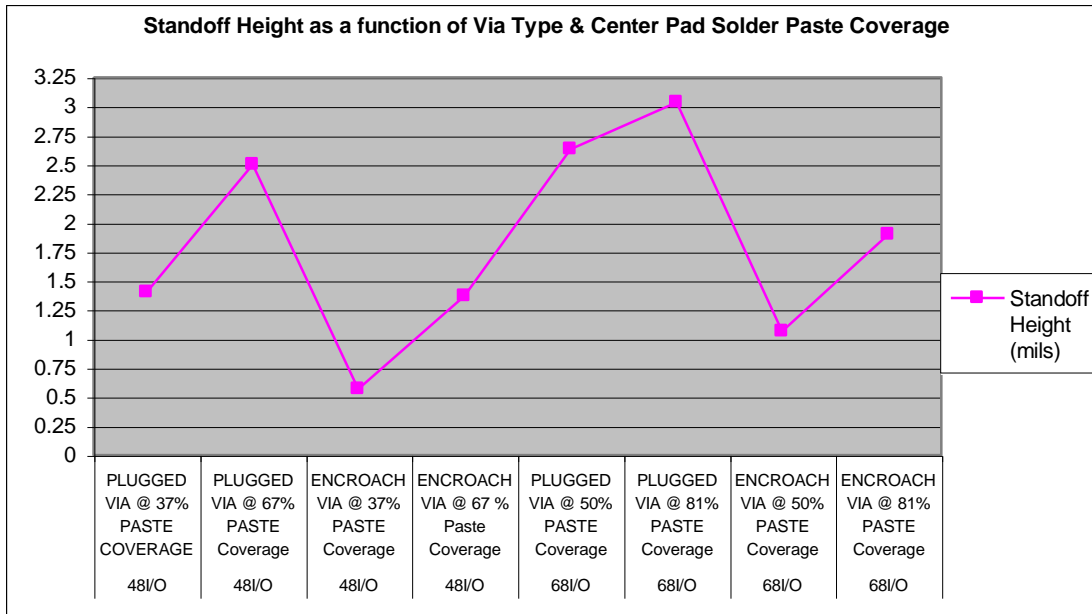
#### **4.5 Solder joint standoff height and fillet formation**

The solder joint standoff is a direct function of amount of paste coverage on the thermal pad and the type of vias used for MLF®s with exposed pad at the bottom. Board mounting studies sponsored by Amkor have clearly shown that the package standoff increases by increasing the paste coverage and by using plugged vias in the thermal pad region. This is shown in Figure 14 below.

The standoff height varies by the amount of solder that wets or flows into the PTH via. The encroached via provides an easy path for solder to flow into the PTH and decreases package standoff height while the plugged via impedes the flow of solder into the via due to the plugged via's closed barrel end. In addition, the number of vias and their finished hole size will also influence the standoff height for encroached via design. The standoff height is also affected by the type and reactivity of solder paste used during assembly, PCB thickness and surface finish, and reflow profile.

To achieve 50 micron thick solder joints, which help in improving the board level reliability, it is recommended that that the solder paste coverage be at least 50% for plugged vias and 75% for encroached via types.

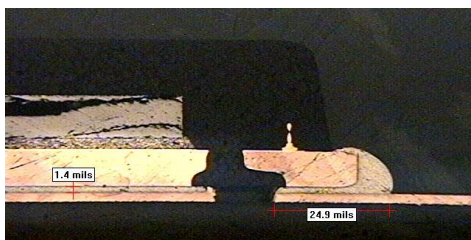
The peripheral solder joint fillets formation is also driven by multiple factors. It should be realized that only bottom surface of the leads are plated with solder and not the ends and the bare Cu on the side of the leads may oxidize if the packages are stored in uncontrolled environment. It is, however, possible that a solder fillet will be formed depending on the solder paste (flux) used and the level of oxidation.



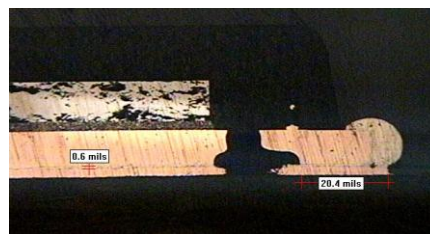
**Figure 14: Standoff height as a function of Via type and paste coverage**

The fillet formation is also a function of PCB land size, printed solder volume, and the package standoff height. The land size listed in Table 1 and 2 along with 1:1 aperture will provide sufficient solder for fillet formation if the package standoff is not excessive. Since there is only limited solder available, higher standoff - controlled by paste coverage on the thermal pad – may not leave enough solder for fillet formation. Conversely, if the standoff is too low, large convex shape fillets may form. This is shown in Figure 15.

Since center pad coverage and via type were shown to have the greatest impact on standoff height the volume of solder necessary to create optimum fillet varies. Package standoff height and PCB pads size will establish the required volume.

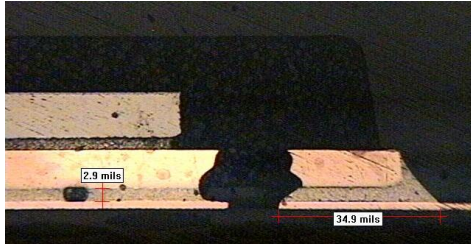


(a) 37% paste coverage, Plugged via, 1.4 mils standoff

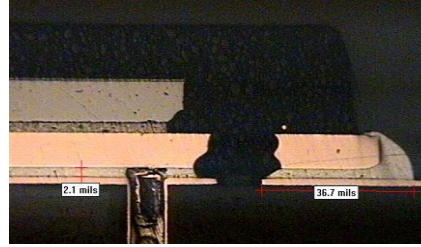


(b) 37% paste coverage, Encroached via, 0.6 mils standoff

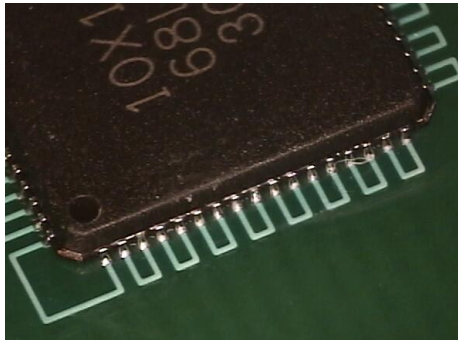




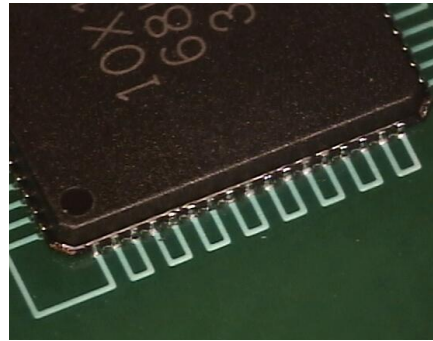
(c) 50% paste coverage, Plugged via, 2.9 mils standoff



(d) 81% paste coverage, Encroached via, 2.1 mils standoff



(e) large PCB pads, 81% paste coverage, plugged vias

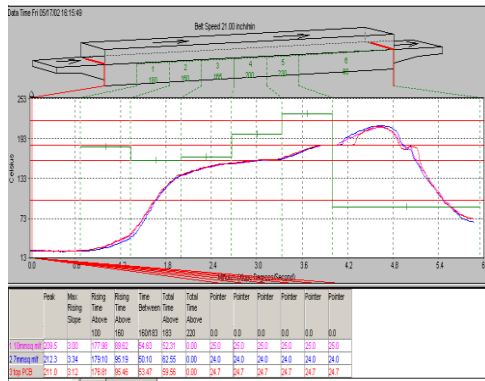


(f) small PCB pads, 81% paste coverage, plugged vias

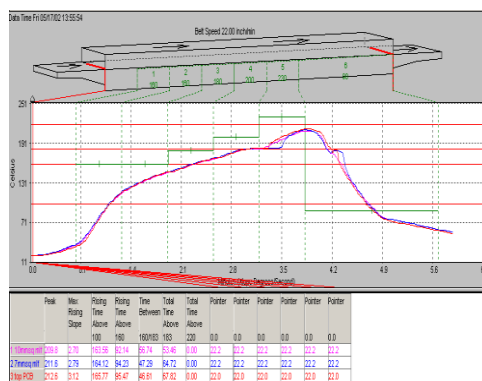
**Figure 15: Solder fillet shape as a function of paste coverage in the thermal pad, via type, standoff, and PCB land size**

#### 4.6 Reflow Profile

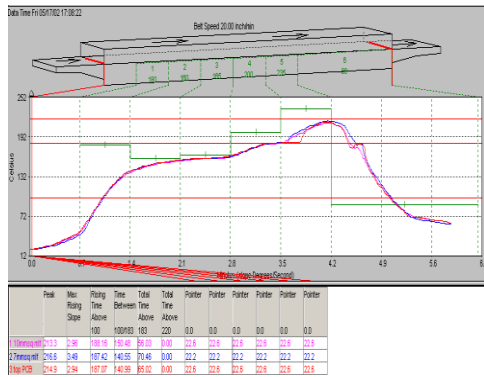
Reflow profile and peak temperature has a strong influence on void formation. Amkor has conducted experiments with different reflow profiles (ramp-to-peak vs. ramp-hold-ramp), peak reflow temperature, and time above liquids using Alpha Metal's UP78 solder paste. Some of the representative profiles are shown in Figure 16. Generally, it is found that the voids in the thermal pad region for plugged vias reduce as the peak reflow temperature is increased from 210 °C to 215 – 220 °C. For encroached vias, it is found that the solder extrusion from the bottom side of the board reduces as the reflow temperature is reduced.



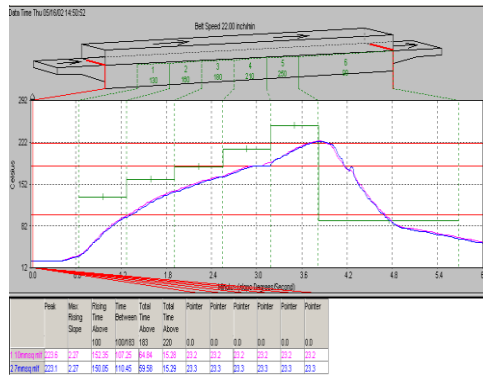
(a) Ramp-Soak-Spike – 210°C peak



(b) Ramp-Spike – 210°C peak



(c) Ramp-Soak-Spike – 215°C peak



(d) Ramp-Spike – 220°C peak

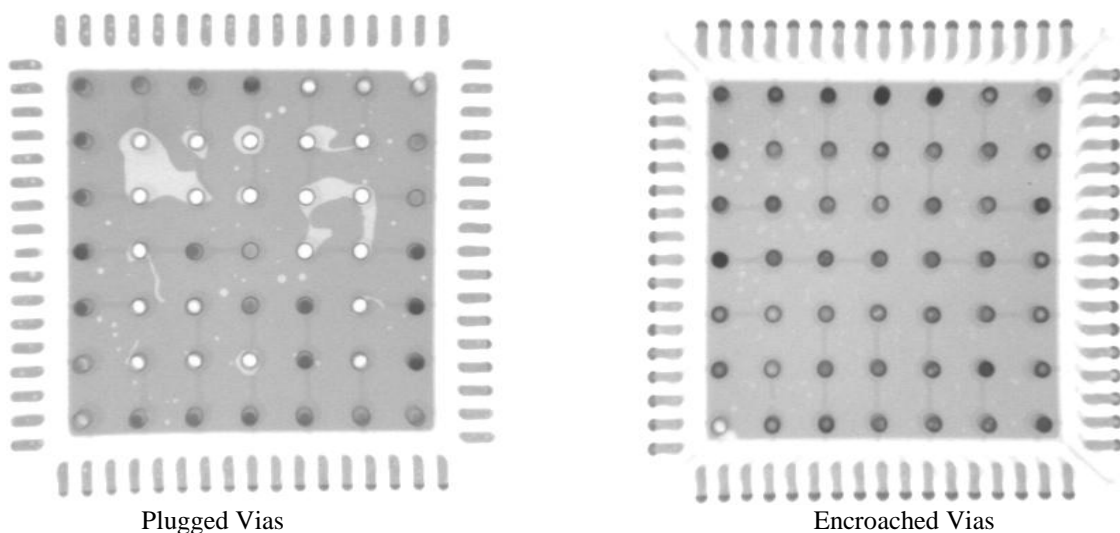
Figure 16: Various reflow profiles

### 5.0 NiPd and Matte Sn finish packages

As mentioned earlier, MLF® packages are available in three lead finishes: post plated SnPb and Matte Sn, and pre plated NiPd with flash of Au. Surface mount studies on parts plated with NiPd and Matte Sn show no significant difference compared to SnPb finish parts. It is generally found, however, that the reflow peak temperature may need to be increased to 215 °C for NiPd parts to reduce voids in the thermal pad region. Other than this factor, the trends seem to be the same as SnPb finished parts, i.e., more voids and higher standoff for plugged vias and less voids and lower standoff for encroached vias, as shown in Figure 17. The figure also shows that although the leads ends are not plated in NiPd finished parts either, solder fillets were still formed when these parts are mounted on the PCB with larger PCB pads and 1:1 aperture for peripheral leads.





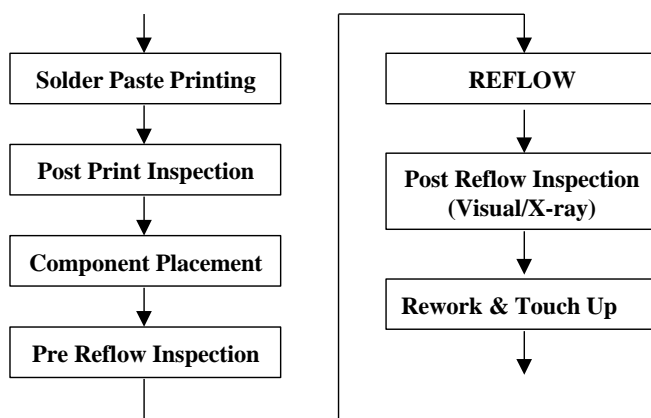


**Figure 17: Fillet formation and voids in thermal pad region for NiPd finish parts.**

## 6.0 Assembly Process Flow

Figure 18 shows the typical process flow for mounting surface mount packages to printed circuit boards. The same process can be used for mounting the MLF@s without any modifications. It is important to include post print and post reflow inspection, especially during process development. The volume of paste printed should be measured either by 2D or 3D techniques. The paste volume should be around 80 to 90% of stencil aperture volume to indicate good paste release. After reflow, the mounted package should be inspected in transmission x-ray for the presence of voids, solder balling, or other defects. Cross-sectioning may also be required to determine the fillet shape and size and joint standoff height.

Typical reflow profiles for No Clean solder paste are shown in Figure 16. Since the actual reflow profile depends on the solder paste being used and the board density, Amkor does not recommend a specific profile. However, the temperature should not exceed the maximum temperature the package is qualified for according to moisture sensitivity level. The time above liquidus temperature should be around 60 seconds and the ramp rate during preheat should be 3°C/second or lower.



**Figure 18: Typical PCB Mounting Process Flow.**

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## 7.0 Rework Guidelines

Since solder joints are not fully exposed in the case of MLF®s, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Rework of MLF® packages can be a challenge due to their small size. In most applications, MLF®s will be mounted on smaller, thinner, and denser PCBs that introduce further challenges due to handling and heating issues. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following only provides a guideline and a starting point for the development of a successful rework process for these packages.

The rework process involves the following steps:

- ❑ Component Removal
- ❑ Site Redress
- ❑ Solder Paste Application,
- ❑ Component Placement, and
- ❑ Component Attachment.

These steps are discussed in the following in more detail. Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125°C to remove any residual moisture from the assembly.

### 7.1 Component Removal

The first step in removal of component is the reflow of solder joints attaching component to the board. Ideally the reflow profile for part removal should be the same as the one used for part attachment. However, the time above liquidus can be reduced as long as the reflow is complete.

In the removal process, it is recommended that the board should be heated from the bottom side using convective heaters and hot gas or air should be used on the top side of the component. Special nozzles should be used to direct the heating in the component area and heating of adjacent components should be minimized. Excessive airflow should also be avoided since this may cause CSP to skew. Air velocity of 15 – 20 liters per minute is a good starting point.

Once the joints have reflowed, the Vacuum lift-off should be automatically engaged during the transition from reflow to cool down. Because of their small size the vacuum pressure should be kept below 15 inch of Hg. This will allow the component not to be lifted out if all joints have not been reflowed and avoid the pad liftoff.

### 7.2 Site Redress

After the component has been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and desoldering braid. The width of the blade should be matched to the maximum width of the footprint and the blade temperature should be low enough not to cause any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and paste manufacturer's recommendations should be followed.

### 7.3 Solder Paste Printing

Because of their small size and finer pitches, solder paste deposition for MLF®s requires extra care. However, a uniform and precise deposition can be achieved if miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50 to 100X magnification. The stencil should then be lowered onto the PCB and the paste should be deposited with a small metal squeegee blade. Alternatively, the mini stencil can be used to print paste on

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the package side also. A 125 microns thick stencil with aperture size and shape same as the package land should be used. Also, no-clean flux should be used, as small standoff of MLF@s does not leave much room for cleaning.

#### **7.4 Component Placement**

MLF® packages are expected to have superior self-centering ability due to their small mass and the placement of this package should be similar to that of BGAs. As the leads are on the underside of the package, split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. Again, the alignment should be done at 50 to 100X magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

#### **7.5 Component Attachment**

The reflow profile developed during original attachment or removal should be used to attach the new component. Since all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

Note) Sketch drawing in this application Notes is reference only. It May not represent all MLF application.

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