“GaNFast™ and GeneSiC™: Twin Engines Drive the Future of High-Power Applications”

Twin Engines

Navitas

GaN + SiC

Pure-Play, Next-Generation Power Semiconductors
• Characteristics of WBG (GaN & SiC) Devices
• Package-dependent thermal design comparisons
• Summary
GaNFast Delivers Value, Reliability, Low Cost

• Company founded in 2014
  o NASDAQ IPO Oct 2021 (NVTS)
  o #1 worldwide GaN supplier

• 650 V\textsubscript{DS} (800 V\textsubscript{PK}) lateral GaN-on-Si process
  o EMode (normally OFF) GaN power device
  o Zero \(Q_{\text{RR}}\) and \(E_{\text{ON}}/E_{\text{OFF}}\) much lower than Si or SiC

• Advanced monolithic integration capability
  o Regulated gate drive minimizes inductance & ringing
  o Logic and Protection functions fully-integrated
  o Enhanced Reliability not feasible in GaN discretes

Discrete GaN is Unprotected GaN

Excessive voltage stress degrades reliability and risks failure

Wide-range input (10~24 V)
Integrated regulation maintains \(V_{\text{GS}}\) within tolerance
200 V/ns Immunity
No inductance or ringing in gate loop
All GaNFast IC Pins have 2 kV HBM ESD

UVLO protection for circuitry and GaN power device

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Crosstalk issue caused by fast switching

- Typical half-bridge circuit and crosstalk waveforms

   ![Half bridge circuit](a)

- Root cause:
  - Fast switching and high dV/dt
  - Low Vth voltage of $V_{GS}$
  - Long drive loop brings the increase of parasitic parameters
  - Weak CMIT performance of the driver ICs

   ![Typical waveforms](b)

Benefits of Integration

- Component reliability, and system reliability

Silicon FET  →  Unprotected GaN  →  GaNFast™

- Old, slow
- High Q_g
- High C_{rss}
- F_{SW} < 100 kHz

- Exposed gate
- External gate drive
- dV/dt sensitivity
- Layout sensitivity
- ESD sensitivity
- Unknown reliability
- Unknown robustness

- Internal Gate
- Integrated Gate Drive
- dV/dt Immunity
- Layout Insensitive
- 2 kV ESD rating
- Proven Reliability
- Proven Robustness

GaNFast™ with GaNSense™

- Autonomous Standby Mode
- Lossless Current Sensing
- Over-Temperature Protection
- Autonomously Protected
- Autonomous Protection
- Lossless Current Sensing
- High Precision
- High Efficiency
GaNFast TOLL Device Characteristics

• Features:
  • TOLL (transistor outline, lead-less), 18 mΩ typical $R_{DS(ON)}$ @25°C
  • 12~18 V for DRIVE to SK
  • Integrated 5 V power supply unit. A typical 15 V drive voltage needs 30 ns for stability
  • Integrated level-shift and deglitch circuit for improved anti-interference performance
Patented Trench-Assisted Planar Gate SiC MOSFETs

Largest range of SiC FETs & diodes (650 V to 6.5 kV)

Lowest RDS(ON) at high temperature (25% lower than industry typical)

World-class survival duration in fault condition

Matching currents (Stable Vth)

Based on Navitas testing of 1200V SiC MOSFETs vs. competitor products

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**Broadest SiC FET Portfolio**

#### GeneSiC

**650–6,500V Trench-Assisted Planar SiC FETs**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>1000 mA</th>
<th>500 mA</th>
<th>100 mA</th>
<th>50 mA</th>
<th>10 mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>650V</td>
<td>⋅ 1000 mA ⋅</td>
<td>⋅ 450 mA ⋅</td>
<td>⋅ 160 mA ⋅</td>
<td>⋅ 45 mA ⋅</td>
<td>⋅ 12 mA ⋅</td>
</tr>
<tr>
<td>750V</td>
<td>* 1000 mA *</td>
<td>* 75 mA *</td>
<td>* 30 mA *</td>
<td>* 20 mA *</td>
<td>* 10 mA *</td>
</tr>
<tr>
<td>1200V</td>
<td>* 1000 mA *</td>
<td>* 75 mA *</td>
<td>* 40 mA *</td>
<td>* 20 mA *</td>
<td>* 10 mA *</td>
</tr>
<tr>
<td>1700V</td>
<td>* 1000 mA *</td>
<td>* 50 mA *</td>
<td>* 50 mA *</td>
<td>* 20 mA *</td>
<td>* 10 mA *</td>
</tr>
</tbody>
</table>

#### GeneSiC

**Most 1,700V SiC FETs**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>1000 mA</th>
<th>500 mA</th>
<th>100 mA</th>
<th>50 mA</th>
<th>10 mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000 mA</td>
<td>⋅ 1000 mA ⋅</td>
<td>⋅ 450 mA ⋅</td>
<td>⋅ 160 mA ⋅</td>
<td>⋅ 45 mA ⋅</td>
<td>⋅ 12 mA ⋅</td>
</tr>
<tr>
<td>750V</td>
<td>* 1000 mA *</td>
<td>* 75 mA *</td>
<td>* 40 mA *</td>
<td>* 20 mA *</td>
<td>* 10 mA *</td>
</tr>
<tr>
<td>1200V</td>
<td>* 1000 mA *</td>
<td>* 50 mA *</td>
<td>* 50 mA *</td>
<td>* 20 mA *</td>
<td>* 10 mA *</td>
</tr>
<tr>
<td>1700V</td>
<td>* 1000 mA *</td>
<td>* 75 mA *</td>
<td>* 64 mA *</td>
<td>* 41 mA *</td>
<td>* 20 mA *</td>
</tr>
</tbody>
</table>

- 50+ SiC MOSFETs, array of standard packages
- Only supplier with 650V to 6,500V SiC MOSFETs

- Broadest industry offering for 1700V SiC MOSFETs

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1) based on GeneSiC voltage range of production released SiC MOSFETs compared to all publicly identified voltage ranges of other SiC suppliers.
# Best High-Speed, High-Temp Performance

## Table of Performance Metrics

<table>
<thead>
<tr>
<th>Supplier</th>
<th>Resistance</th>
<th>Energy Loss</th>
<th>Figure-of-Merit (Low number is better)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R_{DS(ON)}@25°C$ (mΩ)</td>
<td>$R_{DS(ON)}@175°C$ (mΩ)</td>
<td>$E_{ON}@25A$ (µJ)</td>
</tr>
<tr>
<td>GeneSiC</td>
<td>40</td>
<td>57</td>
<td>600</td>
</tr>
<tr>
<td>#2</td>
<td>40</td>
<td>68</td>
<td>600</td>
</tr>
<tr>
<td>#3</td>
<td>40</td>
<td>80</td>
<td>850</td>
</tr>
<tr>
<td>#4</td>
<td>40</td>
<td>71</td>
<td>550</td>
</tr>
<tr>
<td>#5</td>
<td>45</td>
<td>85</td>
<td>520</td>
</tr>
</tbody>
</table>

Lowest power loss at high temp, high speed = Highest Efficiency, Energy Savings Small Size, Light Weight, Low System Costs!

Reference 1,200V SiC FET, 40-45mΩ devices; GeneSiC = Trench-Assisted Planar G3R40MT12J; based on Navitas test result & competitive data sheet parameters.
Faster, Cooler, Longer Lifetime

- GeneSiC trench-assisted planar FET vs. Competitor SiC FET
  - 1,200 V, 40 mΩ, D2pak in half-bridge
  - Represents 7.5 kW DC-DC converter (e.g. data center, EV)
  - 150 kHz switching = ~10x faster than Si IGBT example

- GeneSiC: >80% energy savings (>3,000 kWh/yr) vs Si IGBTs
  - -25°C cooler = 3x longer life vs other SiC
    (reduced maintenance / repair costs)

Test Board

7.5 kW
150 kHz SiC
Test Board

Switching Waveforms
(40 A pk-pk, 20 A turn-off)

Competitor SiC
45 W system loss

GeneSiC
40 W system loss
-30% SiC loss

Thermal Camera

GeneSiC 98°C
Competitor 124°C

Test Circuit
(1-phase of 3-phase motor drive)
High Quality, High Reliability

100%-Tested Avalanche
Highest published capability to handle excess energy in fault condition

Critical in applications like motor drives to withstand unclamped inductive load (UIL) energy dump in situations like motor open-circuit (O.C.)

High Power Paralleling
Matching currents (Stable $V_{TH}$)

Competitor products allow threshold voltage to drop under high voltage, creating risk of turn-on error

GeneSiC packaged and bare-die FETs can be paralleled reliably for high-power applications

Long Short-Circuit Withstand Time
World-class survival duration in fault condition

Critical to prevent failures like motor short circuit where the FET faces full voltage ($V_{DD}$) in ON-state.

GeneSiC

3x Stronger

Competitor

$\begin{array}{c}
\text{GeneSiC} \\
\text{Comp.}
\end{array}$

Avalanche Energy (100% tested, norm.) (2)

0.5 1 1.5 2 2.5 3

$\begin{array}{c}
\text{GeneSiC} \\
\text{Comp. A} \\
\text{Comp. B}
\end{array}$

Short-Circuit Withstand Time (µs) (2)

4 4.25 4.5 4.75 5 5.25 5.5 5.75

Zero reported GeneSiC-related field failures!

1) As of September '23, per GeneSiC records
2) 1,200 V, 20 mΩ FET

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• Characteristics of WBG (GaN & SiC) Devices
• Package-dependent thermal design comparisons
• Summary
Challenges for the packaging and thermal design

• With GaN/SiC die shrink, the package is also reduced, which saves footprint but brings challenges of the heat dissipation
• The design of system heat dissipation becomes very important in practical applications

GaN Systems GS61008P vertical cross-section (source: EETOP)
Full-bridge Eval Board and Test Platform

- DEMO board Top view
- DEMO board Bottom view
- Side view
- Top view

Full-bridge circuit

Drive circuit
## Review: Heat Dissipation TIMS

<table>
<thead>
<tr>
<th>Bonded Copper (BC)</th>
<th>GAP-FILLER</th>
<th>Thermal pad</th>
<th>Sil-pad</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{AL}_2\text{O}_3 )</td>
<td>( \text{ALN} )</td>
<td>CR350</td>
<td>Tgard-K52-2</td>
</tr>
<tr>
<td>Specification</td>
<td>0.63 mm, 96% ( \text{AL}_2\text{O}_3 ) + 0.3 mm, 99.99%, Cu</td>
<td>0.63 mm, ALN + 0.3 mm, 99.99%, Cu</td>
<td>Thermal glue (0.8 mm)</td>
</tr>
<tr>
<td>Thermal conductivity (W/m.k) or Resistance</td>
<td>&gt;24</td>
<td>&gt;170</td>
<td>3.6</td>
</tr>
<tr>
<td>Dielectric strength-AC (KV/mm)</td>
<td>&gt;20</td>
<td>&gt;20</td>
<td>&gt;9</td>
</tr>
<tr>
<td>Coefficient of Thermal Expansion (x10^-6/K)</td>
<td>6.8 (20°C~300°C)</td>
<td>4.7 (20°C~300°C)</td>
<td>N/P</td>
</tr>
<tr>
<td>Cost Contains Two devices (¥)</td>
<td>2.5</td>
<td>12</td>
<td>1.41</td>
</tr>
<tr>
<td>Cost</td>
<td>16</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Review: TOLL Thermal Designs

- **Case 1**
  - Toll devices
  - Solder
  - Copper inlay
  - Solder
  - Copper of DBC
  - Ceramic
  - Copper of DBC
  - TIM
  - Cold plate

- **Case 2**
  - Toll devices
  - Solder
  - Copper inlay
  - Solder
  - Copper of DBC
  - TIM

- **Case 3**
  - Toll devices
  - Solder
  - Copper inlay
  - Solder
  - Copper of DBC
  - TIM

- **Case 4**
  - Toll devices
  - Solder
  - Copper inlay
  - Solder
  - Copper of DBC
  - TIM

- **Case 5**
  - Toll devices
  - Solder
  - Copper inlay
  - TIM
  - Dielectric layer

- 5 practical application conditions for analysis.
**TOLL Simulation Results**

- 25 W Loss pre devices
- 65°C coolant water
- 85°C ambient temperature
- $T_j$ design target is 125°C

<table>
<thead>
<tr>
<th></th>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
<th>Case 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layers</td>
<td>T (°C)</td>
<td>Layers</td>
<td>T (°C)</td>
<td>Layers</td>
</tr>
<tr>
<td>Die</td>
<td>102.09</td>
<td>Die</td>
<td>112.07</td>
<td>Die</td>
</tr>
<tr>
<td>Die attach</td>
<td>100.59</td>
<td>Die attach</td>
<td>110.5</td>
<td>Die attach</td>
</tr>
<tr>
<td>Exposed Pad</td>
<td>100.16</td>
<td>Exposed Pad</td>
<td>110.06</td>
<td>Exposed Pad</td>
</tr>
<tr>
<td>Solder</td>
<td>97.907</td>
<td>Solder</td>
<td>107.81</td>
<td>Solder</td>
</tr>
<tr>
<td>Copper Inlay</td>
<td>96.976</td>
<td>Copper Inlay</td>
<td>106.88</td>
<td>Copper Inlay</td>
</tr>
<tr>
<td>Solder</td>
<td>93.906</td>
<td>TIM</td>
<td>103.81</td>
<td>Copper Inlay</td>
</tr>
<tr>
<td>DBC Cu Top Layer</td>
<td>93.586</td>
<td>DBC Cu Top Layer</td>
<td>92.555</td>
<td>DBC Cu Top Layer</td>
</tr>
<tr>
<td>DBC Al₂O₃ Layer</td>
<td>93.34</td>
<td>DBC Al₂O₃ Layer</td>
<td>92.301</td>
<td>DBC Al₂O₃ Layer</td>
</tr>
<tr>
<td>0.12 mm TIM</td>
<td>86.43</td>
<td>0.12 mm TIM</td>
<td>85.442</td>
<td>0.12 mm TIM</td>
</tr>
<tr>
<td>Cold Plate</td>
<td>81.563</td>
<td>Cold Plate</td>
<td>80.662</td>
<td>Cold Plate</td>
</tr>
<tr>
<td>Coolant</td>
<td>65</td>
<td>Coolant</td>
<td>65</td>
<td>Coolant</td>
</tr>
</tbody>
</table>

- Case 1 is the best thermal solution for the Toll packaging.
## TOLL System Thermal Resistance

### Thermal resistance: \( R_{th} = \Delta T / \Delta P \)

<table>
<thead>
<tr>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
<th>Case 4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Layers</strong></td>
<td><strong>Rth (°C/W)</strong></td>
<td><strong>Layers</strong></td>
<td><strong>Rth (°C/W)</strong></td>
</tr>
<tr>
<td>R_Die</td>
<td>0.06</td>
<td>R_Die</td>
<td>0.0628</td>
</tr>
<tr>
<td>R_Die attach</td>
<td>0.0172</td>
<td>R_Die attach</td>
<td>0.0176</td>
</tr>
<tr>
<td>R_Exposed Pad</td>
<td>0.09012</td>
<td>R_Exposed Pad</td>
<td>0.09</td>
</tr>
<tr>
<td>R_jc</td>
<td>0.16732</td>
<td>R_jc</td>
<td>0.1704</td>
</tr>
<tr>
<td>R_Solder</td>
<td>0.03724</td>
<td>R_Solder</td>
<td>0.0372</td>
</tr>
<tr>
<td>R_Copper Inlay</td>
<td>0.1228</td>
<td>R_Copper Inlay</td>
<td>0.1228</td>
</tr>
<tr>
<td>R_Solder</td>
<td>0.0128</td>
<td>R_Solder</td>
<td>0.1228</td>
</tr>
<tr>
<td>R_DBC Cu Top Layer</td>
<td>0.00984</td>
<td>R_DBC Cu Top Layer</td>
<td>0.01016</td>
</tr>
<tr>
<td>R_DBC Al₂O₃ Layer</td>
<td>0.26984</td>
<td>R_DBC Al₂O₃ Layer</td>
<td>0.268</td>
</tr>
<tr>
<td>R_DBC Cu Bot. Layer</td>
<td>0.00656</td>
<td>R_DBC Cu Bot. Layer</td>
<td>0.00636</td>
</tr>
<tr>
<td>R_0.12mm TIM</td>
<td>0.19468</td>
<td>R_0.12mm TIM</td>
<td>0.1912</td>
</tr>
<tr>
<td>R_Cold Plate</td>
<td>0.66252</td>
<td>R_Cold Plate</td>
<td>0.62648</td>
</tr>
<tr>
<td>R_coolant</td>
<td>1.4836</td>
<td>R_coolant</td>
<td>1.8828</td>
</tr>
</tbody>
</table>

- **Case 1** has the lower thermal resistance than others.
**System Thermal Resistance Verification**

- Q1 & Q2 short circuit.
- \( V_{IN} = 3 \text{ V}, \ I_{IN} = 31.2 \text{ A} \)
- \( V_{DS1} = 0.764 \text{ V}, \ V_{DS2} = 0.756 \text{ V} \)

### Measured Temperature and Calculated Thermal Resistance

<table>
<thead>
<tr>
<th>Device NO.</th>
<th>Temperature</th>
<th>Loss</th>
<th>Thermal Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>56.54 °C</td>
<td>23.82 W</td>
<td>1.32 °C / W</td>
</tr>
<tr>
<td>Q2</td>
<td>54.81 °C</td>
<td>23.57 W</td>
<td>1.26 °C / W</td>
</tr>
</tbody>
</table>

**Simulation Result:**

- Q1 & Q2 short circuit.
- \( V_{IN} = 3 \text{ V}, \ I_{IN} = 31.2 \text{ A} \)
- \( V_{DS1} = 0.764 \text{ V}, \ V_{DS2} = 0.756 \text{ V} \)

- Measured device temperature is **CASE** temperature (\( T_{CASE} \))
- Device loss is calculated by: \( P = VDS \cdot Iin \)
- Since the temperature of junction cannot be directly obtained during the actual test, the thermal resistance of the test is smaller than that of the simulation.
TOLL Thermal Model Available

- Transient thermal resistance

![Graph showing thermal resistance vs pulse duration](image)

- Transient $T_j$ simulation for PFC stage

<table>
<thead>
<tr>
<th>$R_{th}$ ($^\circ C/W$)</th>
<th>$C_{th} (W*^\circ C)$</th>
<th>$T$ (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7.858E-03</td>
<td>6.068E-03</td>
</tr>
<tr>
<td>2</td>
<td>5.064E-02</td>
<td>6.609E-03</td>
</tr>
<tr>
<td>3</td>
<td>1.000E-06</td>
<td>2.861E+00</td>
</tr>
<tr>
<td>4</td>
<td>2.028E-01</td>
<td>1.214E-02</td>
</tr>
</tbody>
</table>

Foster model
### Review: Bottom-Side Cooling per Package

<table>
<thead>
<tr>
<th>Packaging</th>
<th>TOLL</th>
<th>PSOP-30L</th>
<th>SOIC-22L</th>
<th>D2PACK</th>
<th>CCPACK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exposed Pad Area (mm²)</td>
<td>60.52</td>
<td>96.52</td>
<td>37.4</td>
<td>49.92</td>
<td>60.56</td>
</tr>
<tr>
<td>Device $R_{j_C}$ (°C/W)</td>
<td>0.174</td>
<td>0.203</td>
<td>0.113</td>
<td>0.816</td>
<td>0.146</td>
</tr>
<tr>
<td>Copper inlay (mm)</td>
<td>5*10</td>
<td>7*12</td>
<td>4*11.5</td>
<td>6.5*10.5</td>
<td>6*12.5</td>
</tr>
<tr>
<td>Copper inlay Area (mm²)</td>
<td>50</td>
<td>84</td>
<td>46</td>
<td>68.25</td>
<td>75</td>
</tr>
<tr>
<td>Length of Pin-Fin base (mm)</td>
<td>62</td>
<td>70</td>
<td>70</td>
<td>70</td>
<td>70</td>
</tr>
</tbody>
</table>

- Each packaging corresponding different thermal solution (Case1 to Case5).
### Simulation Results of $T_j$ @ 25 W Power Loss

<table>
<thead>
<tr>
<th>Case</th>
<th>Description</th>
<th>TOLL</th>
<th>PSOP-30L</th>
<th>SOIC-22L</th>
<th>D2PACK</th>
<th>CCPACK</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(Solder + DBC + 0.12mm Gap-Filler)</td>
<td>$T_j=101.8^\circ$C</td>
<td>$T_j=96.88^\circ$C</td>
<td>$T_j=101.1^\circ$C</td>
<td>$T_j=112.5^\circ$C</td>
<td>$T_j=98.66^\circ$C</td>
</tr>
<tr>
<td>2</td>
<td>(0.12mm Gap-Filler + DBC + 0.12mm Gap-Filler)</td>
<td>$T_j=111.8^\circ$C</td>
<td>$T_j=103.53^\circ$C</td>
<td>$T_j=112.74^\circ$C</td>
<td>$T_j=121.18^\circ$C</td>
<td>$T_j=106.5^\circ$C</td>
</tr>
<tr>
<td>3</td>
<td>(0.8mm Gap-Filler)</td>
<td>$T_j=129.6^\circ$C</td>
<td>$T_j=116.7^\circ$C</td>
<td>$T_j=129.85^\circ$C</td>
<td>$T_j=137.51^\circ$C</td>
<td>$T_j=121.87^\circ$C</td>
</tr>
<tr>
<td>4</td>
<td>(0.203mm Sil-Pad)</td>
<td>$T_j=136.6^\circ$C</td>
<td>$T_j=122.12^\circ$C</td>
<td>$T_j=136.62^\circ$C</td>
<td>$T_j=144.38^\circ$C</td>
<td>$T_j=127.89^\circ$C</td>
</tr>
<tr>
<td>5</td>
<td>(2oz-Cu/150-micron dielectric layer/3mm-Al5052H32)</td>
<td>$T_j=113.25^\circ$C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- TOLL and SOIC-22L packaging have the same heat-dissipation capability.
### $R_{th}$ Comparison (Bottom side cooling)

<table>
<thead>
<tr>
<th>Case</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>Solder + DBC + 0.12mm Gap-Filler</td>
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<tr>
<td>Case 2</td>
<td>0.12 mm Gap-Filler + DBC + 0.12 mm Gap-Filler</td>
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<tr>
<td>Case 3</td>
<td>0.8 mm Gap-Filler</td>
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<tr>
<td>Case 4</td>
<td>0.203 mm Sil-Pad</td>
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<tr>
<td>Case 5</td>
<td>2 oz-Cu, 150 um dielectric layer, 3 mm-Al5052H32</td>
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</tbody>
</table>

#### Conditions:
- Same die size
- Bottom-side cooling device
- 25 W loss per device

- TOLL and SOIC-22L packaging have the same heat dissipation capability
- PSOP-30L has the best heat capability but larger PCB area
3-in-1 Bi-Directional OBC + DC-DC

- Bi-Directional 6.6kW OBC/3kW DC-DC combo
- Optimized design with 650 V GaN and 1200 V SiC

AC-DC + DC-AC + DC-DC
• Navitas’ Shanghai EV System Design Center:
  • Optimized Magnetic designs, higher $F_{SW}$
  • Optimized system and component thermal design
• Achieves:
  • Higher efficiency
  • Higher power density
  • Lower weight
  • *Faster time-to-market*
Summary

- GaNFast power ICs and GeneSiC MOSFETs enable high frequency, high efficiency, higher power density
- Small die size and package size bring thermal challenges for high-power applications
- Copper inlay technology is an effective method for bottom-side cooling
- Packaging types are reviewed, and thermal designs analyzed
- Results show that DBC heat insulation technology is the best strategy
- NVTS roadmap includes TOLL and more package types for different high-power applications
“GaNFast™ and GeneSiC™: Twin Engines Drive the Future of High-Power Applications”

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