Who Needs Avalanche?

GaNFast Power ICs maximize transient voltage ratings and boost circuit ruggedness

Introduction

Traditional Silicon high voltage power MOSFETs have maximum voltage ratings that include maximum allowable avalanche energy levels. Avalanche breakdown limits the robustness and reliability of the power MOSFET due to the rapid and uncontrolled increase in current and the absorption of the transient or surge energy by the switch itself. GaNFast Power ICs do not have this avalanche breakdown effect so they can withstand higher transient voltage spikes and ride-through transient conditions without absorbing any of the surge energy. This article explains the avalanche effect in silicon, how GaNFast Power ICs high blocking voltage behavior works, and compares V_{DSmax} ratings for Silicon, GaN IC, and discrete GaN technologies for continuous and transient conditions.

Avalanche! Look Out Below!

The Avalanche effect is exactly as it sounds. Just like a small snowslide can trigger a chain reaction of collisions causing massive amounts of snow to flow rapidly down a mountain, avalanche in a MOSFET occurs when the drain voltage exceeds the maximum breakdown voltage limit (BV_{DSS}). The high electric field accelerates carriers in the device that causes a chain reaction of collisions of carriers with atoms. This uncontrolled chain reaction causes the current flowing through the device to multiply suddenly. The resulting high current causes a rapid temperature rise within the silicon and ultimately leads to the destruction of the silicon device. This is a well-known and well-characterized weakness of silicon MOSFETs and has resulted in a maximum avalanche energy rating (typically in millijoules) that the device can withstand when its drain-source voltage exceeds the BV_{DSS} limit. This rating is for a single-event only and it is encouraged by silicon MOSFET manufacturers to avoid this condition completely by using external methods such as snubbers and varistors to limit the voltage below the breakdown limit.

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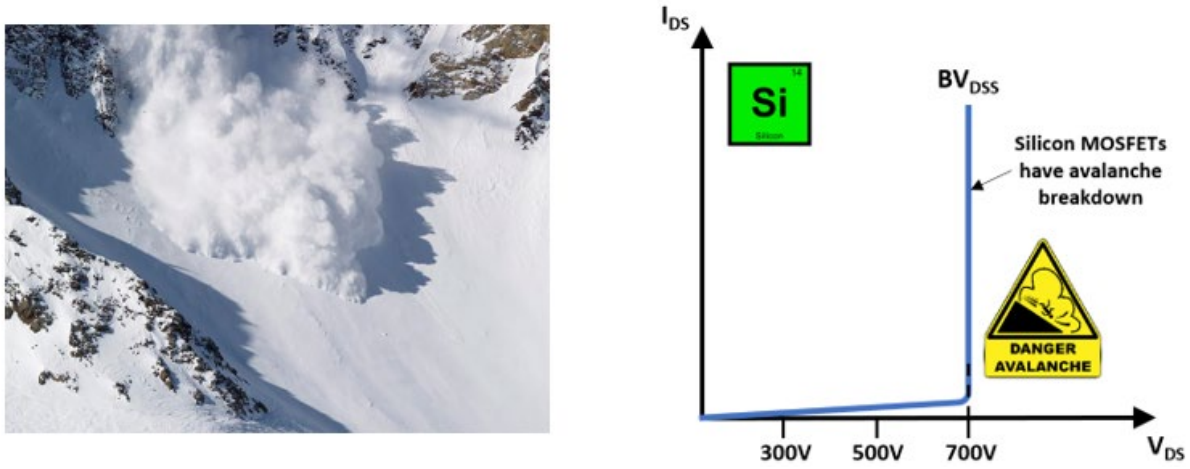

Fig. 1, Silicon MOSFET avalanche breakdown effect

The amount of avalanche energy depends on the amplitude and duration of the voltage spike that is being clamped by the silicon device. When using a switched inductive test circuit (Figure 2), the switch is turned on to charge up the inductor to a desired level (I_{AS}) and then turned off to allow the voltage across the switch to ring up and exceed BV_{DSS}. The MOSFET then enters avalanche, clamps the voltage to the BV_{DSS} level, and the inductor current discharges into the drain. For silicon device with a 700V BV_{DSS} rating, for example, and 100 µsec avalanche duration time with 10 A inductor current, the avalanche energy = 0.5 x (700V_{DS}-50V_{DD}) x 10A x 100us = 325 mJ! Already from this simple example we can see that avalanche breakdown can generate enormous amounts of energy in a very short amount of time. Also, since this time duration is very short, the heat generated from this energy does not have time to flow out of the package and to the PCB so the device will heat up very quickly to very high temperatures (> 200C)! Also, this example is only for a single avalanche event (at starting Tj = 25C) so the device has time to cool back down before the next event. For repetitive avalanche events, the device temperature will continue to rise and eventually thermally destruct.

The silicon FET also includes a parasitic BJT that can self-turn-on during avalanche causing latch-up failures. Silicon MOSFET manufacturers have gone to great lengths to characterize their devices and provide maximum avalanche ratings in an effort to work-around this inherent device weakness. But when the device is in the field, the actual surge voltage, current, time duration and no. of events (and resulting avalanche energy and device temperature) are all highly unpredictable. This places the robustness and reliability of the silicon device at high risk.

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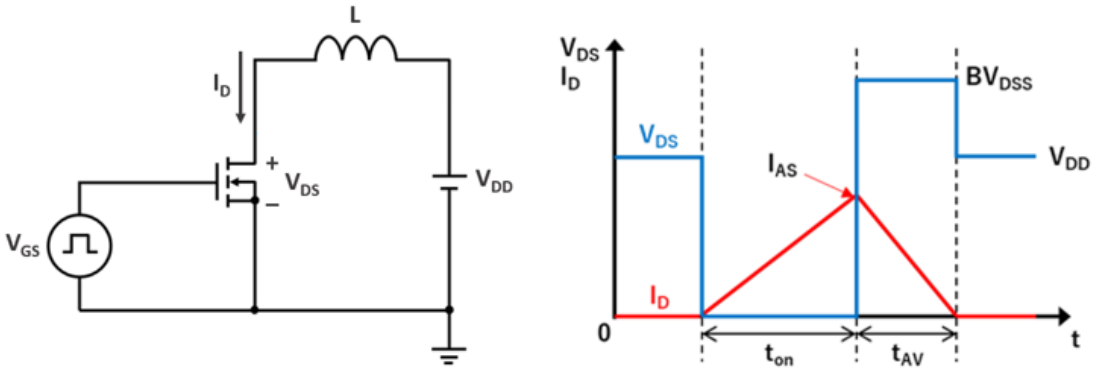

Fig. 2, Silicon MOSFET avalanche unclamped inductive test circuit and waveforms

No Avalanche, No Problem!

While Si devices have avalanche breakdown which limits their absolute maximum rating, GaNFast Power ICs do not have an intrinsic p-n junction for voltage blocking. As the drain voltage increases, they behave more like an insulator and will continue to increase in leakage well beyond the absolute maximum rating (Figure 3). This intrinsic behavior enables GaNFast Power ICs to continue switching through surge events or during circuit ringing or overshooting instead of avalanching. For a typical IEC61000-4-5 AC line surge condition, a 2 kV voltage spike can occur at the AC mains input that lasts 50usec (half-value decay time). Some of this surge energy is absorbed by the input EMI filter and DC bus capacitor. The remaining energy can still increase the DC bus capacitor from 400V up to levels around 700V. The switched node of a half-bridge DC/DC circuit, for example, should withstand this voltage and ride-through the surge condition. For good margin, GaNFast ICs have an 800V $V_{DS(TRAN)}$ peak transient voltage rating, and each IC is tested at higher voltages (up to 1000 V) during production to ensure excellent robustness in the field.

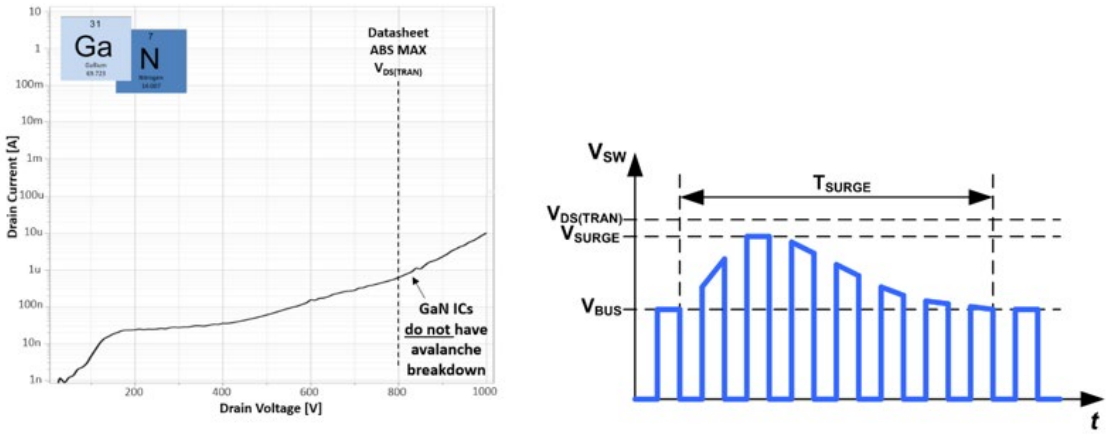

Fig. 3, GaNFast Power ICs do not have avalanche breakdown and can ride through voltage surges

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Over 3.5 Billion Spikes!

Navitas GaNFast ICs have undergone extensive robustness and reliability testing. For transient voltage spike testing, the maximum drain voltage is pulsed repetitively to a level of 800 V for a duration of 100 µsec (Figure 4). This is repeated every 2 msec for 2000 hours = 3,600,000,000 spikes! After testing, the GaN ICs are rescreened and show no change in functionality or any electrical parameters versus pre-test conditions. These results further reinforce the ruggedness of GaNFast ICs and their ability to withstand and ride through high voltage surge conditions.

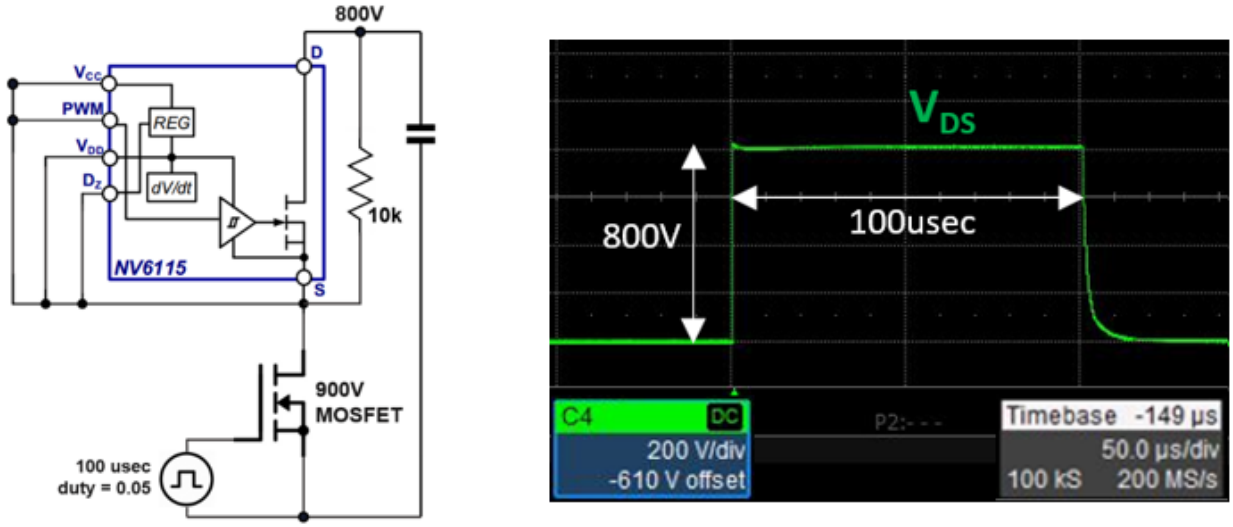

Fig. 4, GaNFast Power ICs voltage spike test circuit and VDS waveform

Continuous Ratings Matter!

In addition to the $V_{DS(TRAN)}$ rating for surge voltage immunity, the maximum VDS continuous rating, $V_{DS(CONT)}$, is also important for blocking repetitive circuit voltage waveforms over all line and load conditions. For the high-frequency quasi-resonant (HFQR) Flyback topology, the switch drain voltage waveform must be carefully inspected and checked to confirm that the absolute maximum ratings are not exceeded (Figure 5). During the switch off-time, the drain voltage rings up and overshoots to a peak level and then settles at a plateau voltage ($V_{PLATEAU}$) = V_{BUS} level + V_{OUT} x N_P/N_S. To guarantee reliability and lifetime requirements, $V_{PLATEAU}$ should not exceed the 80% derated level of 560V. When comparing $V_{DS(CONT)}$ ratings versus other GaN manufacturers (Figure 5), it can be seen that Navitas GaNFast ICs have the highest $V_{DS(CONT)}$ rating (700V). This is due to the Navitas proprietary GaN IC termination design and the extensive reliability testing performed by Navitas, making it the ideal choice for providing enough drain voltage margin to satisfy reliability and lifetime requirements.

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Silicon MOSFETs also have a 700V maximum VB_{DSS} breakdown rating, but the V_{SPIKE} overshoot each switching cycle can exceed this level and cause repetitive and uncontrolled avalanche. As mobile charger and adapter power levels and output voltage levels increase, these maximum voltage ratings will become even more critical and necessary in order to meet acceptable reliability standards.

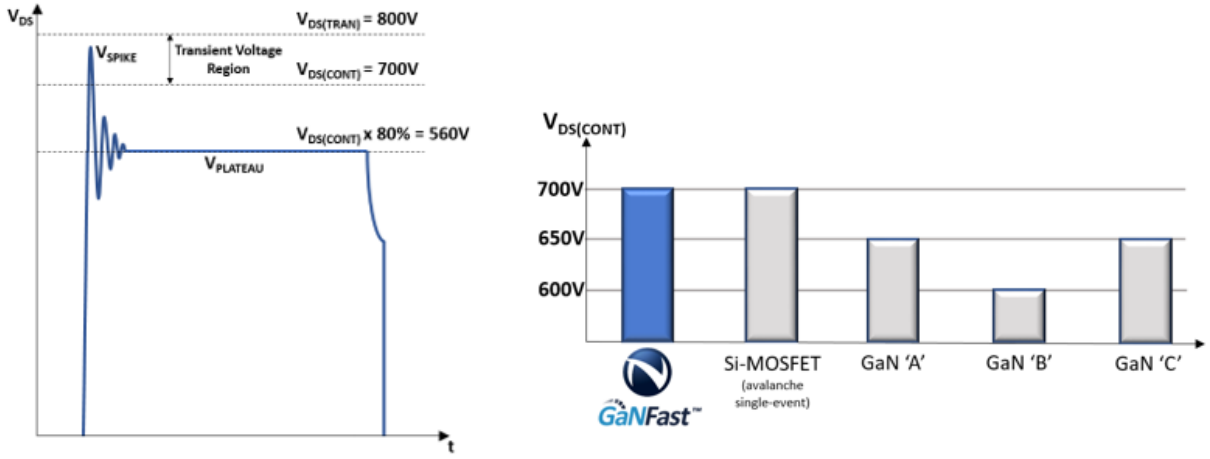

Fig. 5, HFQR flyback drain voltage waveform and $V_{DS(CONT)}$ ratings comparison

Conclusion

In the past, silicon MOSFET manufacturers performed avalanche testing and provided maximum avalanche ratings due to inherent device limitations in order to enable designers to realize their products. Many applications utilized avalanche and a rugged avalanche does give a system designer some comfort about the unforeseen inductive energy spike that might occur. Avalanche can also place circuit limitations on achievable current, voltage and power levels, especially for the QR flyback topology. GaNFast ICs intrinsically block higher voltage levels and this extra voltage margin is used to ride through surges instead of avalanche. This allows circuit topologies to be extended beyond their existing range in both performance and robustness. Combining the highest continuous and transient voltage ratings together with other GaNFast IC integrated features such as gate, drive, protection, and loss-less current sensing, and an industry-first 20-year warranty, we now have a rugged, reliable and proven solution to realize high-frequency, high-density and high-efficiency power supply designs. These ratings are already available today and will only continue to improve in the future.

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