Thermal Simulation Model for Selection of QFN 5x6, QFN 6x8 and QFN 8x8 Package Types

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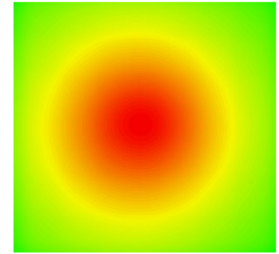


Introduction

Designing a high-frequency and high-density power supply for a specific application and meeting all electrical, mechanical and thermal requirements can be a very challenging task. Part of fulfilling the thermal requirements involves ensuring that the GaN power FET junction temperature (T_J) does not exceed the recommended maximum rating during all line and load conditions, and also keeping the maximum plastic case touch temperature below its maximum allowable level. Selecting the correct QFN package type and $R_{DS(ON)}$ value can be a challenge in itself due to the large portfolio of products available and difficulty in predicting the final system temperatures.

This application note includes a detailed thermal setup and simulations for different power levels for QFN 5x6, QFN 6x8 and QFN 8x8 package types based on top- and bottom-cooled thermal management solutions. The results of these simulations include estimated device junction temperatures (T_J) for different device power loss (P_{LOSS}) values. This model will help guide designers to select the correct $R_{DS(ON)}$ value and QFN package type for their application based on cooling method, device power loss, and resulting device junction temperature (T_J).

Overview

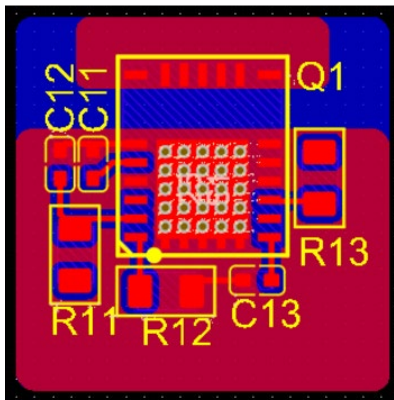
The QFN 5x6, QFN 6x8 and QFN 8x8 package types each have their own unique package dimensions, surface areas, and cooling pad sizes. These all have an effect on the final GaN device junction temperature (T_J) for a given device P_{LOSS}, and cooling method. For top-cooling, the package top side surface area will affect how well the heat can flow from the die upward to the thermal interface material (TIM). For bottom-cooling, the pad size and PCB thermal vias will affect how well the heat can flow from the die downward to the PCB board. These different parameters and cooling methods need to be analyzed further and thermally simulated so we can compare the thermal performance of each package type and help guide designers to more easily select the correct package for their application and thermal requirements.

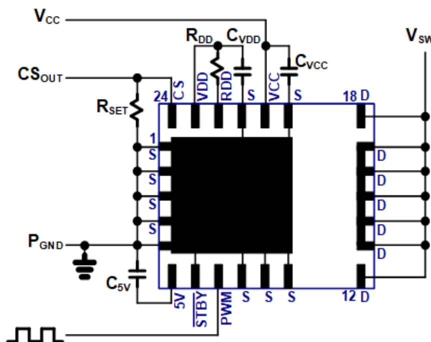
Figure 1. QFN 5x6, QFN 6x8, QFN 8x8 package types

PCB Layouts

2-layer PCB layouts were created for each package type under similar PCB size and copper area conditions (Figure 2). The IC components for each GaN Power IC are included in the layouts since these affect how the heat can flows away from the package in each direction. The components are placed on the top layer and connected with top layer traces (no vias). The remainder of the top side area is filled up with copper (red). The bottom layer copper fills up the complete PCB area on the bottom side. Thermal vias are then placed inside the pad area of each IC, and the heat flows from the pad down to the PCB to the top and bottom layers.

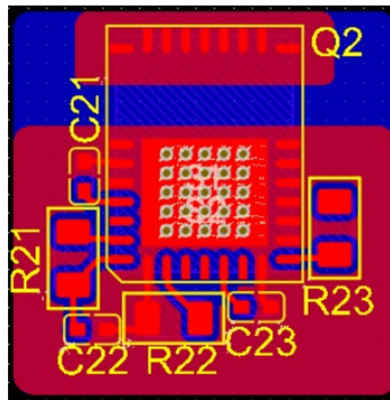
NV615x QFN 5x6

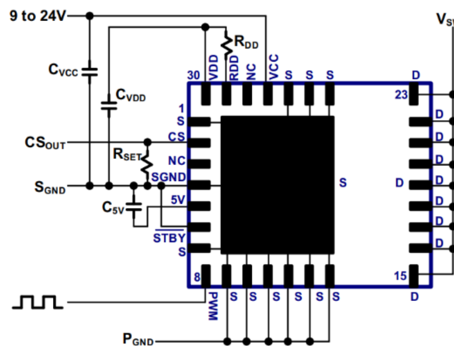




- No. of vias: 25
- Top side Cu area (red): 10 x 13 mm
- Bot side Cu area (blue): 13 x 13 mm
- PCB size: 13 x 13 mm
- PCB thickness: 1.2 mm
- No. of PCB layers: 2
- PCB Copper thickness: 2 oz

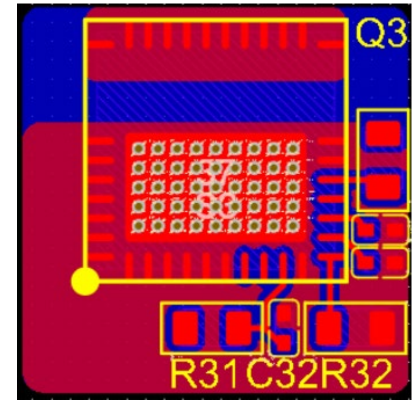
NV613x QFN 6x8

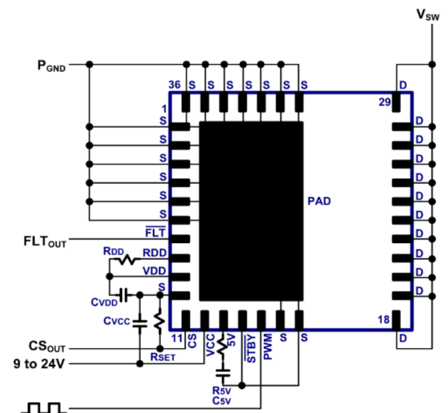




- No. of vias: 25
- Top side Cu area (red): 10 x 13 mm
- Bot side Cu area(blue): 13 x 13 mm
- PCB size: 13 x 13 mm
- PCB thickness: 1.2 mm
- No. of PCB layers: 2
- PCB Copper thickness: 2 oz

NV6169 QFN 8x8





- No. of vias: 45
- Top side Cu area (red): 10 x 13 mm
- Bot side Cu area (blue): 13 x 13 mm
- PCB size: 13 x 13 mm
- PCB thickness: 1.2 mm
- No. of PCB layers: 2
- PCB Copper thickness: 2 oz

Figure 2. Schematic and PCB layouts used for thermal simulations

Thermal Model Stack-Up (Top-Cooled)

The top-cooled thermal model stack-up includes the GaN Power IC QFN mounted on the top side of a FR4 PCB (Figure 3). The heat due to the device power loss thermally conducts from the internal GaN power FET, up through the QFN plastic package, through the TIM and Mylar materials, through the copper shielding, and to the plastic case. The heat then thermally convects from the top surface of the plastic case to the surrounding ambient air. Heat also flows from the device downward to the PCB, and spreads laterally to the sides and then upward through the same materials to the plastic case. So multiple parallel paths of heat flow towards the top side are formed. The bottom area below the PCB is the inside of the power supply unit and it heats up to very high temperature that limits heat flow in the downward direction.

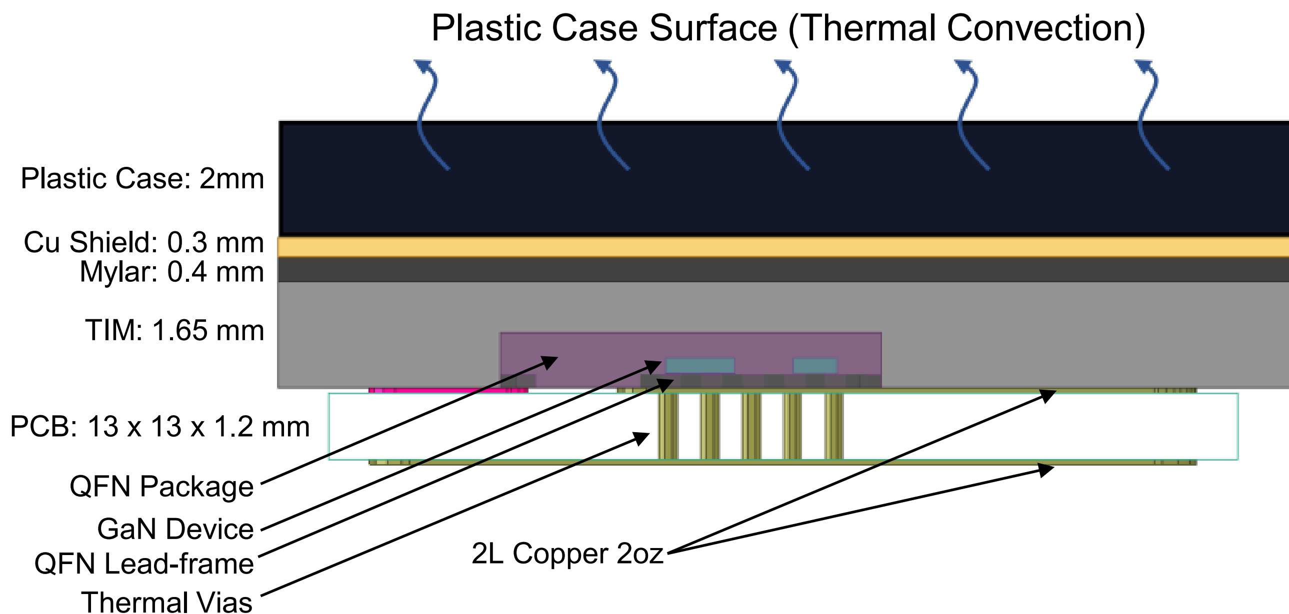


Figure 3. Thermal stack-up for top-side cooling method

Item #	Material	Thickness	Thermal Conductivity
1	Plastic Case	2 mm	11.54 W/m^2K (thermal convection)
2	Copper Shield	0.3 mm	399 W/mK
3	Mylar	0.4 mm	0.17 W/mK
4	TIM	1.65 mm	0.7 W/mK
5	QFN Molding Compound	0.85 mm	1 W/mK
6	QFN Lead Frame	0.2 mm	260 W/mK
7	PCB FR4 w/ 2L & 2oz	1.2 mm	0.35 W/mK
8	Copper thermal vias	Hole = 0.33 mm Dia = 0.65 mm	399 W/mK

Figure 4. Thermal conductivity summary table for top side cooling materials

Thermal Simulation Setup (Top-Cooled)

The top-cooled simulation setup (Figure 4) includes the device and stack-up of materials with additional boundary conditions of 85℃ (fixed) for the other three edges of the closed power supply system. This internal ambient air will increase to high temperatures during the simulation and limit thermal conduction in the downward direction (similar to actual power supply design with power components placed on opposite side of PCB from the device). The closed power supply system is then placed into a larger closed system with the ambient air temperature set at 25℃. This setup is very similar to the thermal testing method of an actual power supply unit on the bench inside an enclosed chamber.

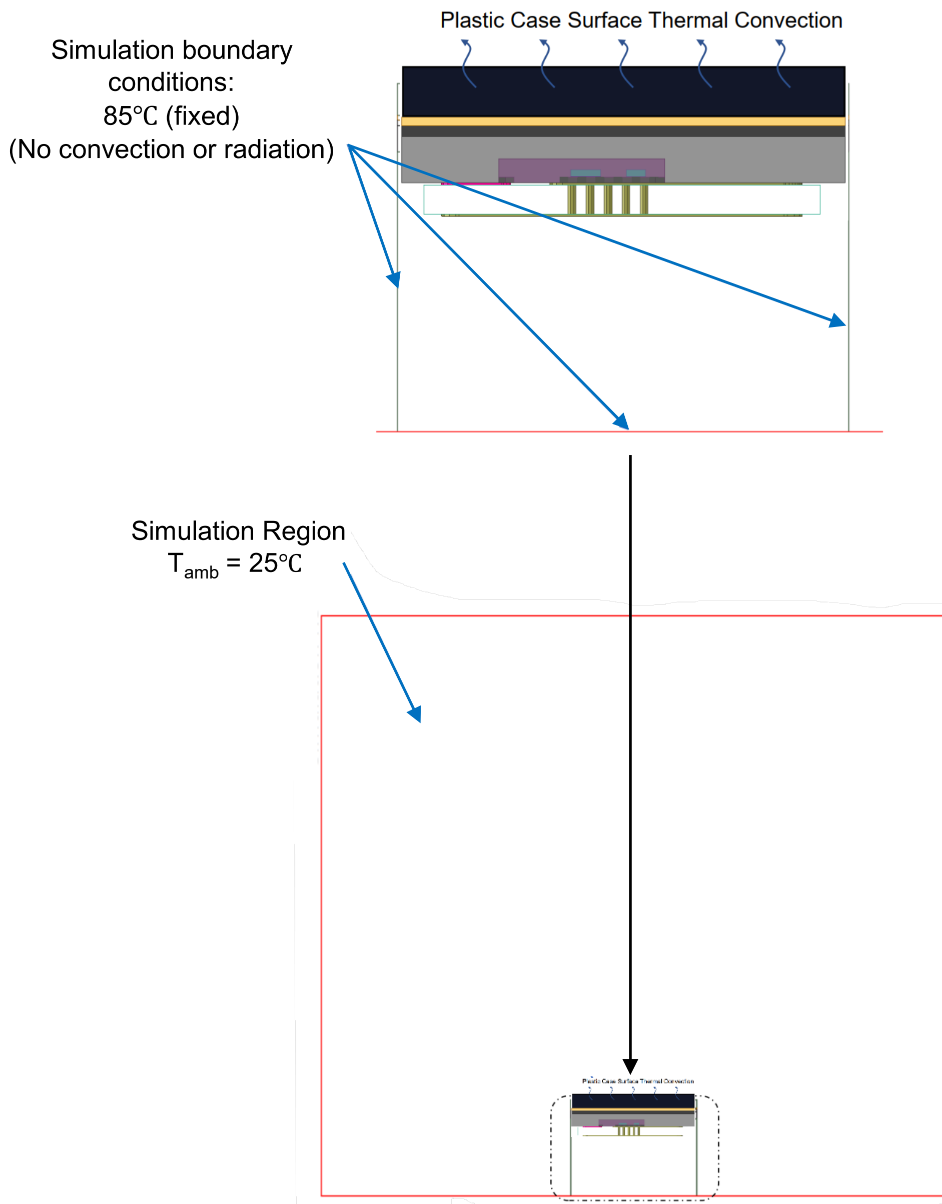


Figure 4. Thermal simulation setup diagrams for top cooling method

Thermal Simulation Results (Top-Cooled)

Top-cooled thermal simulations were run for each package type at 0.5 W, 1 W, and 1.5 W P_{LOSS} conditions, and the target plastic case surface temperature was set at 70℃. The data was then plotted for P_{LOSS} vs T_J, and for each package type (Figure 5). From these curves, the designer can estimate the device T_J temperature for a given P_{LOSS} and package type. At lower P_{LOSS} values (0.5 W) there is a small difference in device T_J temperature between the package types. As P_{LOSS} increases above 1 W, the T_J difference becomes larger. The difference in P_{LOSS} versus T_J for each package type can be used in two ways. For a given $T_{J(MAX)}$ (i.e., 120℃), QFN 8x8 will allow 7% more P_{LOSS} compared to QFN 5x6, or, for a given PLOSS (i.e., 1.28 W), QFN 8x8 will reduce Tj by about 4 deg C compared to QFN 5x6. Depending on the P_{LOSS} for the application and the $T_{J(MAX)}$ target, increasing the package size can help give additional design margin for tolerances.

Top Side Cooling	QFN 5x6	QFN 6x8	QFN 8x8
P_{LOSS}	0.506	0.507	0.507
Plastic Case	70	70	70
Copper Shielding	71.3	71.2	71.2
Mylar	71.3	71.2	71.2
TIM	77.7	77.2	77.0
QFN package	84	83.2	82.8
GaN Die	86	85.2	84.8
P_{LOSS}	0.941	0.940	0.939
Plastic Case	70	70	70
Copper Shielding	71.5	71.5	71.5
Mylar	71.5	71.5	71.5
TIM	87.9	87.2	86.7
QFN package	104.3	102.8	101.8
GaN Die	106.3	104.8	103.8
P_{LOSS}	1.379	1.376	1.374
Plastic Case	70	70	70
Copper Shielding	71.6	71.6	71.7
Mylar	71.6	71.6	71.7
TIM	96.9	95.7	95.0
QFN package	122.1	119.8	118.2
GaN Die	124.1	121.8	120.2

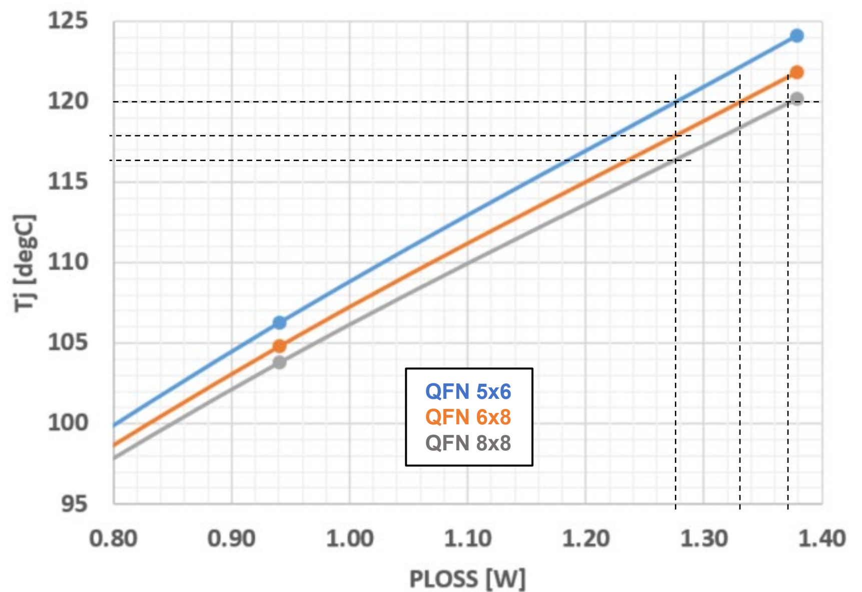


Figure 5. Top-cooled thermal simulation data & curves (P_{LOSS} vs T_J) for different package types

Thermal Model Stack-Up (Bottom-Cooled)

The bottom-cooled thermal model stack-up includes the GaN Power IC QFN mounted on the top side of a FR4 PCB (Figure 6). The heat due to the device power loss thermally conducts from the internal GaN power FET, down through the QFN leadframe, through the PCB and vias, through TIM and Mylar materials, through the copper shielding, and to the plastic case. The heat then thermally convects from the bottom surface of the plastic case to the surrounding ambient air. The top area above the QFN is the inside of the power supply unit and it heats up to very high temperature that limits heat flow in the upward direction.

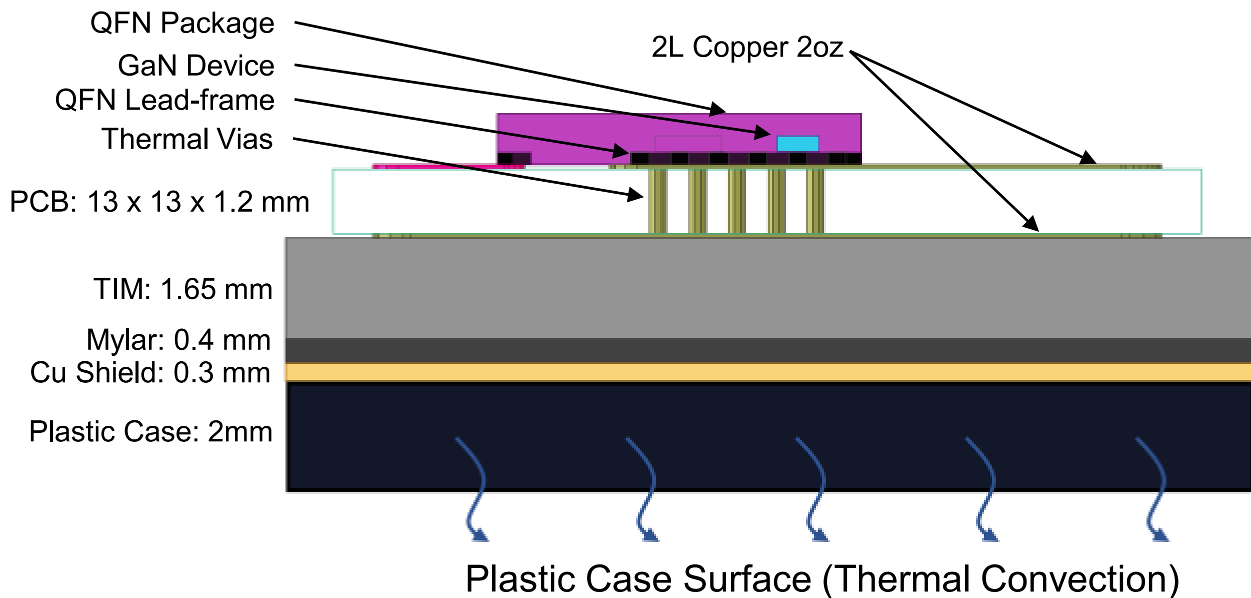


Figure 6. Thermal stack-up for bottom-side cooling method

Item #	Material	Thickness	Thermal Conductivity
1	QFN Molding Compound	0.85 mm	1 W/mK
2	QFN Lead Frame	0.2 mm	260 W/mK
3	PCB FR4 w/ 2L & 2oz	1.2 mm	0.35 W/mK
4	Copper thermal vias	Hole = 0.33 mm Dia = 0.65 mm	399 W/mK
5	TIM	1.65 mm	0.7 W/mK
6	Mylar	0.4 mm	0.17 W/mK
7	Copper Shield	0.3 mm	399 W/mK
8	Plastic Case	2 mm	11.54 W/m^2K (thermal convection)

Figure 7. Thermal conductivity summary table for bottom side cooling materials

Thermal Simulation Setup (Bottom-Cooled)

The bottom-cooled simulation setup (Figure 8) includes the device and stack-up of materials with additional boundary conditions of 85℃ (fixed) for the other three edges of the closed power supply system. This internal ambient air will increase to high temperatures during the simulation and limit thermal conduction in the upward direction (similar to actual power supply design with power components placed on opposite side of PCB from the device). The closed power supply system is then placed into a larger closed system with the ambient air temperature set at 25℃. This setup is very similar to the thermal testing method of an actual power supply unit on the bench inside an enclosed chamber.

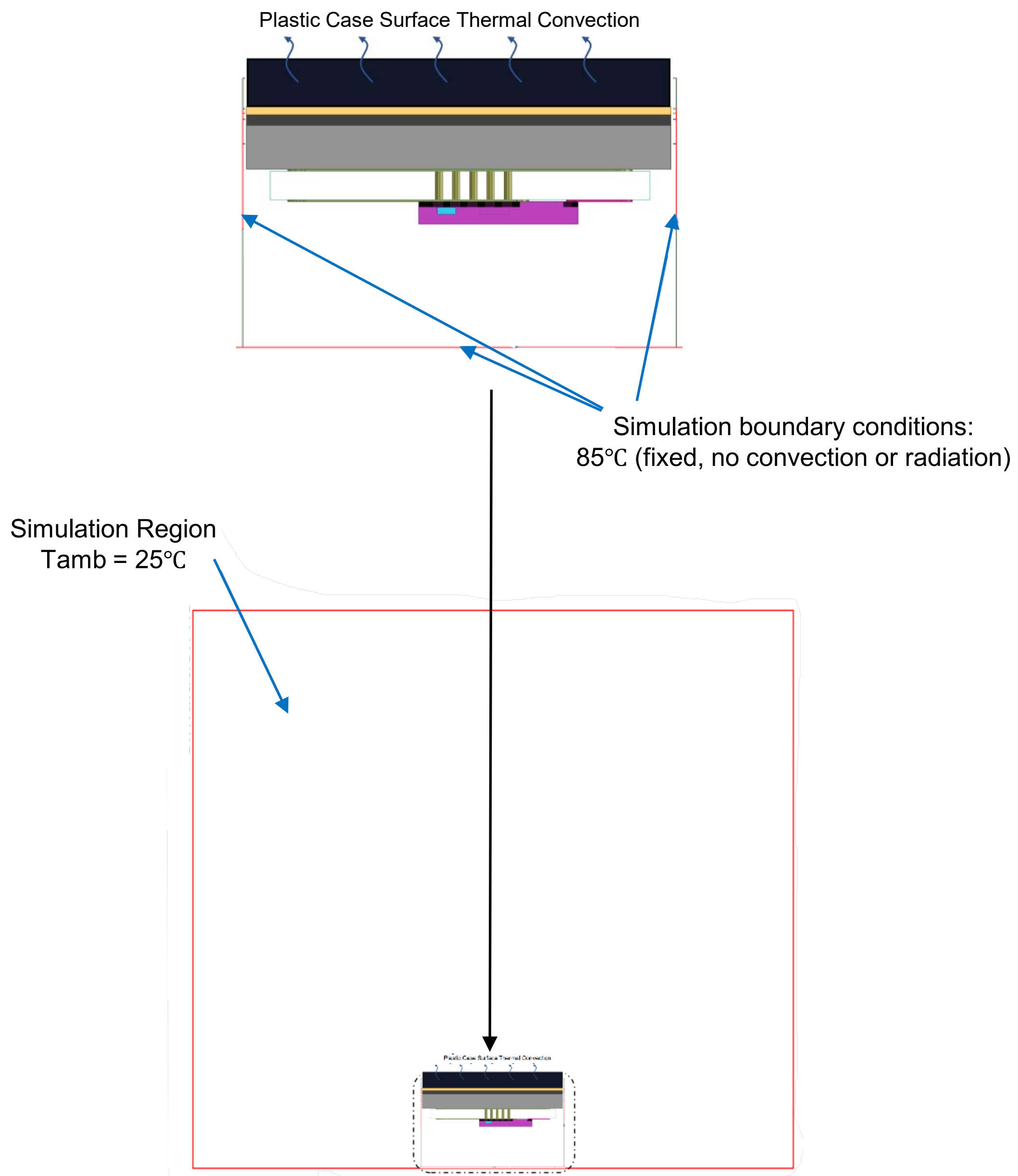


Figure 8. Thermal simulation setup diagrams for bottom cooling method

Thermal Simulation Results (Bottom-Cooled)

Bottom-cooled thermal simulations were run for each package type at different P_{LOSS} values, and again with the target plastic case surface temperature set at 70℃ (figure 9). From these curves, the designer can also estimate the device T_J temperature for a given PLOSS and package type. With bottom side cooling, the T_J temperatures are about 3℃ lower than compared with top side cooling, for the same P_{LOSS} value (i.e., 1.35 W). The same trade-off as top-cooled also exists for bottom-cooled for the different package types. When increasing the package size from QFN 5x6 to QFN 8x8, the designer can increase the PLOSS budget for a given T_J, or reduce T_J for a given P_{LOSS}.

Bottom Side Cooling	QFN5x6	QFN6x8	QFN8x8
P_{LOSS}	0.552	0.554	0.557
GaN Die	89.6	89	88.2
GaN Pad	86.5	86	85.2
Bottom of PCB	83.5	83	82.7
Copper Shielding	71.7	71.8	71.7
Plastic Case	70	70	70
P_{LOSS}	1.028	1.038	1.038
GaN Die	107.7	106.3	104.6
GaN Pad	101.6	100.3	98.7
Bottom of PCB	95.6	94.3	93.4
Copper Shielding	72.1	72	72.1
Plastic Case	70	70	70
P_{LOSS}	1.500	1.512	1.511
GaN Die	125.7	123.5	120.9
GaN Pad	116.5	114.7	112
Bottom of PCB	107.5	106.1	104.9
Copper Shielding	72.3	72.2	72.3
Plastic Case	70	70	70

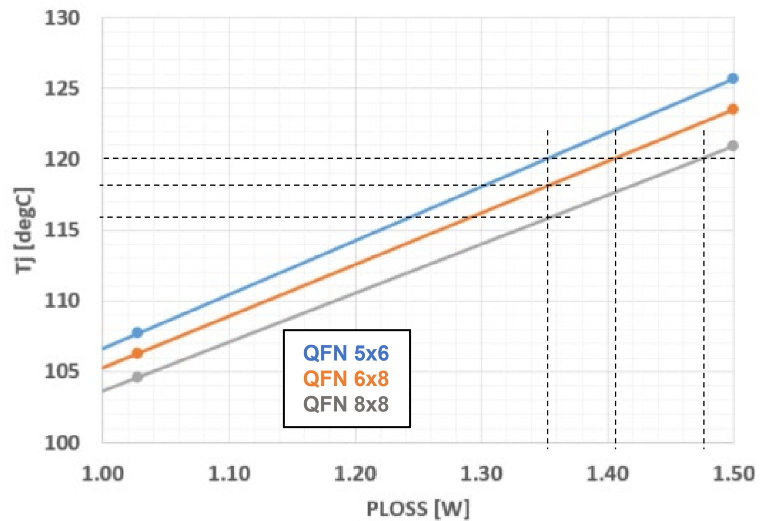


Figure 9. Bottom-cooled thermal simulation curves (P_{LOSS} vs T_J) for different package types

$R_{DS(ON)}$ and Package Type Selection

A typical 65 W HFQR Flyback circuit will have 1.5 A_{RMS} current flowing in the primary side switch at 90 V_{AC} and 100% output load. The P_{LOSS} values at this 1.5 Arms condition are calculated for different $R_{DS(ON)}$ values (Table 1), and the corresponding T_J values for top and bottom cooling methods are obtained from the thermal simulation graphs (Figure 10). From the summary table, the designer can select from different $R_{DS(ON)}$ values and package types, depending on P_{LOSS}, T_J, and preferred cooling method. From the data, $R_{DS(ON)}$ = 260mΩ gives high T_J values close to or greater than 115℃ for all top-cooled options, as well as bottom-cooled QFN 5x6. $R_{DS(ON)}$ = 170m gives very low T_J values close to 100℃ for all cooling methods and package types. $R_{DS(ON)}$ = 210mΩ looks like a reasonable selection due to T_J values below 110℃ for all cooling methods and package types (which allows for good T_J margin away from a Tj-max = 120℃). The designer can further optimize for package type selection based on cooling method and PCB footprint area.

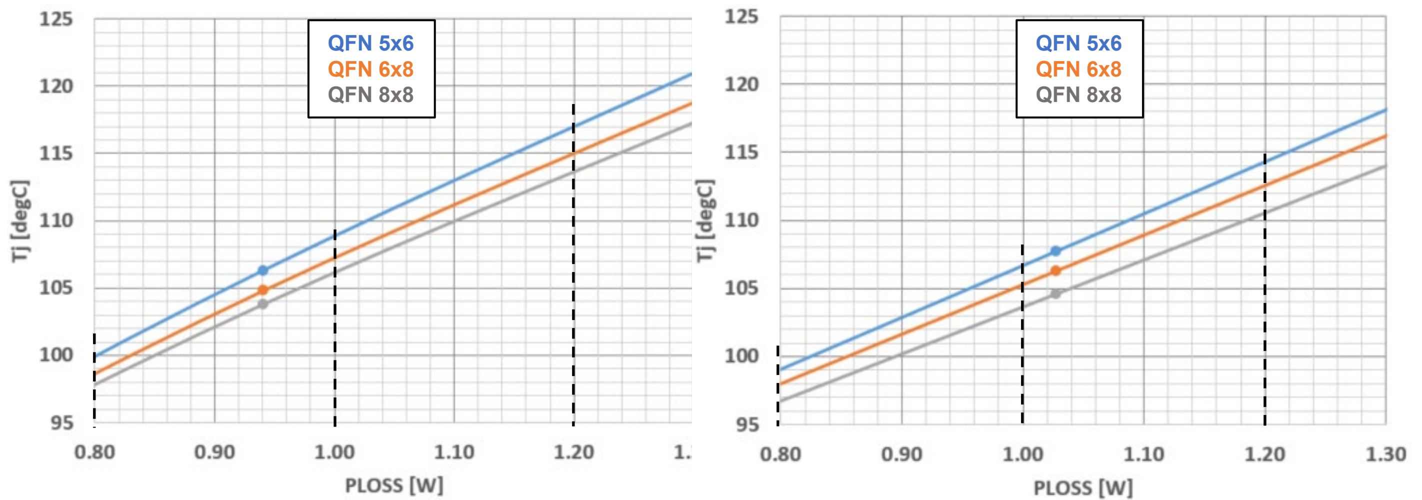


Figure 10. Top-cooling (left) and bottom-cooling (right) thermal simulation curves

$R_{DS(ON)}$ Typ_25C [mΩ]	$R_{DS(ON)}$ typ_125C [mΩ]	I_{SWITCH} [A_{RMS}]	P_{LOSS} [W]	T_J QFN5x6 Top-Cooled [°C]	T_J QFN6x8 Top-Cooled [°C]	T_J QFN8x8 Top-Cooled [°C]	T_J QFN5x6 Bot-Cooled [°C]	T_J QFN6x8 Bot-Cooled [°C]	T_J QFN8x8 Bot-Cooled [°C]
260	520	1.5	1.2	117	115	114	114	112	111
210	420	1.5	1.0	109	107	106	107	105	104
170	340	1.5	0.8	100	99	98	99	98	97

Table 1. I_{SWITCH}, P_{LOSS}, and T_J estimates for different $R_{DS(ON)}$ values (65 W HFQR Flyback Circuit, 90 V_{AC}/100%)

Conclusions

These thermal simulations are intended to be used as a guide for designers to estimate the T_J and help select the correct $R_{DS(ON)}$ and package type for a given P_{LOSS} and cooling method. The T_J temperature differences between the different package types are typically between 3-5℃ at P_{LOSS} values above 1 W, and these differences can help greatly when designing a power supply for worst case conditions and design margin is required. The thermal simulations have also shown that these differences can allow for higher $R_{DS(ON)}$ values to be used (in a larger package), especially if bottom-cooling method is used. Final results with actual power supply measurements may vary depending on the final materials used in the thermal stack-up and their thermal conductivity values.

References (www.navitassemi.com)

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2) Thermal Management of GaNFast NV612x Power IC, AN011, Navitas Semiconductor, 2019
3) GaNFast NV613x/NV615x, NV6169 Power ICs with GaNSense Technology datasheets, Navitas Semiconductor, 2021/2022

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