3.3 kV SiC MOSFETs Accelerate Grid-Connected Energy Storage

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Navitas' GeneSiC trench-assisted planar-gate silicon carbide (SiC) MOSFETs offer cool, rugged performance

The grid supplies energy from generators and delivers it to customers via transmission and distribution (T&D) networks. In the U.S., use of electricity storage to support and optimize T&D has been limited due to high storage costs and limited design and operational experience. Recent improvements in storage and power technologies, however, coupled with changes in the marketplace, herald an era of expanding opportunity for electricity storage.

Figure 1 illustrates the future vision for electricity production and T&D infrastructure, identifying grid-connected storage as critical for more reliable, more cost-effective models. Energy storage improves T&D performance by compensating for electrical anomalies and disturbances such as: (A) variations in voltage, (e.g., short-term spikes or dips, longer-term surges, or sags); (B) variations in the primary frequency at which power is delivered; (C) low power-factor (voltage and current excessively out of phase with each other); (D) harmonics (the presence of currents or voltages at frequencies other than the primary); (E) interruptions in service.

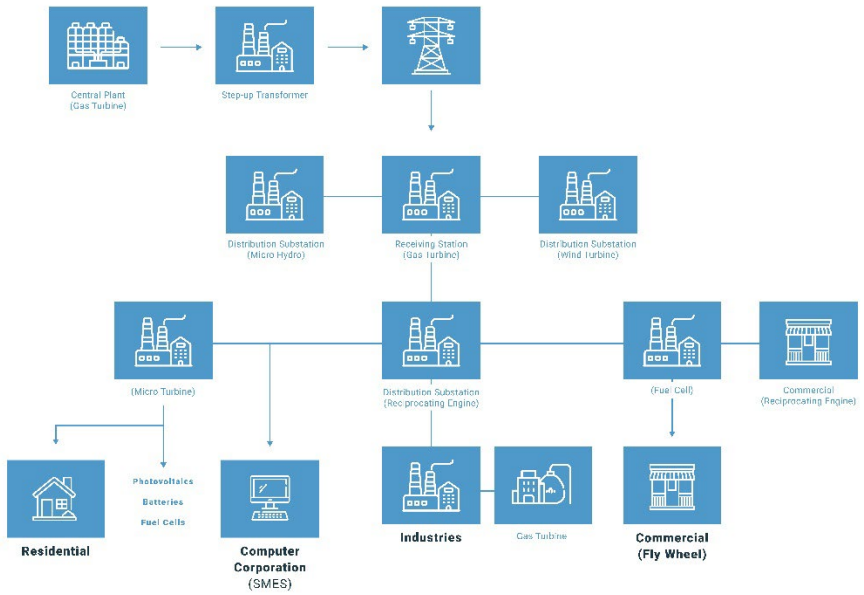

Fig. 1: Grid-connected energy storage elements are critical to future power transmission and distribution.

Utility-attached storage reduces costs by allowing purchase of inexpensive electricity during periods of low demand and supply of that energy when the price would otherwise be higher. Storage may also be used in lieu of adding generation capacity. In many areas, transmission capacity is not keeping pace with peak demand, meaning transmission systems are becoming congested - driving increased transmission access charges and use of congestion charges or "locational marginal pricing".

Storage is also increasingly used to balance out intermittent power supplies from renewable energy resources such as wind and solar.

Silicon Carbide Drives Storage Innovation

Use of all-SiC inverters will revolutionize electricity delivery, renewable energy integration and energy storage. It is well-recognized that silicon-based semiconductors have inherent limitations that reduce their suitability for utility-scale applications. With SiC, applications including static transfer switches, dynamic voltage-restorers, static VAR compensators (SVCs), high-voltage direct-current (HVDC) transmission and flexible alternate-current transmission systems (FACTS) all become economically viable. With SiC, medium-voltage inverter manufacturers can realize efficiencies of >97.8% at 100 kW - 1 MW, allowing more compact inverters to be deployed at large scale across residential and industrial implementations.

Integrating a Battery Energy Storage System (BESS) with Medium Voltage (MV) Grid

A BESS is integrated to an MV grid (2.3 kV, 4.16 kV or 13.8 kV) using an isolated topology such as a dual active bridge (DAB) followed by an active front-end converter (AFEC). A three-level, neutral-point clamped topology both reduces filter requirements compared to a two-level topology, and the voltage stress across the SiC MOSFETs[i]. Depending on grid voltage, a series connection of the SiC 3.3 kV MOSFET-Diode devices is possible as shown in Figure 2. The LV side is made through 1,200 V SiC devices. In the DAB, the MV transformer (LV to MV conversion) can be operated between 10 - 20 kHz. Single or three-phase system can be used depending on the power requirements.

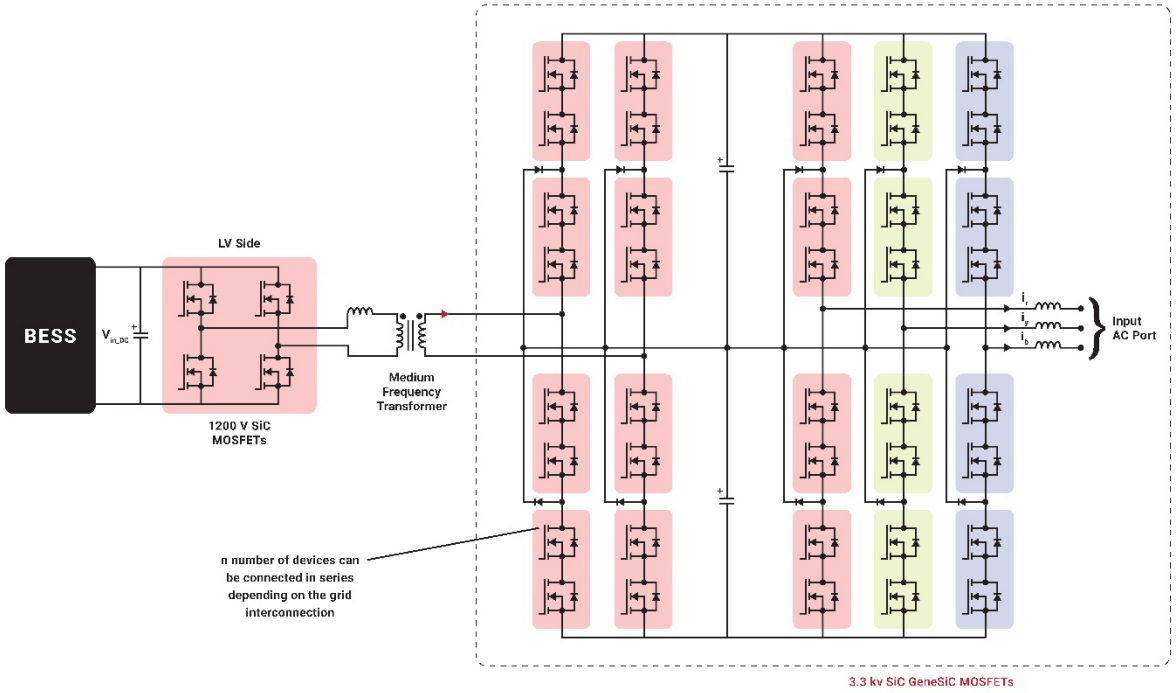

Fig. 2: System topology for interconnecting the BESS system to an MV grid

The MV SiC MOSFETs' fast switching-transients can result in a dV/dt as high as 100 kV/µs, imposing a requirement for a very low isolation capacitance in the gate drive circuit[ii]. Power transmission stage design objectives are high isolation requirements, low coupling capacitance and optimized gate-driver footprint. In general, MV applications require series connection of devices for redundancy and high operating voltages. Series connection of MV SiC devices requires gate drivers that can switch all devices simultaneously. Delay in turn on of the series connected devices may result in voltage mismatch, leading to overvoltage or improper voltage sharing across devices.

Using single 3.3 kV SiC MOSFET-diodes to replace series-connected 1.2 - 1.7 kV MOSFETs or IGBTs has tremendous advantages including simple gate drive, reduced parasitic inductance, lower conduction losses and higher efficiency. Overall size, weight and cooling requirements of the power converter can, therefore, be significantly reduced.

Tests of circuit efficiency and junction temperatures on a 3.3 kV / 400 A GeneSiC SiC MOSFET, 3.3 kV / 400 A Si IGBT and a series connection of two 1.7 kV / 325 A SiC MOSFETs from a third party in a 4.16 kV modular multi-level converter revealed significant benefits of the 3.3-kV SiC MOSFETs. In general, the 3.3-kV SiC MOSFETs reduced losses and enabled a smaller installed semiconductor die area, improving the power density of the system (including volume of heat sinks and fans).

3.3. kV SiC MOSFET with Monolithically-Integrated MPS Diode

Further efficiency and reliability advantages can be achieved by monolithically integrating a Merged PiN Schottky (MPS) diode within the MOSFET. This enables free-wheeling diode operation (low conduction and switching losses) without an externally-connected Schottky diode, while reducing the parasitic inductance associated with an external diode connection. Furthermore, this bypasses the built-in P-Well/N-Drift body-diode of the DMOSFET structure whose operation can induce faulting of the basal-plane dislocations inevitably present within the N- drift layer of the DMOSFET.

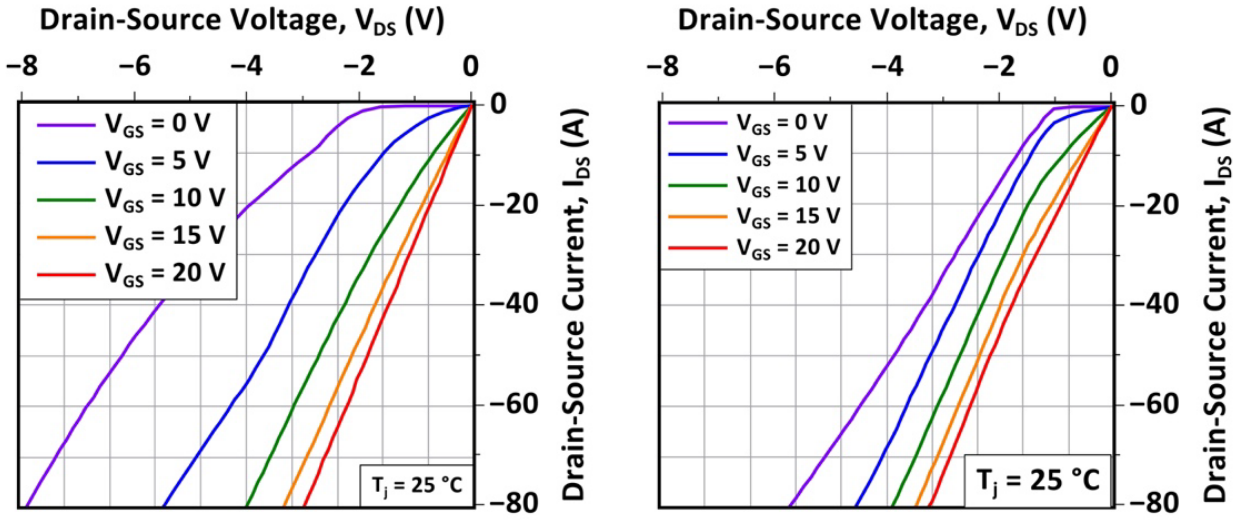

Fig. 3: Third-quadrant I-V characteristics measured on 3.3 kV, 40 mΩ, discrete SiC MOSFET (left) and SiC MOSFET with monolithically-integrated MPS diode (right)

Advantages include more efficient bi-directional performance, temperature independent switching, low switching and conduction losses, reduced cooling requirements, superior long-term reliability, ease of paralleling and lower costs.

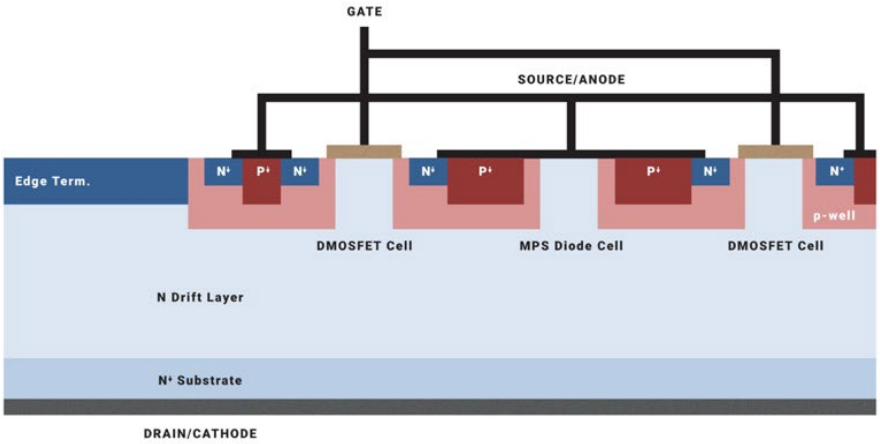

Fig. 4: Cross-sectional device schematic of 3.3 kV SiC MOSFET with monolithically-integrated Schottky rectifier.

Navitas' GeneSiC 3.3 kV discrete SiC MOSFETs and SiC MOSFETs with monolithically integrated MPS diodes typically have a breakdown voltage range of 3.6 – 3.9 kV, well above the datasheet value. When implementing a monolithic diode, there is a slighter higher drain leakage current observed at elevated voltages, due to Schottky barrier lowering under high electric fields. Figure 5 shows that in tests GeneSiC mono-SiC MOSFETs demonstrated typical breakdown voltages of 3.5 - 3.7 kV with leakages $\approx$ 50 µA (or 0.3 mA/cm^2) at the rated 3.3 kV blocking voltage, for an $R_{DS(ON)}$ of approximately 80 mΩ (measured).

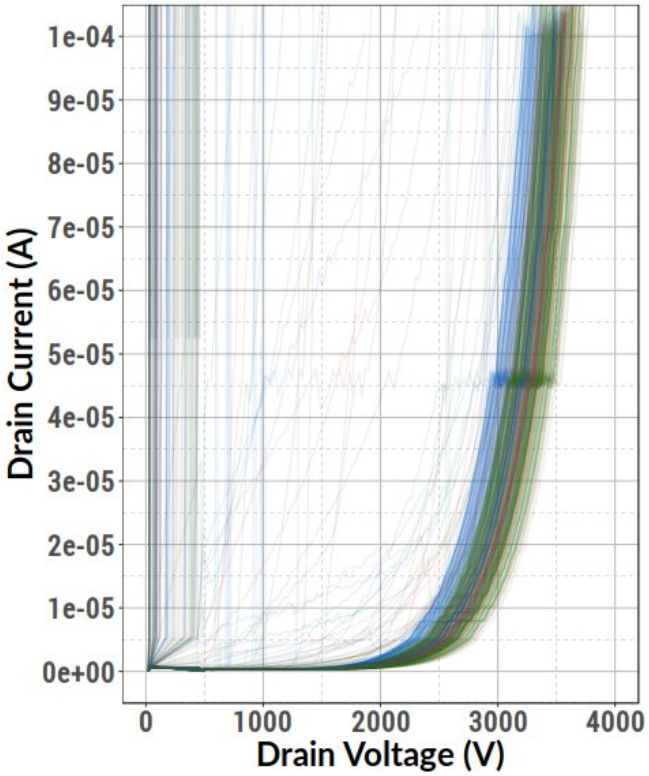

Fig. 5: 3rd Quadrant breakdown characteristic measured on 3.3 kV SiC MOSFETs with monolithically-integrated MPS diodes.

Unclamped inductive switching (UIS) switching measurements were used to investigate avalanche robustness of the 3.3 kV SiC MOSFETs with integrated MPS diodes. The drain current/voltage waveforms at a peak drain current of 30 A are shown in Fig. 6. Drain voltage rises to a maximum of 4,200 V during the test and a maximum avalanche-withstand time (t_{AV}) of 35 µs and single-pulse avalanche energy (E_{AS}) of 2.6 J (or 7.6 J/cm^2) are extracted from the UIS measurements. In comparison, the test performed on a discrete 3.3 kV discrete SiC MOSFET with the same load-inductance extracted an E_{AS} of 4.8 J.

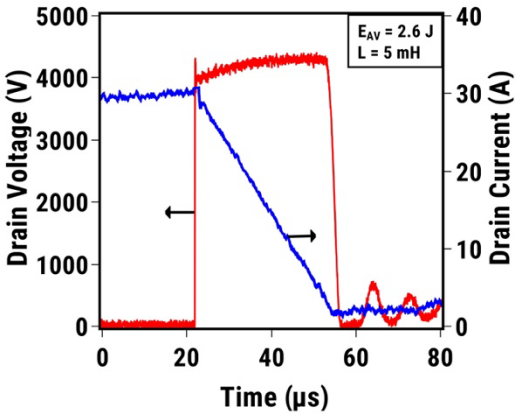

Fig. 6: Drain current and voltage waveforms from UIS measurement performed on a 3.3 kV SiC MOSFET with monolithically-integrated MPS diode.

Short-Circuit Robustness

The short-circuit robustness of the GeneSiC MOSFETs was evaluated by subjecting 3.3 kV discrete SiC MOSFETs with and without monolithically-integrated MPS diodes to a 1,200V DC link. A +20 V / -5 V gate-drive scheme was used and the device was mounted on a 25°C baseplate. The drain current increases to a maximum of 525 A during the short-circuit pulse and a short-circuit withstand time of 4.5 µs was measured (Fig. 7).

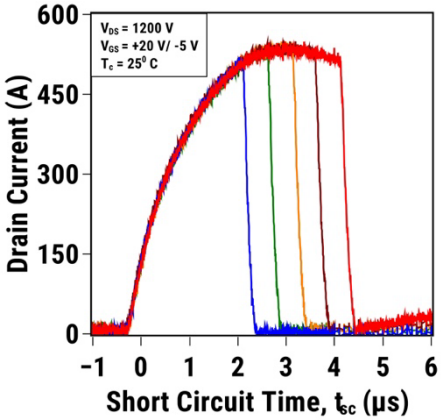

Fig. 7: Drain-current waveform recorded during a short-circuit test performed on a 3.3 kV SiC MOSFET with monolithically-integrated MPS diode at a DC-link voltage of 1,200 V.

Summary

Deploying SiC in inverters will accelerate the adoption of energy-storage technologies and make them critical elements of future grids. Integrating a BESS to an MV grid through an isolated topology shows that using 3.3 kV single SIC MOSFETs enables higher system efficiency, lower operating temperature, and smallest die size, compared to an equivalent silicon IGBT or two 1,700V SiC MOSFETs in series.

GeneSiC 3.3 kV SiC MOSFETs with monolithically-integrated monolithic MPS diodes achieve breakdown voltages well above 3.3 kV and demonstrate smooth switching performance while fully activating the monolithic MPS diode. This significantly reduces power losses in third quadrant operation and enhances device reliability by alleviating bipolar degradation. UIS testing reveals a robust avalanche capability and short circuit withstand times to 4.5us.

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Additional Information

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