GaN-based High Frequency and High-power Density 2-in-1 Bidirectional OBCM Design for EV Application

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Introduction
- The integrated design of OBC and LV DC/DC can reduce the system size, improve the power density and reduce the cost.
- Wide-band gap semiconductor device GaN brings an opportunity to further improve the power density of Power-Supply-Unit in EV.

System Topology
- Interleaved CCM Totem-pole PFC for Bi-AC/DC Stage.
- Bi-directional CLLC with delay-time control of wide voltage range output, ZVS and high switching frequency (450 kHz~1.2 MHz) range for Bi-DC/DC Stage.
- Hard switching full bridge for LV DC/DC.
- All 650V GaN devices for high voltage side.

Bi-AC/DC Stage
- Totem-pole PFC per phase parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vac</td>
<td>220 V</td>
</tr>
<tr>
<td>iac_RMS</td>
<td>16 A</td>
</tr>
<tr>
<td>Vbus</td>
<td>400 V</td>
</tr>
<tr>
<td>f_Line/f_s</td>
<td>50 Hz / 100 kHz</td>
</tr>
</tbody>
</table>

$$L_{PFC\_min} = \frac{V_{bus}^2}{k_{Ripple} \cdot \sqrt{2} \cdot I_{Ac\_RMS} \cdot 2 \cdot f_s}$$

- Usually, the value of $$k_{Ripple}$$ is set to 1 for per-phase current. Based on the parameters in Table 1, minimum inductance satisfying the demand is 45 uH.
- High-flux core, low loss for high frequency applications, volume is reduced by about 20% compared with the traditional 50 kHz PFC inductor design.

Bi-DC/DC Stage
- LC resonant circuit as a second-order system is suitable for phase plane analysis.
- Delay-time control can achieve high gain output adjustment for DC/DC.

Phase plane analysis for half switching cycle
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**Characters of Bi-DC/DC Stage and Mag. Design**

- $f_{s} > f_{r}$ is maintained throughout the output voltage range and keeping "V" shape.
- Larger Angle $\alpha$ means larger system gain.
- Narrow $f_s$ range and good for transformer design.

**Functions of Navitas NV651X-series GaN devices**

- 12~18 V for DRIVE to SK.
- Integrated level-shift and deglitch circuit for improved anti-interference performance
- GaNFast power ICs are easy-to-use, highspeed, high-performance ‘digital-in, power-out’ building blocks.
- Monolithic integration of GaN gate drive & GaN power stage enables “zero loss in turn-off because the gate-drive loop has ~zero impedance,” eliminates parasitic gate-loop inductance and prevents gate ringing and glitching.

**2-in-1 OBC Prototype and key waveforms**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{cc}$</td>
<td>85-265 V</td>
</tr>
<tr>
<td>$V_{bat}$</td>
<td>250-500 V</td>
</tr>
<tr>
<td>$f_{s}$</td>
<td>32 A</td>
</tr>
<tr>
<td>$f_{s}$</td>
<td>23.5 A</td>
</tr>
<tr>
<td>Power</td>
<td>$6.6$ kW charging, $220$ $V_{bat}$/6.0 kVA discharging</td>
</tr>
<tr>
<td>$L_{DC}$</td>
<td>50 $\mu$H</td>
</tr>
<tr>
<td>$f_{s}$</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Res. Inductor</td>
<td>4.0 $\mu$H</td>
</tr>
<tr>
<td>Res. Cap.</td>
<td>40 $nF$ (equivalent)</td>
</tr>
<tr>
<td>Res. Frequency</td>
<td>400 kHz</td>
</tr>
<tr>
<td>Trans. turns ratio</td>
<td>1.2</td>
</tr>
</tbody>
</table>

**Thermal and Efficiency**

- GaN device are all below 110°C which verifies the feasibility of heat dissipation.
- GaN based high-frequency transformer is more than 50% smaller than that of Si based design.

**Discharging 6.0 kVA non-linear load**

**Prototype "2-in-1" OBC dimensions**

- Platform set-up

**GaNFast functionality**

**Typical double-pulse test waveform**

**Comparison of transformer volumes at different $f_{s}$**

**Table 2 Main parameters of 2-in-1 OBC**

- Volume 2.46 L
- Power 6.0 kW
- Efficiency
  - Charging mode: 94.57%
  - Discharging mode: 95.33%

**Efficiency of OBC @ charging and discharging**

- Efficiency of HV-LV DC-DC
  - Charging mode: 95.36%
  - Discharging mode: 95.32%

**Efficiency of HV-UV DC-DC**

- Charging mode: 93.89%
- Discharging mode: 93.35%

**Platform set-up**

**Discharging 6.0 kVA non-linear load**

**Feasibility of GaN in high power, high-frequency applications is verified**

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