# 1200 V SiC JBS Diodes With Ultra-Low Capacitive Reverse Recovery Charge For Fast Switching Applications

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### I. Introduction

SiC JBS diodes offer exceptional features that include but are not limited to high temperature operation, high blocking voltages and fast switching capabilities[i]. This document presents the superior switching performance delivered by GeneSiC's 1200 V/12 A SiC JBS diode when compared with SiC Schottky diodes from other manufacturers and fast recovery Si diodes (FREDs).

A Schottky diode, unlike a PIN rectifier is a majority carrier device and therefore has no minority carriers stored in the drift layer during the forward operating mode, resulting in a zero reverse recovery current (attributed to stored charge). However, the thinner and more heavily doped voltage blocking layer in a SiC Schottky diode typically possesses a higher junction capacitance as compared to a Si PIN diode of the same voltage rating. As a result, there is a small yet finite reverse recovery current in SiC Schottky diodes due to the capacitive displacement current. However, unlike the reverse recovery characteristics displayed by Si PIN diodes, the capacitive recovery characteristics observed in SiC Schottky diodes are independent of temperature, forward current level as well as turn-off dI/dt. In Si technology, impractical epitaxial specifications relegate Schottky diodes to < 600 V applications. GeneSiC's 1200 V SiC Schottky diodes are specially designed to minimize the capacitive charge, thereby enabling faster switching transients.

### II. Turn-Off measurements

An inductively loaded chopper circuit shown in Figure 1 is used for investigating the turnoff characteristics of the diodes. The commonly used double-pulse method is applied for inducing a reverse recovery transient as the diode turns off from a conducting state[ii]. During the first gate turn-on pulse, the IGBT ($Z_1$) is turned on and the diode, $D_1$ is in the blocking state. When $Z_1$ is turned off, the inductor current flows through $D_1$, which then becomes forward biased. During the second gate turn-on pulse applied to $Z_1$, the diode $D_1$ will turn off and any reverse recovery/capacitive current of $D_1$ will add to the turn-on current of $Z_1$.

Turn-off measurements were performed on various 1200 V SiC Schottky and Si Ultrafast recovery diodes to investigate the reverse recovery characteristics at junction temperatures of 25 °C and 150 °C. The total turn off charge is the sum of the capacitive and reverse recovery (RR) charge. The turn-off charge is calculated by integrating the RR current over the RR time.

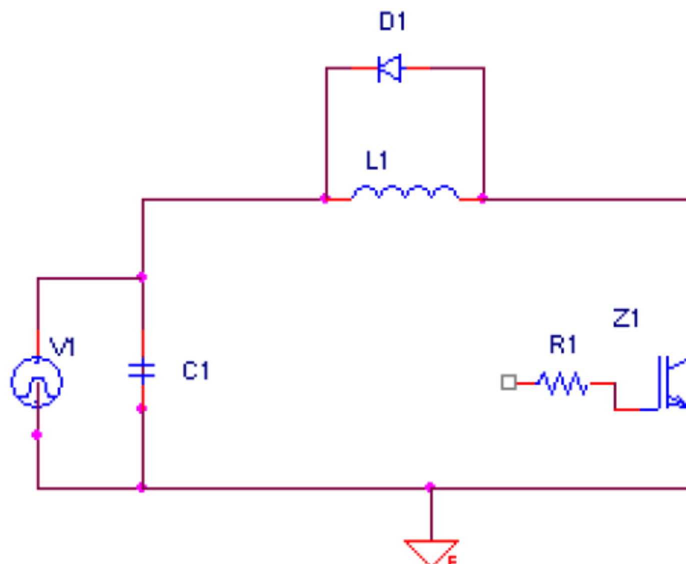


**Fig. 1: Schematic of the test circuit used for investigating turn-off characteristics of diodes**

The RR peak currents ($I_{RR}$) and RR times ($t_{rr}$) of the 1200 V/12 A GeneSiC SiC JBS diode are the lowest when compared to competitor SiC Schottky diodes as well as the Si FRED (Figure 2). High-temperature operation of a PiN diode increases the lifetime of the injected minority carriers, thereby increasing the RR charge which is evident in Si FREDs. In contrast, the absence of stored charge in the majority carrier SiC Schottky diodes implies that any observed reverse recovery charge is purely capacitive in nature. A definitive signature of capacitive reverse recovery is a temperature independent RR charge which can be discerned from Figure 2 for all the SiC Schottky diodes. The low RR charge of GeneSiC diodes indicates superior switching performance over the other SiC Schottky diodes and Si FREDs.

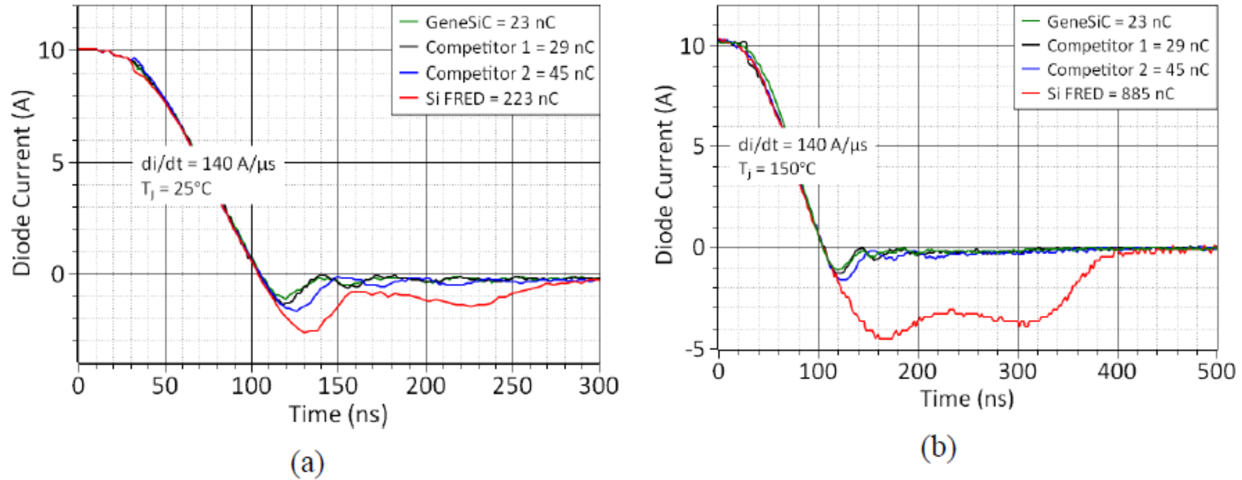


**Fig. 2: Turn-off characteristics of 1200 V/12 A GeneSiC, 1200 V/10 A competitor and 1200 V/15 A Si FRED diodes at junction temperatures of (a) 25 °C and (b) 150 °C. The integrated RR charge is indicated next to the corresponding diode type.**

## III. Capacitance-Voltage Characterization

Capacitance-Voltage (C-V) characterization of high-power diodes is critical for determining the epi-layer doping, built-in potential of the Schottky contact and chip size. The junction capacitance of a power diode represents the variation of depletion charge with respect to the applied reverse bias. The differential capacitance decreases gradually with increasing reverse bias until the punch-through voltage is reached, and then saturates at voltages higher than the punch-through limit[iii]. The punch-through voltage, $V_{PT}$ for a Schottky diode can be expressed as:

$$V_{PT} = \frac{qN_D W^2}{2\epsilon_S} \tag{1}$$

where ‘$q$’ is the electronic charge, ‘$N_D$’ is the epi-layer doping, ‘$W$’ is the epi-layer thickness and ‘$\epsilon_S$’ is the semiconductor permittivity. The punch-through voltage of GeneSiC’s 1200 V diodes is calculated as ≈ 740 V using equation (1).

Differential C-V measurements were conducted on GeneSiC's 1200 V/12 A SiC Schottky diode and the two other competitor 1200 V/10 A SiC diodes (Figure 3) up to 200 V with a 1 V step using an LCR meter and an external power supply. The C-V data was extrapolated till the punch-through limit for the GeneSiC diode, using the linear relationship between ($1/C^2$) and applied reverse voltage ($V_R$). The differential capacitance was assumed to be constant beyond the punch-through limit (the validity of this assumption was confirmed by device simulations). The zero bias capacitance ($C_{J0}$) for the GeneSiC diode is significantly lower than the $C_{J0}$ measured on the competitor diodes, as a result of the special device/process design used for fabrication. The lower $C_{J0}$ is partly responsible for the lower reverse recovery charge obtained for the GeneSiC diode, as shown in Figure 2. A capacitive charge ($Q_c$) of 36 nC is extracted by integrating the CV curve up to 1000 V. This low value of $Q_c$ is in reasonable agreement with the $Q_c$ extracted from the reverse recovery characteristics shown in Figure 2. The somewhat higher value of capacitive charge (36 nC) obtained from C-V results compared to the turn-off charge (23 nC) is attributed to the measurement error and the approximations used for the extrapolation of C-V graph.

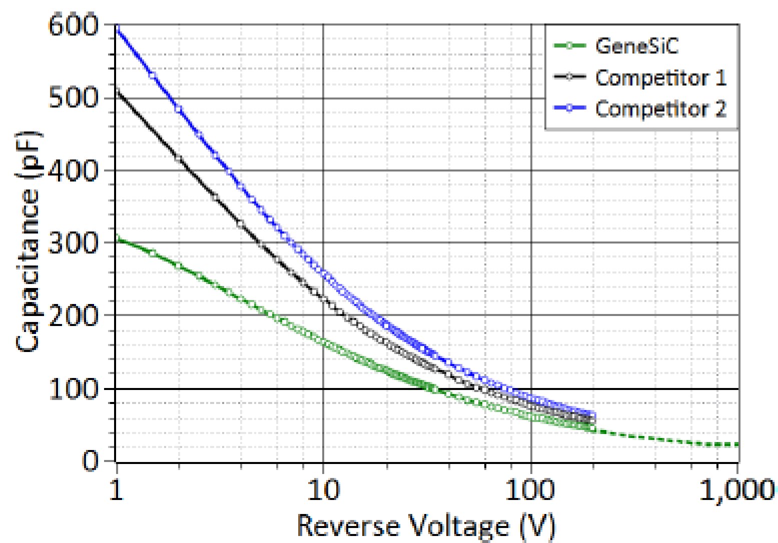


**Fig. 3: Capacitance - Voltage characteristics of GeneSiC 1200 V/ 12 A JBS diode.**

**References**

i. R. Singh et al. “Large Area, Ultra-high Voltage 4H-SiC p-i-n Rectifiers”, IEEE Transactions on Electron Devices, 49(12), 2002, pp.2054-2063

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iii. T. Funaki et al. “Evaluation of High Frequency Switching Capability of SiC Schottky Barrier Diode based on Junction Capacitance Model”, IEEE Transactions on Power Electronics, 23(5), 2008, pp.2602-2611.

## Additional Information

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